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Z86017

PCMCIA Interface

Product Specification

PS010902-0901

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Table of Contents

List of Figures

List of Tables

Z86017 PCMCIA Interface

Features

- 256 Bytes of Attribute Memory
- Five Configuration Registers
- Direct Memory Access (DMA) Support
- EEPROM Sequencer Circuitry for Program Loading From a Local EEPROM, Master Mode
- Serial Peripheral Interface (SPI) Circuitry Allows Control Through the Local Microprocessor, Slave Mode
- PCMCIA to I/O Peripheral
- PCMCIA to ATA/IDE Translation
- ATA/IDE to ATA/IDF Mapping, Pass Through Mode
- Operates from a 3 V to 5.5V Power Supply
- Conforms to PCMCIA Standards
- Low Power Dissipation:
  - 12 mW @ 3V
  - 25 mW @ 5V
  - 250 mW @ 5V (in power down mode)
- 100-Pin Low Profile VQFP Package
- Advanced 1.2 Micron CMOS Process

General Description

The Z86017 is a general-purpose PCMCIA adaptor chip used on the card side of the interface. The Z86017 easily configures to all types of memory and I/0 mapped peripheral hardware. Mapping is performed from the I/O and Memory mapped PCMCIA to local peripheral ICs that support Ethernet controllers, UARTs,

modems, printer ports, solid state memory, rotating disk memory, and other peripheral devices.

The Z86017 can be used in a stand-alone configuration without the use of a local processor by providing all of the attribute memory, CCRs, range, interrupt types through a serial EEPROM. The serial EEPROM is read automatically using an internal EEPROM sequencer. The Z86017 can also be configured through a local processor for use on intelligent controller systems.

Power connections follow conventional descriptions below:

Table 1. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

The Z86017 provides for the PCMCIA to IDE translation, IDE to IDE mapping, or PCMCIA to three general-purpose maps (Figure 1).

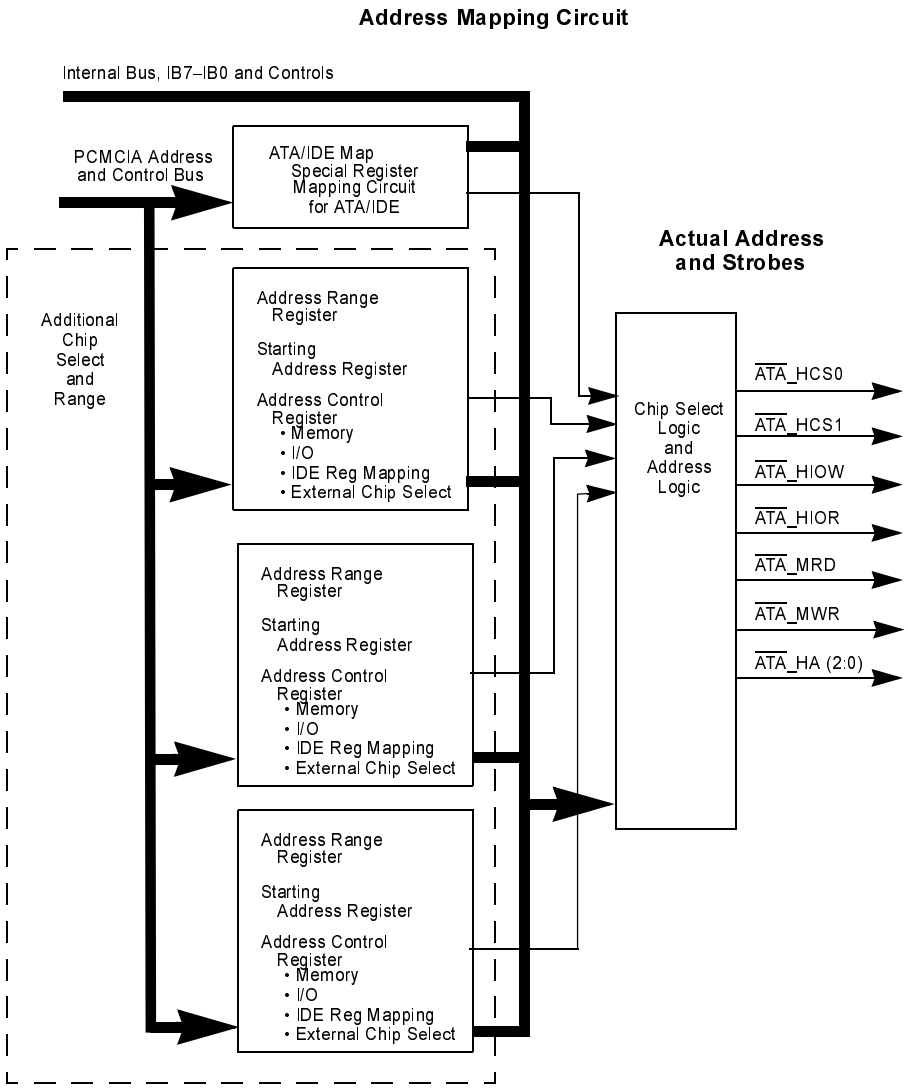

Figure 1. Z86017 Functional Block Diagram

The local processor connects to the Z86017 through the serial interface or can be programmed through an external EEPROM (Figure 2). If the external EEPROM does not have the valid signature inside, the Z86017 acknowledges all selects on the PCMCIA interface.

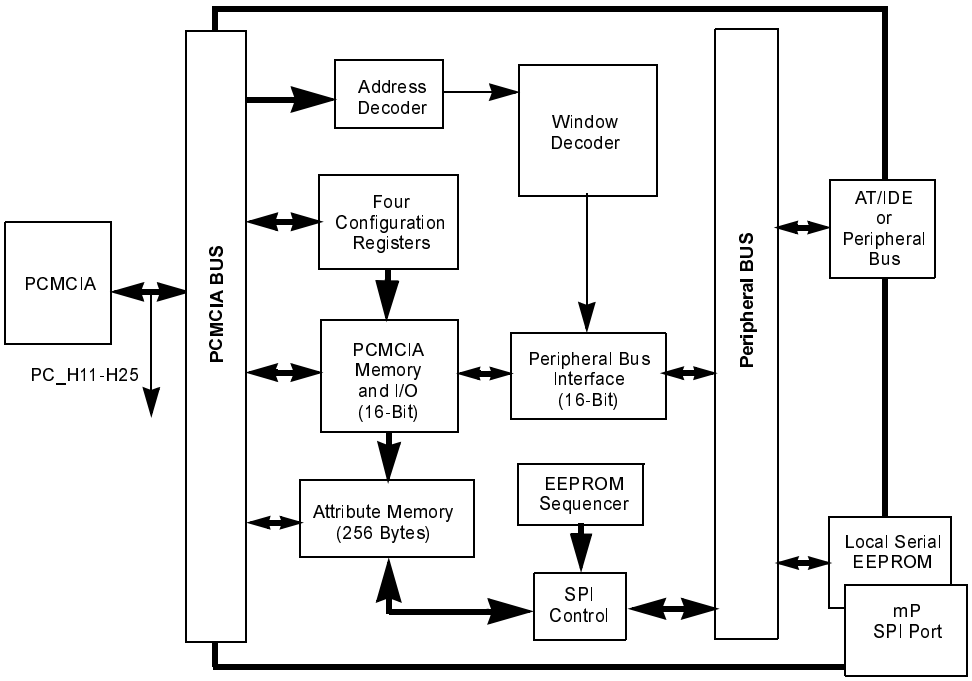

Figure 2. Connection Block Diagram

The Z86017 IC can become an EEPROM interface master or a local processor slave. There are two independent sequencer circuits in the IC to provide for the master and slave operation (Figure 3).

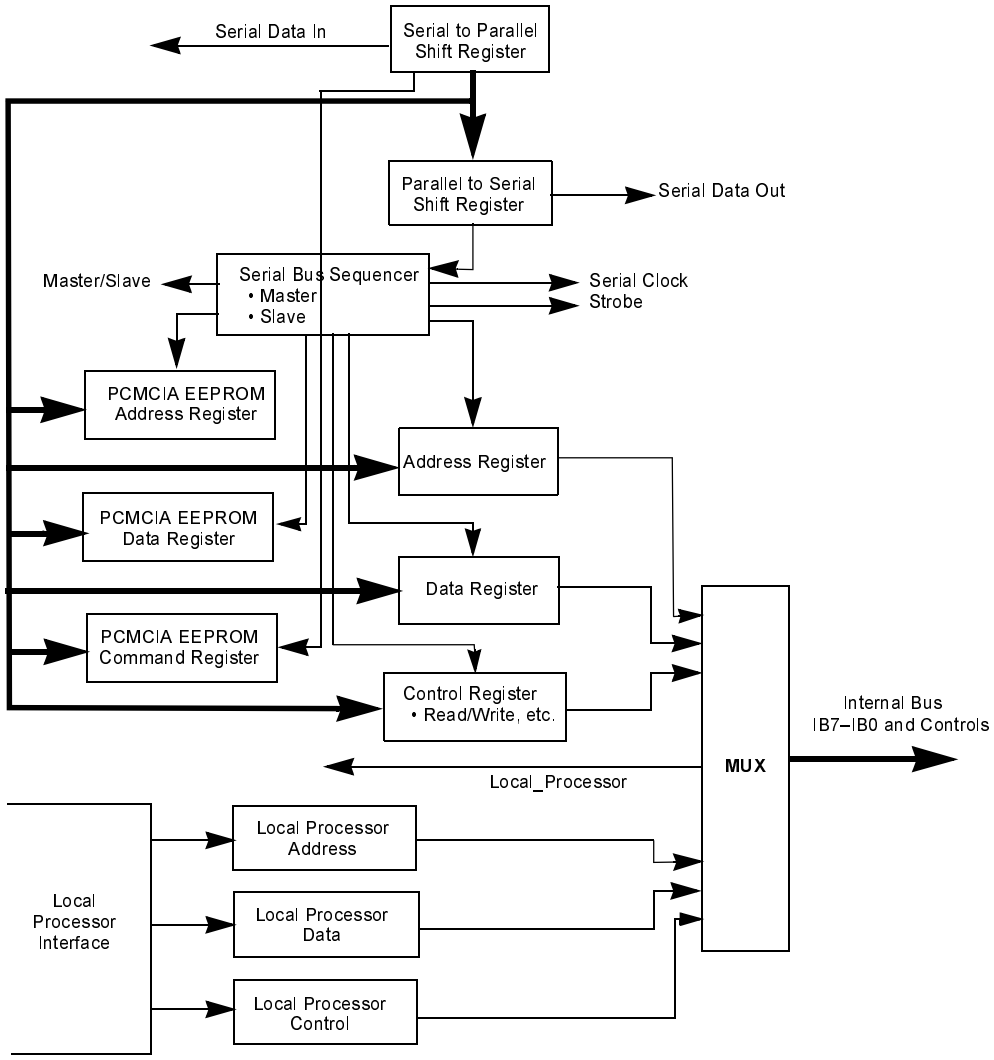

Figure 3. Serial Interface Diagram

The Z86017 IC provides the five standard PCMCIA registers. Three additional registers have been added to provide for remote programming of the EEPROM (Figure 4).

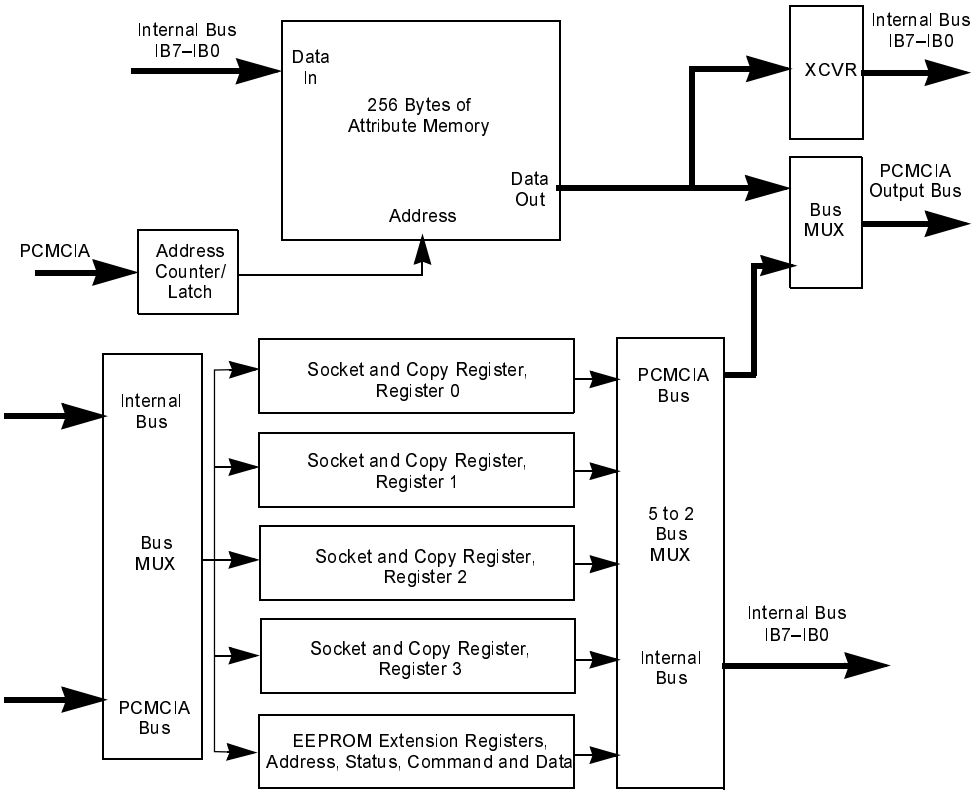

Figure 4. Attribute and Configuration Memory Diagram

Pin Description

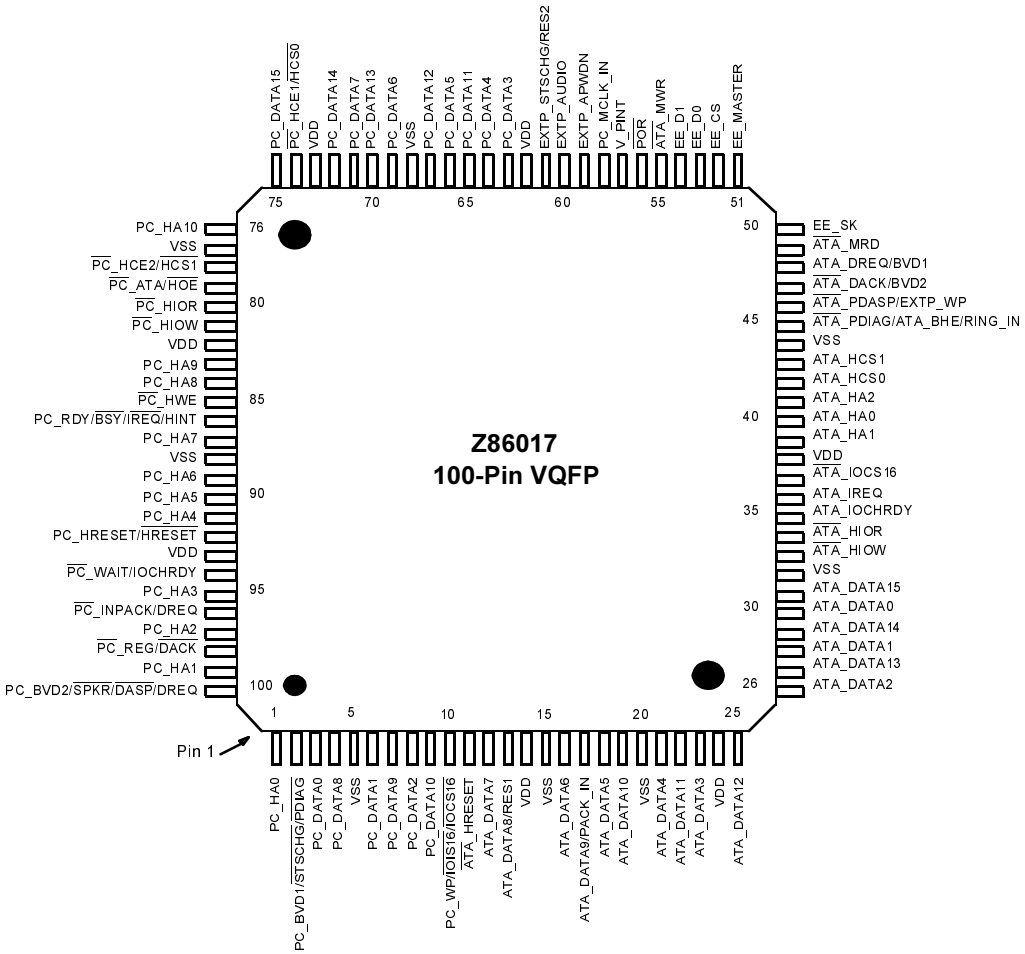

Figure 5. Z86017 100-Pin VQFP Package

Pin Identification

Table 2. Pin Identification

Pin No.	Name	Description
1	PC _HA0	PCMCIA Address, Bit 0
2	$\overline{\text{PC}}$_STSCHG/BVD1/$\overline{\text{PDIAG}}$	PCMCIA Status Change or BVD1 or ATA PDIAG Bit
3	PC _DATAO	PCMCIA Data, Bit 0
4	PC _DATA8	PCMCIA Data, Bit 8
5	VSS	Ground
6	PC_DATA1	PCMCIA Data, Bit 1
7	PC_DATA9	PCMCIA Data, Bit 9
8	PC _DATA2	PCMCIA Data, Bit 2
9	PC _DATA10	PCMCIA Data, Bit 10
10	PC_WP/$\overline{\text{IOIS16}}$/$\overline{\text{IOCS16}}$	PCMCIA I/O Is 16-Bit Transfers or WRITE PROTECT
11	$\overline{\text{ATA}}$_HRESET	AT Host RESET
12	ATA_DATA7	AT Host Data, Bit 7
13	ATA_DATA8/RES 1	AT Host Data, Bit 8 or Reserved Bit 1 in I/O CCR4
14	VDD	Supply Voltage
15	VSS	Ground
16	ATA_DATA6	AT Host Data, Bit 6
17	ATA_DATA9	AT Host Data, Bit 9 or Packet into CCR4
18	ATA DATA5	AT Host Data, Bit 5
19	ATA-DATA10	AT Host Data, Bit 10
20	VSS	Ground
21	ATA_DATA4	AT Host Data, Bit 4
22	ATA_DATA11	AT Host Data, Bit 11
23	ATA_DATA3	AT Host Data, Bit 3
24	VDD	Supply Voltage
25	ATA-DATA12	AT Host Data, Bit 12
26	ATA DATA2	AT Host Data, Bit 2

Table 2. Pin Identification (Continued)

Pin No.	Name	Description
27	ATA-DATA13	AT Host Data, Bit 13
28	ATA DATA1	AT Host Data, Bit 1
29	ATA-DATA14	AT Host Data, Bit 14
30	ATA_DATA0	AT Host Data, Bit 0
31	ATA-DATA15	AT Host Data, Bit 15
32	VSS	Ground
33	$\overline{\text{ATA}}$_HIOW	AT Host I/O Write Strobe
34	$\overline{\text{ATA}}$_HIOR	AT Host I/O Read Strobe
35	ATA_IOCHRDY	AT Host I/O Channel Ready
36	ATA_IREQ	AT Host Interrupt Request
37	$\overline{\text{ATA}}$_IOIS16	AT Host I/O Is 16 Bits Wide
38	VDD	Supply Voltage
39	ATA_HA1	AT Host Address, Bit 1
40	ATA_HA0	AT Host Address, Bit 0
41	ATA_HA2	AT Host Address, Bit 2
42	ATA_HCS0	AT Host Chip Select 0
43	ATA_HCS1	AT Host Chip Select 1
44	VSS	Ground
45	$\overline{\text{ATA}}$_PDIAG/ATA_BHE/Ring-in	PDIAG I/O or Byte High Enable or Ring-in to CCR4
46	$\overline{\text{ATA}}$_PDASP/EXTP_WP	PDASP I/O or Write Protect In
47	$\overline{\text{ATA}}$_DACK/BVD2	AT Host DMA Acknowledge or BVD2 input
48	ATA_DREQ	AT Host DMA Request
49	$\overline{\text{ATA}}$_MRD	AT Host Memory Read Strobe
50	EE-SK_EPROM	Data Clock
51	EE-MASTER	EEPROM Is Master
52	EE-CS	EPROM Data Chip Select
53	EE-DO	EPROM Data Out
54	EE-DI	EPROM Data In
55	$\overline{\text{ATA}}$_MWR	AT Host Memory Write Strobe

Table 2. Pin Identification (Continued)

Pin No.	Name	Description
56	POR	Power-On Reset
57	M_PINT	Local Processor Interrupt
58	PC_MCLK_IN	Master Clock In
59	EXTP_PWDN	Power Down Output
60	EXTP_AUDIO	Audio Input
61	EXTP_STSCHG	Status Change Input
62	VDD	Supply Voltage
63	PC_DATA3	PCMCIA Data, Bit 3
64	PC_DATA4	PCMCIA Data, Bit 4
65	PC_DATA11	PCMCIA Data, Bit 11
66	PC_DATA5	PCMCIA Data, Bit 5
67	PC-DATA12	PCMCIA Data, Bit 12
68	VSS	Ground
69	PC_DATA6	PCMCIA Data, Bit 6
70	PC_DATA13	PCMCIA Data, Bit 13
71	PC_DATA7	PCMCIA Data, Bit 7
72	PC-DATA14	PCMCIA Data, Bit 14
73	VDD	Supply Voltage
74	$\overline{\text{PC}}$_HCE1/HCS0	PCMCIA Chip Select 0
75	PC-DATA15	PCMCIA Data, Bit 15
76	PC-HA10	PCMCIA Address, Bit 10
77	VSS	Ground
78	$\overline{\text{PC}}$_HCE2/HCS1	PCMCIA Chip Select 1
79	$\overline{\text{PC}}$_ATA/$\overline{\text{HOE}}$	PCMCIA Output Enable
80	$\overline{\text{PC}}$_HIOR	PCMCIA I/O Read Strobe
81	$\overline{\text{PC}}$_HIOW	PCMCIA I/O Write Strobe
82	VDD	Supply Voltage
83	PC_HA9	PCMCIA Address, Bit 9
84	PC_HA8	PCMCIA Address, Bit 8
85	$\overline{\text{PC}}$_HWE	PCMCIA WRITE Strobe

Table 2. Pin Identification (Continued)

Pin No.	Name	Description
86	PC_RDY/$\overline{\text{BSY}}$HI$\overline{\text{REQ}}$/HINT	PCMCIA Interrupt Request or PCMCIA Ready/$\overline{\text{Busy}}$
87	PC_HA7	PCMCIA Address, Bit 7
88	VSS	Ground
89	PC_HA6	PCMCIA Address, Bit 6
90	PC_HA5	PCMCIA Address, Bit 5
91	PC_HA4	PCMCIA Address, Bit 4
92	PC_HRESET/$\overline{\text{HRESET}}$	PCMCIA Reset
93	V_{DD}	Supply Voltage
94	$\overline{\text{PC}}$_WAIT/$\overline{\text{IOCHRDY}}$	PCMCIA I/O Channel Ready
95	PC_HA3	PCMCIA Address, Bit 3
96	$\overline{\text{PC}}$_INPACK/DREQ	PCMCIA Input Acknowledge
97	PC_HA2	PCMCIA Address, Bit 2
98	$\overline{\text{PC}}$_REG/$\overline{\text{DACK}}$	PCMCIA Register Signal
99	PC_HA1	PCMCIA Address, Bit 1
100	PC_SPKR/$\overline{\text{DASP}}$/DREQ	IDE DASP Pin or PCMCIA Speaker

Pin Functions

- $\overline{\text{PC}}$_HCE1/$\overline{\text{HCS0}}$, (*Input, Schmitt-Triggered, 100 kΩ Pull-Up*):
  - PCMCIA Mode: Host Card Enable 1 (active Low). Enables even or odd numbered data bytes onto the “PC-DATA (7-0)” Bus.
    ATA Mode: Host Chip Select 0 (active Low).
- $\overline{\text{PC}}$_HCE2/$\overline{\text{HCS1}}$, *(Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  - PCMCIA Mode: Host Card Enable 2 (active Low). Enables odd numbered data bytes onto the “PC-DATA (15-8)” Bus.
    ATA Mode: Host Chip Select 1 (active Low).
- PC-HA (10-3)*(Input, Schmitt-Triggered)*:
  - PCMCIA Mode: Host Address Lines, Bits 10-3.
    ATA Mode: Not used.

- PC-HA (2-0)*(Input, Schmitt-Triggered)*:
  - PCMCIA Mode: Host address Lines, Bits 2-0.
    ATA Mode: Host address Lines, Bits 2-0.
- $\overline{\text{PC}}$_SPKRUDASP/DREQ (*Input/Output, Tri-Stated, SmA)*:
  - PCMCIA Mode: Speaker Output (active Low). This signal is the opposite polarity of the “EXTP_AUDIO” input signal and the extended special function bus in PCMCIA Mode. If configured in the general-purpose address recognition registers, this signal is DMA request, active Low, when ATA_DREQ is asserted active High.
    ATA Mode: Slave present bit when in ATA mode or when enabled in PCMCIA mode.
- $\overline{\text{PC}}$_HIOR *(Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  - PCMCIA Mode: Host Input/Output Read Strobe (active Low). In PCMCIA I/O Mode, this is the Input/Output Read Strobe.
    ATA Mode: Input/Output Read Strobe (active Low).
- $\overline{\text{PC}}$_HIOW (*Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  - PCMCIA Mode: Host Input/Output Write Strobe (active Low). Mode, this is the Input/ Output Write Strobe.
    ATA Mode: Input/Output Write Strobe (active Low).
- PC_RDY/BSY/$\overline{\text{IREQ}}$/HINT *(Output, 8mA)*:
  - PCMCIA Mode: Ready/Busy (active High) or /IREQ (active Low). In PCMCIA Common Memory Mode, this signal is Ready/Busy. This signal is asserted BUSY by the Reset logic. In PCMCIA I/O Mode, this signal is /IREQ.
    ATA Mode: Host Interrupt (active High). This signal sends an interrupt to the host when enabled.
- PC_WP/$\overline{\text{IOIS16}}$/$\overline{\text{IOCS16}}$(*Output, Tri-Stated, 8mA)*:
  - PCMCIA Mode: Write Protect (active High) or I/O is 16 bits (active Low). In PCMCIA Common Memory Mode, this signal is write protect. In PCMCIA I/O Mode, this signal is I/O and 16 bits. This signal indicates a 16-bit data transfer is active on the PCMCIA Bus.
    ATA Mode: I/O Chip Select 16 bits (active Low). Indicates a 16-bit transfer is active on the bus.
- PC_WAIT/AOCHRDYAOCHRDY(*Output, Tri-State, 8mA)*:
  - PCMCIA Mode: Wait (active High). Inserts wait states when held active and the chip is being selected in I/O or Memory Mode.
    ATA Mode: Wait (active High). Inserts wait states when held active and the chip is being selected.

- PC_HRESET/HRESET *(Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  - PCMCIA Mode: Host Reset (active High). Host input reset signal.
    ATA Mode: Host Reset (active Low). Host input reset signal.
- $\overline{\text{PC}}$_INPACK/DREQ *(Output, Tri-Stated, 8 mA*):
  - PCMCIA Mode: Input Acknowledge (active Low). This signal is asserted by the peripheral to drive data and/or command/status on the data bus when the chip is selected.
    ATA Mode: Data request (active High). This signal is issued during DMA data transfers on the data bus as defined in ATA.
- $\overline{\text{PC}}$_REG/$\overline{\text{DACK}}$ *(Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  - PCMCIA Mode:Register Bit (active Low). This signal is asserted when the host selects I/O Memory or Attribute Memory.
    ATA Mode: Data Acknowledge (active Low). This signal is issued during DMA data transfers on the data bus as defined in ATA.
- $\overline{\text{PC}}$_STSCHG/$\overline{\text{PDIAG}}$*(Input/Output, 8 mA)*:
  - PCMCIA Mode: Status Change (active Low). This signal is used to indicate changes in the Card Configuration Registers.
    ATA Mode: Passed diagnostics (active Low).
- $\overline{\text{PC}}$_ATA/$\overline{\text{OE}}$ *(Input, Schmitt-Triggered,100 kΩ Pull-Down)*:
  - PCMCIA Mode: Output Enable (active Low).
    ATA Mode: AT Mode (active Low). This signal indicates AT Mode when pulled Low on a Power-On Reset.
- $\overline{\text{PC}}$-WE *(Input, Schmitt-Triggered, 100 kit Pull-Up)*:
  - PCMCIA Mode: Write enable (active Low).
    ATA Mode. Not used.
- PC DATA (15-0) *(Input/Output, Tri-Stated, 8 mA)*:
  - PCMCIA Mode:Host Data Lines, 16 bits.
    ATA Mode:Host Data Lines, 16 bits.
- /POR *(Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  Power-On Reset (active Low). Local power on reset signal.
- EE_DO (Output, 2mA):
  EEPROM Data Out (active High). This signal indicates serial data is valid during “EE_SK” edge. In Master Mode or Slave Mode, this signal is an output.
- EE-SK *(Input/Output, 2 mA)*:
  EEPROM Data Clock (active High). This signal is an output in Master Mode. In Slave Mode, this signal is an input.

- EE-CS *(Input/output, 2 mA)*:
  EPROM Data Chip Select (active High). This signal is an output in Master Mode. In Slave Mode, this signal is an input.
- EE_DI *(Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  EPROM Data Input (active High). This signal is an input in Master Mode or Slave Mode.
- PC_MCLK_IN *Input, Schmitt-Triggered)*:
  Master Clock Input. This is the input clock signal used to generate all internal timing when reading the EEPROM using the internal EEPROM sequencer. It is also used to generate internal timing for Ready.
- EXTP_STSCHG *(Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  Status Change Input (active High). This signal outputs the value of the status changed line on the PCMCIA bus if enabled in the CCR Register.
- EXTP_AUDIO (*Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  Audio Input (active High). This signal is the input signal which reflects the audio output. This signal is active High, whereas the Speaker Output on the PCMCIA Bus is active Low.
- EXTP_PWDN *(Output, 2 mA)*:
  Power Down Output (active High). This signal reflects the state of the Power Down Bit in the CCR.
- $\overline{\text{ATA}}$_MRD *(Output, 2mA)*:
  External Memory Read Strobe (active Low).
- $\overline{\text{ATA}}$_MWR *(Output, 2 mA)*:
  External Memory Write Strobe (active Low).
- $\overline{\text{ATA}}$_PDASP/EXTP_WP *(Input/Output, Tri-Stated, 2 mA)*:
  Local AT bus side PDASP signal controlled by internal bits ZEN_EXT_PDASP (Input) or ZEN _INPUTT_PDASP (Output). When configured as write protect, this signal stops all Write Strobes on the local AT Bus.
- $\overline{\text{ATA}}$_PDIAG/$\overline{\text{ATA}}$_BHE *(Input/Output, Tri-Stated, 2 mA)*:
  Local AT bus side PDIAG signal controlled by internal bits ZEN_EXT_PDIAG (Input) or ZEN_INPUTT_PDIAG (Output). When configured as High Byte Enable for memory boards, “ATA_BHE” indicates a High Byte available or High Byte requested on the Local AT Bus.
- ATA_IOCHRDY *(Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  I/O Channel Ready (active High). This input signal indicates the I/O Channel on the Local AT Bus is ready.
- $\overline{\text{ATA}}$_IOIS16 *(Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  I/O Channel is 16 bits (active Low). This input signal indicates the I/O Channel on the Local AT bus is 16 bits wide.

- EE-MASTER *(Input, Schmitt-Triggered, 100 kΩ Pull-Up)*:
  EEPROM Master Interface Enabled (active High). When this input is set High, an EEPROM is present. When this signal is set Low, no EEPROM is present.
- $\overline{\text{ATA}}$_HCSO *(Output, 2 mA)*:
  IDE/ATA Mode: AT Host Chip Select 0 (active Low). This signal is used to select the IDE interface chip as standard IDE format.
  Local Bus Mode: Chip Select 0 (active Low). This signal is used to connect as a chip select for an external peripheral device as defined by the address range and offset register definition.
- $\overline{\text{ATA}}$_HCS1 *(Output, 2 mA)*:
  IDE/ATA Mode: AT Host Chip Select 1 (active Low). This signal is used to select the IDE interface chip as standard IDE format.
  Local Bus Mode: Chip Select 1 (active Low). This signal is used to connect as a chip select for an external peripheral device as defined by the address range and offset register definition.
- ATA_HA (2-0) (*Output, 2 mA)*:
  IDE/ATA Mode: AT Host Address Lines, Bits 2-0. These lines are used to address the IDE interface chip task register file as standard IDE format.
  Local Bus Mode: Address Lines, Bits 2-0. These lower three bits offset from starting address.
- ATA_IREQ *(Input, Schmitt-Triggered)*:
  IDE/ATA Mode: AT Host Interrupt Request (active High).
  Local Bus Mode: Interrupt Request (active High).
- $\overline{\text{ATA}}$_HIOR *(Output, 2mA)*:
  IDE/ATA Mode: AT Host I/O Read Strobe (active Low).
  Local Bus Mode: I/O Read Strobe or Memory Read Strobe or Data Strobe (active Low). The function of this signal depends on the configuration.
- $\overline{\text{ATA}}$_HIOW (*Output, 2 mA)*:
  IDE/ATA Mode: AT Host I/O Write Strobe (active Low).
  Local Bus Mode: I/O Write Strobe or Memory Write Strobe or Read/Write Data Enable (active Low).The function of this signal depends on the configuration.
- $\overline{\text{ATA}}$_HRESET*(Output, 2 mA)*:
  IDE/ATA Mode: AT Host Reset (active High or Low). This signal is the reset output to the IDE controller.
  Local Bus Mode: AT Host Reset (active High or Low). This signal is the reset output to the peripheral device if PCMCIA signal is active.
- ATA_DATA (15-0)(*Input/Output, Tri-Stated, 2 mA)*:
  IDE/ATA Mode: Host Data Bus, Bits 15-0.
  Local Bus Mode: Peripheral Data Bus, Bits 15-0.

- ATA_DREQ/BVD1 *(Input, Schmitt-Triggered)*:
  IDE/ATA Mode:AT Host DMA Request (active High).
  Local Bus Mode: Peripheral Bus DMA Request (active High). When PCMCIA is connected, this signal is asserted through the “PC SPKR” pin on the PCMCIA interface.
- $\overline{\text{ATA\_DACK}}$/BVD2 *(Output, 2 mA)*:
  IDE/ATA Mode:AT Host DMA Acknowledge (active Low).
  Local Bus Mode: Peripheral Bus DMA Acknowledge (active Low). DMA acknowledge is generated by Z86017 whenever DMA acknowledge is configured in the PCMCIA address registers and the address corresponds to the DMA address.
- M_PINT *(Output, Tri-stated)*:
  Microprocessor Interrupt (active High). This signal is the interrupt to local microprocessor.
- V_{SS} *(Input)*:
  Digital Ground
- V_{DD}*(Input)*:
  Digital Supply Voltage

Absolute Maximum Ratings

Table 3. Absolute Maximum Rating

Symbol	Description	Min	Max	Unit
VCC	Supply Voltage[1]	-0.3	+7.0	V
TSTG	Storage Temperature	-65	+150	C
TA	Operating Ambient Temperature	Note[2]	Note[2]	C

1. Voltages on all pins with respect to GND.
2. See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted (Test Load Diagram).

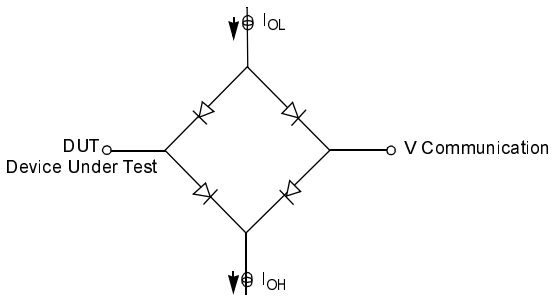

Figure 6. Test Load Diagram

DC Specifications

Table 4. Absolute Rating Limits

Parameter	Symbol	Unit	Min Value	Max Value
Supply Voltage	V_{DD}	(V)	-0.5	7.0
Input Voltage	V_i	(V)	-0.5	V_{DD} + 0.5
Output Voltage	V_o	(V)	-0.5	V_{DD} + 0.5
Storage Temperature	T_{stg}	(C)	-40	+125
Temperature Under Bias	T_{bias}	(C)	-25	+85

Table 5. 3-Volt Operating Conditions

Parameter	Symbol	Unit	Min Value	Max Value
Supply Voltage	V_{DD}	(V)	3.0	5.5
Input High Voltage for TTL Inputs	V_{IH}	(V)	2.4	V_{DD}
Input Low Voltage for TTL Inputs	V_{IL}	(V)	-0.5	0.6
Operating Temperature	T_a	(C)	0	70

Table 6. 5-Volt Operating Conditions

Parameter	Symbol	Unit	Min Value	Max Value
Supply Voltage	V_{DD}	(V)	4.5	5.5
Input High Voltage for TTL Inputs	V_{IH}	(V)	2.4	V_{DD}
Input Low Voltage for TTL Inputs	V_{IL}	(V)	-0.5	0.8
Operating Temperature	T_a	(C)	0	70

DC Electrical Characteristics

Table 7. DC Electrical Characteristics

Parameter	Symbol	Unit	Min Value	Max Value
Power Supply Current	I_{DDS}[1]	(mA)		5 (5V) 4 (3V)
Output High Voltage	V_{OH} (I_{OH} = -2mA)	(V)	2.4	V_{DD}
Output Low Voltage	V_{OL} I_{OL} = 2 mA	(V)		0.4
Input Leakage Current	I_L $V_i \le V_{DD}$	(mA)	-10	10
Power Dissipation	Pmax	mW µW		25 (5V) 12 (3V) 250 µW (Power down mode)
Input Capacitance	C_i	(pf)		8 pf

1. I_{DDS} is specified at 1 MHz on PCMCLKIN and V_{DD} on EESK

Internal Attribute Memory Timing

Table 8. Internal Attribute Memory Timing

Item	Symbol	Min	Max	Units
Read Cycle Time	tc(R)	300		nS
Address Access Time	ta(A)		300	nS
Card Enable Time	ta(CE)		300	nS
Output Enable Access Time	ta(OE)		150	nS
Output Disable Time from CE	tdis(CE)		100	nS
Output disable time from OE	tdis(OE)		100	nS
Output enable time from CE	ten CE)	5		nS
Output enable time from OE	ten(OE)	5		nS
Data Valid from ADD Change	tv(A)	0		nS
Address Setup Time	Tsu(A)	30		nS
Address Hold Time	th(A)	20		nS
Card Enable Setup Time	tsu(CE)	0		nS
Card Enable Hold Time	th(CE)	20		nS
Wait Valid from OE	tv(WT-OE)		35	nS
Wait Pulse Width	tw(WT)		12	µS
Data Setup for wait Released	tv(WT)	0		nS

Table 9. PCMCIA Memory Write and Read Timing

		200nS		150 nS		100 nS	
Speed Version	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Write Cycle Time	tc(W)	200		150		100	
Write Pulse Width	tw(WE)	120		80		60	
Address Setup Time	tsu(A)	20		20		10	
Address Setup Time for WE	tsu(A-WEH)	140		100		70	
Card Enable Setup Time for WE	tsu(CE-WEH)	140		100		70	

Table 9. PCMCIA Memory Write and Read Timing (Continued)

		200nS		150 nS		100 nS	
Speed Version	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Data Setup Time for WE	tsu (D-WEH)	60		50		40	
Data Hold Time	th(D)	30		20		15	
Write Recover Time	trec(WE)	30		20		15	
Output Disable Time from WE	tdis(WE)		90		75		50
Output Disable Time from OE	tdis(OE)		90		75		50
Output Setup from WE	ten(WE)	5		5		5	
Output Enable Setup from WE	tsu(OE-WE)	10		10		10	
Card Enable Hold from WE	th(OE-WE)	10		10		10	
Card Enable Setup Time	tsu(OE-WE)	0		0		0	
Card Enable Hold Time	th(CE)	20		20		15	
Wait Valid from WE	tv(WT-WE)		35		35		35
Wait Pulse Width	tw(WT)		12us		12μS		12 μS
WE high from Wait Released	tv(WT)	0		0		0	

Table 10. I/O Read Timing Specification

Item	Symbol	Min	Max	Units
Data Delay after IORD	td(IORD)		100	nS
Data Hold following IORD	th(IORD)	0		nS
LORD Width Time	tw(IORD)	165		nS
Address Setup before IORD	tsuA(IORD)	70		nS
Address Hold Following IORD	thA(IORD)	20		nS
CE Setup before IORD	tsuCE(IORD)	5		nS
CE Hold Following IORD	thCE(IORD)	20		nS
REG Setup before IORD	tsuREG(IORD)	5		nS

Table 10. I/O Read Timing Specification (Continued)

Item	Symbol	Min	Max	Units
REG hold following IORD	thREG(IORD)	0		nS
INPACK Delay to IORD	tdINPACK(IORD	0	45	nS
INPACK Delay from IORD	tdINPACK(IORD)		45	nS
10IS16 Delay from Address	tdIOIS16(ADR)		35	nS
10IS16 Delay Rise From Address	tdIOIS16(ADR)		35	nS
Wait Delay from IORD	tdWAIT(IORD)		35	nS
Data Delay from Wait Rising	td W Ty		35	nS
Wait Width Time	tw WT		12	µS

Table 11. I/O Write Timing Specification

Item	Symbol	Min	Max	Units
Data Setup before IOWR	tsu(IOWR)	60		nS
Data Hold after IOWR	th(IOWR)	30		nS
IOWR Width Time	tw(IOWR)	165		nS
Address setup to IOWR	tsuA(IOWR)	70		nS
Address Hold after IOWR	thA(IOWR)	20		nS
CE setup before IOWR	tsuCE(IOWR)	5		nS
CE hold after IOWR	thCE(IOWR)	20		nS
REG Setup before IOWR	tsuREG(IOWR)	5		nS
REG hold after IOWR	thREG(IOWR)	0		nS
10IS16 Delay falling from Address	tdIOIS16(ADR)		35	nS
IOIS16 delay Rising from Address	tIdIOIS16(ADR)		35	nS
Wait Delay Falling from IOWR	tdWAIT(IOWR)		35	nS
Wait Width Timing	twWAIT		12	µS