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ZiLOG

Totally Logical

Z86129/130/131

NTSC LINE 21 DECODER

FEATURES

Devices	Speed (MHz)	Pin Count/ Package Types	Standard Temp. Range	On-Screen Display & Closed Captioning	Automatic Data Extraction V-Chip	Automatic Data Extraction Time of Day
Z86129	12	18-Pin DIP, SOIC	0° to +70°C	Yes	Yes	Yes
Z86130	12	18-Pin DIP, SOIC	0° to +70°C	No	Yes*	Yes*
Z86131	12	18-Pin DIP, SOIC	0° to +70°C	No	No	Yes

Note: *The Z86130 recovers the line 21 data in both of field1 and field2. It also has V-Chip-specific registers and the output (pin-13) to control program blocking with minimal communications between the Z86130 and the host processor.

- Complete Stand-Alone Line 21 Decoder for Closed-Captions and Extended Data Services (XDS).
- Preprogrammed to Provide Full Compliance with EIA–608 Specifications for Extended Data Services.
- Automatic Extraction and Serial Output of Special XDS Packets such as Time of Day, Local Time Zone, and Program Blocking *(V-Chip)*.
- Cost-Effective Solution for NTSC Violence Blocking inside Picture-in-Picture (PiP) Windows.
- Minimal Communications and Control Overhead Provides Simple Implementation of Violence Blocking, Closed Captioning, and Auto Clock Set Features.
- Programmable, Full Screen On-Screen Display (OSD) for Creating OSD or Captions inside a Picture-in-Picture (PiP) Window (Z86129 only).
- I^2C Serial Data and Control Communication
- User-Programmable Horizontal Display Position for easy OSD Centering and Adjustment (Z86129 only).

GENERAL DESCRIPTION

The Z86129/130/131 is a stand-alone integrated circuit, capable of processing Vertical Blanking Interval (VBI) data from both fields of the video frame in data conforming to the transmission format defined in the Television Decoder Circuits Act of 1990 and in accordance with the Electronics Industry Association specification 608 (EIA–608).

The Line 21 data stream can consist of data from several data channels multiplexed together. Field 1 has four data channels: two Captions and two Text. Field 2 has five additional data channels: two Captions, two Text and Extended Data Services (XDS). XDS data structure is defined in EIA–608. The Z86129 can recover and display data transmitted on any of these nine data channels. The Z86130 and Z86131 are derivatives of the Z86129. The Z86130 and Z86131 do not have OSD capability, but are ideally suited for Line 21 data slicer applications.

The Z86129/130/131 can recover and output to a host processor via the I^2C serial bus the recovered XDS data packet defined in EIA–608 as it is defined in the table above (Z86130 provides the raw Line 21 data, which must be decoded properly for the applications). On-chip XDS filters in Z86129 is fully programmable, enabling recovery of only those XDS data packets selected by the user.The Z86131 is designed especially for extracting XDS time information with proper XDS filter setup for Automatic Clock-Set features in TVs, VCRs, and Set-Top boxes. And the Z86130 is designed especially for V-Chip and Line 21 data recovery.

In addition, the Z86129/130 is ideally suited to monitor Line 21 of video displayed in a PiP window for violence blocking purposes. A block diagram of the Z86129/130/131 is illustrated in Figures 1 and 2.

GENERAL DESCRIPTION (Continued)

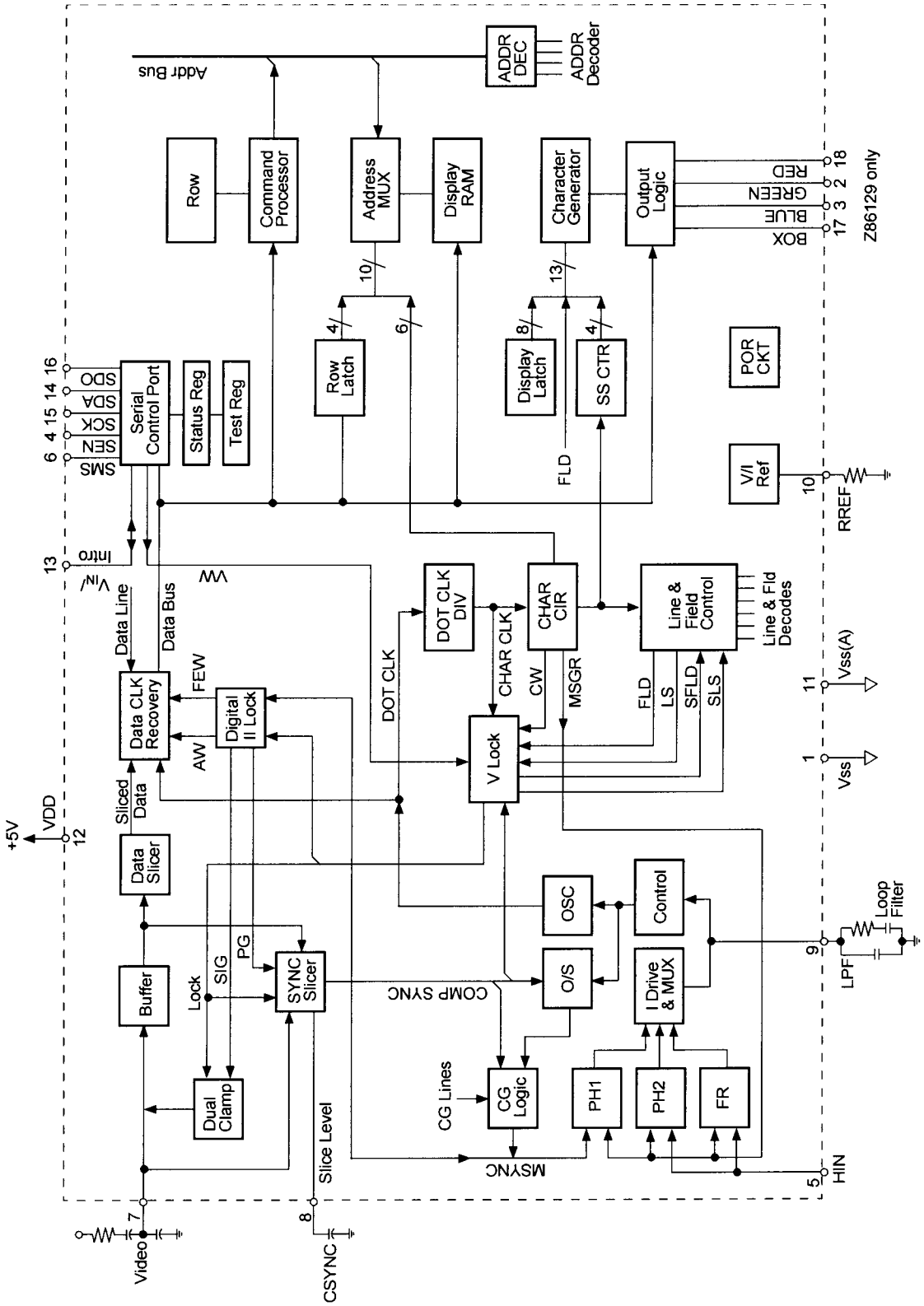

Figure 1. Z86129 Block Diagram

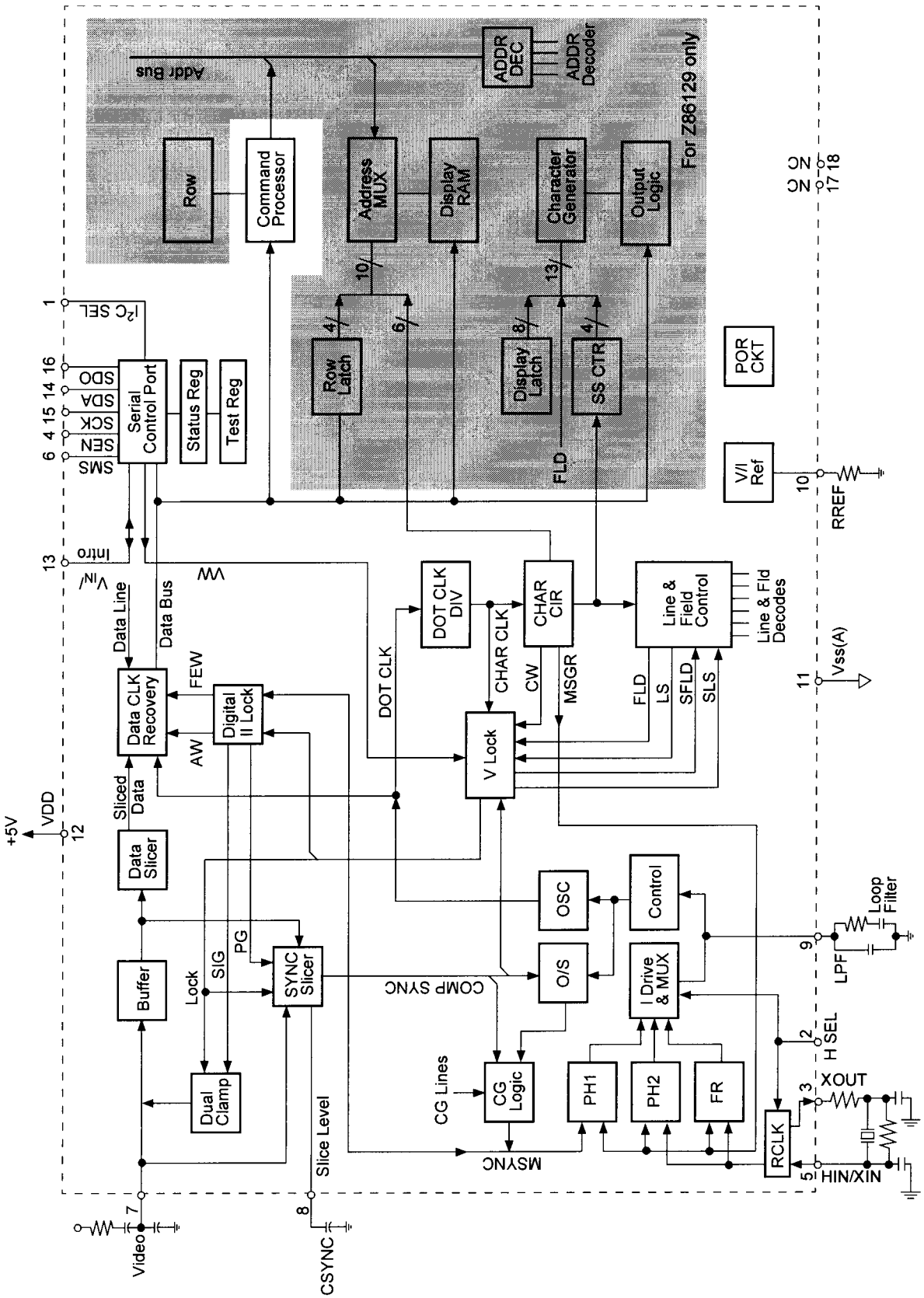

Figure 2. Z86130/131 Block Diagram

PIN DESCRIPTION

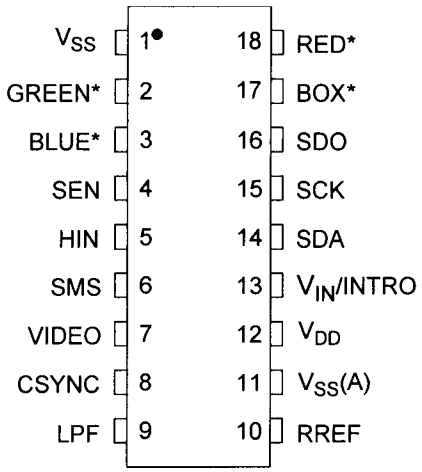

Figure 3. Z86129, 18-Pin DIP/SOIC Pin Configuration

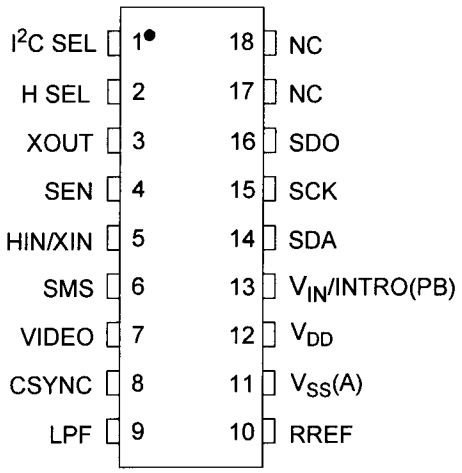

Figure 4. Z86130/131, 18-Pin DIP/SOIC Pin Configuration

Table 1. Z86129 Pin Identification

No	Symbol	Function	Direction
1	V_{SS}	Power Supply GND	
2*	GREEN	Video Output	Output
3*	BLUE	Video Output	Output
4	SEN	Serial Enable	Input
5	HIN	Horizontal In	Input
6	SMS	Serial Mode Select	Input
7	VIDEO	Composite Video	Input
8	CSYNC	Composite Sync	Output
9	LPF	Loop Filter	Output
10	RREF	Resistor Reference	Input
11	V_{SS}(A)	Pwr. Supply (Analog) GND	
12	V_{DD}	Power Supply	
13	V_{IN}/INTRO	Vertical In/Interrupt Out	In/Output
14	SDA	Serial Data	In/Output
15	SCK	Serial Clock	Input
16	SDO	Serial Data Out	Output
17*	BOX	OSD Timing Signal	Output
18*	RED	Video Output	Output

Note: *DIP and SOIC pin configuration are identical.

Table 2. Z86130/131 Pin Identification

No	Symbol	Function	Direction
1*	I^2C SEL	I^2C Slave Address Select	Input
2	H SEL	HIN/XTAL Select	Input
3	XOUT	XTAL Output	Output
4	SEN	Serial Enable	Input
5	HIN/XIN	Horizontal In/XTAL Input	Input
6	SMS	Serial Mode Select	Input
7	VIDEO	Composite Video	Input
8	CSYNC	Composite Sync	Output
9	LPF	Loop Filter	Output
10	RREF	Resistor Reference	Input
11	$V_{SS\ (A)}$	Pwr. Supply (Analog) GND	
12	V_{DD}	Power Supply	
13**	V_{IN}/INTRO (PB)	Vertical In/Interrupt Out (Program Blocking)	In/Output (Output)
14	SDA	Serial Data	In/Output
15	SCK	Serial Clock	Input
16	SDO	Serial Data Out	Output
17	NC	No Connect	
18	NC	No Connect	

Notes:

*DIP and SOIC pin configuration are identical; must be tied to V_{SS} for current revision. A secondary I^2C address will be available in the future.

**This pin is used as PB (Program Blocking) output in Z86130 to indicate whether the incoming video program is in the blocking set-up programmed.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage**	–0.5 to 6.0	V
V_{IN}	DC Input Voltage**	–0.5 to V_{DD} +0.5	V
V_{OUT}	DC Output Voltage**	–0.5 to V_{DD} +0.5	V
I_{IN}	DC Input Current per Pin	+10	mA
I_{OUT}	DC Output Current per Pin	+20	mA
I_{DD}	DC Supply Current	+30	mA
P_D	Power Dissipation per Device	300	mW
T_{STG}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

Notes:

*Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits specified in the DC and AC Characteristics tables, pages 5 and 6, or the Pin Description section, page 9.

**Voltages referenced to V_{SS}(A) and V_{SS}.

STANDARD TEST CONDITIONS

The characteristics listed in the following section apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (5).

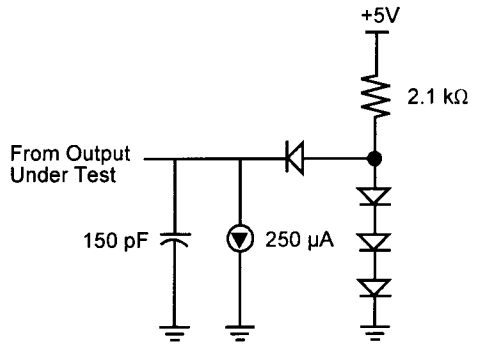

Figure 5. Standard Test Load

DC ELECTRICAL CHARACTERISTICS

Table 3. DC Electrical Characteristics
(T_A = 0°C to +70°C; V_{DD} = +4.75V to +5.25V)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}	Input Voltage Low		0	0.2 V_{DD}	V
V_{IH}	Input Voltage High		0.7 V_{DD}	V_{DD}	V
V_{OL}	Output Voltage Low	I_{OL} = 1.00 mA	–	0.4	V
V_{OH}	Output Voltage High	I_{OH} = 0.75 mA	V_{DD} –0.4V	–	V
I_{IL}	Input Leakage	0V, V_{DD}	–3.0	3.0	µA
I_{DD}	Supply Current	Estimated*		30	mA
Kf	VCO Gain		–	TBD	MHz/V
I_{LP}	Loop Filter Current		–	TBD	mA

Note: *Not guaranteed.

AC AND TIMING CHARACTERISTICS

Table 4. Composite Video Input

Parameter	Conditions
Amplitude	1.0V p-p ±3 dB
Polarity	Sync tips negative
Bandwidth	600 kHz
Signal Type	Interlaced
Max Input R	470 ohms
DC Offset	Signal to be AC coupled with a minimum series capacitance of 0.1 µF

ELECTRICAL CHARACTERISTICS

Nonstandard Video Signals must exhibit the characteristics indicated in Table 5.

Table 5. Characteristics

Parameter	Conditions
Sync Amplitude	200 mV minimum
Vertical Pulse Width	3H ±0.5H
Vertical Pulse Tilt	20 mV maximum
H Timing	Phase Step (Head Switch) ±10 µs maximum Fh Deviation (long term) ±0.5% maximum Fh p-p Deviation (short term) ±0.3% maximum
Vertical Sync Signal	The internal sync circuits lock to all 525 or 625 line signals having a vertical sync pulse that meets the following conditions: • It is at least 2H wide • It starts at the proper 2H boundary for its field • If equalizing pulse serrations are present, they must be less than 0.125H in width.
Minimum Signal-to-Noise	The Z86129/130/131 functions down to a 25 dB signal-to-noise ratio (CCIR-weighted) with one error per row or better at that level.
Ratio to Composite Video	Input

Horizontal Signal Input (preferably H Flyback and refer to 1 and 2 to use external XTAL or clock input for Z86130/131 only)

Table 6. Horizontal Signal Input

Parameter	Conditions	
Amplitude	CMOS level signal where Low <= 0.2 V_{CC}	
Video Lock Mode	Polarity	Any
	Frequency	15,734.263 Hz ±3%
HIN Lock Mode	Polarity	Any
	Frequency	Same as Display Horizontal Flyback Pulse (HFB) pulse

Table 7. XTAL Input on HIN/XIN and XOUT—Z86130/131 Only

Parameter	Conditions
Frequency	32.768 KHz
Frequency tolerance	+/– 20ppm @ Ta=25C, CL=12.5pF
Equivalent XTALs	Epson C–001R 32.768K–A or Fox NC26, NC28

Table 8. Clock Input on HIN/XIN—Z86130/131 Only

Parameter	Conditions
Frequency	32.768 kHz +/– 2%

Line 21 Input Parameters (at 1.0V p-p)

Note: Line 21 must be in its proper position to the leading edge of the Vertical Sync signal.

Table 9. Line Input Parameters

Parameter	Conditions
Cod Amplitude	50 IRE
Code Zero Level	5 IRE, +15 IRE relative to Back Porch
Start of Code	10.5 ±0.5 µs (measured from the midpoint of the falling edge of the most recent clock run-in cycle to the midpoint of the rising edge of the start bit).
Start of Data	3.972 µs, –0.00 µsec, +0.30 µs (measured from the midpoint of the falling edge of the most recent clock run-in cycle to the midpoint of the rising edge of the start bit).

Timing Signals

Table 10. Timing Signals

Parameter	Conditions
Dot	768 x FH = 12.0839 MHz
Dot Period	82.75 ns
Character Cell Width	1.324 µs (tH/48)
Width of Row (Box)	45.018 µs (34 chars = 17/24 x tH
Width of Row (Char)	42.370 µs (32 chars = 2/3 x tH
Horizontal Display Timing	The timing of the output signals Box and RGB have been set to make a centered display. The positioning of these outputs can be adjusted in 330 ns increments by writing a new value to the Z86129 H Position Register (Address = 02h).

PIN DESCRIPTIONS (Z86129 ONLY)

Inputs

VIDEO (Pin 7). Composite NTSC video input, 1.0V p-p (nom), band limited to 600 kHz. The circuit operates with signal variation between 0.7–1.4V p-p. The polarity is sync tips negative. This signal pin should be AC coupled through a 0.1 µF capacitor and driven by a source impedance of 470 ohms or less.

HIN (Pin 5). Horizontal Sync input signal at CMOS level must be supplied. When the device is used in VIDEO LOCK mode, this signal pulls the on-chip VCO within the proper range. The circuit uses the frequency of this signal which must be within ±3% F_h but can be of either polarity. When used in the H LOCK mode, the VCO phase locks to the rising edge of this signal. The HPOL bit of the H Position register can be set to operate with either polarity of input signal (usually the H Flyback signal). The timing difference between HIN rising edge and the leading edge of composite sync (of VIDEO input) is one of the factors which affects the horizontal position of the display. Any shift resulting from the timing of this signal can be compensated for with the horizontal timing value in H Position Register. H LOCK is intended for use when the part is generating an OSD display when no video signal is present.

SMS (Pin 6). Mode select pin for the Serial Control Port. When this input is at a CMOS High state (1) the Serial Control Port operates in the SPI mode. When the input is Low (0), the Serial Control Port operates in the I^2C slave mode. In SPI mode, the SEN pin must be tied High. (See Reset Operation section, below.)

SEN (Pin 4). Enable signal for the SPI mode operation of the Serial Control Port. When this pin is Low (0), the SPI port is disabled and the SDO pin is in the high-impedance state. Transitions on the SCK and SDA pins are ignored. SPI mode operation is enabled when SMS is High (1).

SCK (Pin 15). Input pin for serial clock signal from the master control device. In I^2C mode operation the clock rate is expected to be within I^2C limits. In SPI mode, the maximum clock frequency is 10 MHz.

Reset Operation. When the SMS and SEN pins are both in the Low (0) state, the part is in the Reset state. Therefore, in the I^2C mode the SEN pin can be used as an NReset input. When SPI mode is used, if three wire operation is desired, both SMS and SEN can be tied together and used as the NReset input. In either mode, NReset must be held Low (0) for at least 100 ns.

Input/Output

V_{IN}/INTRO (Pin 13). In external (EXT) vertical lock mode of operation, the internal vertical sync circuits lock to the V_{IN} input signal applied at this pin. The part locks to the rising or falling edge of the signal in accordance with the setting of the V Polarity command. The default is rising edge. The V_{IN} pulse must be at least 2 lines wide.

In INTRO Mode, when configured for internal vertical synchronization, this pin is an output pin providing an interrupt signal to the master control device in accordance with the settings in the Interrupt Mask Register.

SDA (Pin 14). When the Serial Control Port has been set to I^2C mode operation, this pin serves as the bidirectional data line for sending and receiving serial data. In SPI mode operation it operates as serial data input. SPI mode output data is available on the SDO pin.

Outputs

SDO (Pin 16). Provides the serial data output when SPI mode communications have been selected. This pin is not used in I^2C mode operation.

Box (Pin 17). Black box keying output is an active High, CMOS level signal used to key in the black box in the captions/text displays. This output is in the high-impedance state when the background attribute is set to semi-transparent.

RED, GREEN, BLUE (Pins 2, 3, 18). Positive acting CMOS levels signals.

Color Mode: Red, Green and Blue character video outputs for use in a color receiver.

- Mono Mode: All three outputs carry the character luminance information

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Note: The selection of Color/Mono Mode is user controlled in bit D_1 of the Configuration Register (Address=00h). (See Internal Registers section, page 33).

CSync (Pin 8). Sync slice level. A 0.1-µF capacitor must be tied between this pin and analog ground V_{SS}(A). This capacitor stores the sync slice level voltage.

LPF (Pin 9). Loop Filter. A series RC low-pass filter must be tied between this pin and analog ground V_{SS}(A). There must also be second capacitor from the pin to V_{SS}(A).

RREF (Pin 10). Reference setting resistor. Resistor must be 10 kOhms, ±2%.

Power Supply

V_{DD} (Pin 12). The voltage on this pin is nominally 5.0 Volts and may range between 4.75 to 5.25 Volts with respect to the V_{SS} pins.

V_{SS} (Pins 1, 11). These pins are the lowest potential power pins for the analog and digital circuits. They are normally tied to system ground.

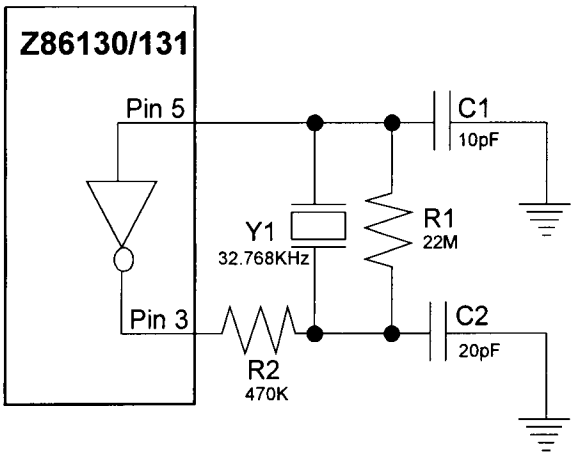
Note: The recommended printed circuit pattern for implementing the power connection and critical components is in the Application Information section, page 58.

PIN DESCRIPTIONS (Z86130/131 ONLY)

Inputs

VIDEO (Pin 7). Composite NTSC video input, 1.0V p-p (nom), band limited to 600 kHz. The circuit operates with signal variation between 0.7–1.4V p-p. The polarity is sync tips negative. This signal pin should be AC coupled through a 0.1 µF capacitor and driven by a source impedance of 470 ohms or less.

HIN/XIN (Pin 5). This pin can function in two different modes. When XTAL mode has been selected (see HIN description below) the horizontal sync signal is generated on the chip using an external 32.768-kHz crystal circuit, as illustrated below. This circuit must be connected between pin 5 and 3.



Crystal Type: 32.768 kHz, CL=12.5pF
Series Resistance < 35 kOhms
(18 kOhms typ)
Epson, C-001R 32.768 kHz or
Fox, NC26, NC28 or equivalent

Figure 6. XTAL Circuit

When HIN mode has been selected a Horizontal Sync input signal at CMOS level must be supplied to pin 5. When the device is used in VIDEO LOCK mode, this signal pulls the on-chip V_{CO} within the proper range. The circuit uses the frequency of this signal which must be within ±3% F_h but can be of either polarity. When used in the H LOCK mode, the V_{CO} phase locks to the rising edge of this signal. The HPOL bit of the H Position register can be set to operate with either polarity of input signal (usually the H Flyback signal).

SMS (Pin 6). Mode select pin for the Serial Control Port. When this input is at a CMOS High state (1) the Serial Control Port operates in the SPI mode. When the input is Low (0), the Serial Control Port operates in the I^2C slave mode. In SPI mode, the SEN pin must be tied High. (See Reset Operation section, below.)

SEN (Pin 4). Enable signal for the SPI mode operation of the Serial Control Port. When this pin is Low (0), the SPI port is disabled and the SDO pin is in the high-impedance state. Transitions on the SCK and SDA pins are ignored. SPI mode operation is enabled when SMS is High (1).

SCK (Pin 15). Input pin for serial clock signal from the master control device. In I^2C mode operation the clock rate is expected to be within I^2C limits. In SPI mode, the maximum clock frequency is 10 MHz.

I^2C SEL (Pin 1). Tying this pin Low selects the Slave Read Address 29h and the Slave Write Address 28h. Tying this pin High selects the alternate Slave Address but it is not available in the current version.

H SEL (Pin 2). It selects the source of the Horizontal Sync signal. Tying pin 2 High selects the XTAL mode. The 32.768-kHz crystal circuit must be connected between pins 5 & 3. Tying pin 2 Low selects HIN mode operation. The appropriate Horizontal Sync signal must be supplied to pin 5.

Reset Operation. When the SMS and SEN pins are both in the Low (0) state, the part is in the Reset state. Therefore, in the I^2C mode the SEN pin can be used as an NReset input. When SPI mode is used, if three wire operation is desired, both SMS and SEN can be tied together and used as the

PIN DESCRIPTIONS (Z86130/131 ONLY) (Continued)

NReset input. In either mode, NReset must be held Low (0) for at least 100 ns.

Input/Output

V_{IN}/INTRO (PB:Z86130 only; Pin 13). This pin can be used as V_{IN}/INTRO for Z86131. It is a dedicated output pin, PB (Program Blocking), in Z86130.

In the Z86130, as described in the Input section, PB output is High for indicating the incoming video program is in the program blocking set-up.

In the Z86131, this pin is an output providing an interrupt signal to the master control device in accordance with the settings in the interrupt Mask Register.

SDA (Pin 14). When the Serial Control Port has been set to I^2C mode operation, this pin serves as the bidirectional data line for sending and receiving serial data. In SPI mode operation it operates as serial data input. SPI mode output data is available on the SDO pin.

Outputs

SDO (Pin 16). Provides the serial data output when SPI mode communications have been selected. This pin is not used in I^2C mode operation.

PB (Pin 13). This pin is for the Z86130 only and refer to V_{IN}/INTRO(PB) descriptions in the Input/Output section above.

XOUT (Pins 3). This pin is XTAL output. It is be NC (No connect for inputting 32.768-kHz frequency from external device.

CSync (Pin 8). Sync slice level. A 0.1-µF capacitor must be tied between this pin and analog ground V_{SS}(A). This capacitor stores the sync slice level voltage.

LPF (Pin 9). Loop Filter. A series RC low-pass filter must be tied between this pin and analog ground V_{SS}(A). There must also be second capacitor from the pin to V_{SS}(A). Values for the three parts to be specified at a later date.

RREF (Pin 10). Reference setting resistor. Resistor must be 10 kohms, ±2%.

NC. No Connect

Pin 17, 18. These pins are NC (No Connect).

Power Supply

V_{DD} (Pin 12). The voltage on this pin is nominally 5.0 Volts and may range between 4.75 to 5.25 Volts with respect to the V_{SS} pins.

V_{SS} (Pins 11). These pins are the lowest potential power pins for the analog and digital circuits. They are normally tied to system ground.

Note: The recommended printed circuit pattern for implementing the power connection and critical components is in the Application Information section, page 58.

Z86129/130/131 BLOCK DIAGRAM DESCRIPTION

As discussed, the Z86129/130/131 are defined differently for the requirements of Line 21 Data applications. However the part number, Z86129, is used to describe the functions of the block diagram. In this description, there are some descriptions that are not applicable to the Z86130/131 for the feature differences listed on page 1.

The Z86129 is designed to process both fields of Line 21 of the television VBI and provide the functional performance of a Line 21 Closed-Caption decoder and Extended Data Service decoder. It requires two input signals, Composite Video and a horizontal timing signal (HIN), and several passive components for proper operation. A vertical input signal is also required if OSD display mode is desired when no video signal is present. The Decoder performs several functions, namely extraction of the data from Line 21, separation of the normal Line 21 data from the XDS data, on-screen display (Z86129 only) of the selected data channel and outputting of the XDS data through the serial communications channel.

Input Signals

The Composite Video input should be a signal which is nominally 1.0 Volt p-p with sync tips negative and band limited to 600 kHz. The Z86129 operates with an input level variation of ±3 dB.

The HIN input signal is required to bring the VCO close to the desired operating frequency. It must be a CMOS level signal. The HIN signal can have positive or negative polarity and is only required to be within 3% of the standard H frequency. When configured for EXT HLK operation, this signal should correspond to the H Flyback signal.

The timing difference between HIN rising edge and the leading edge of composite sync (of VIDEO input) is one of the factors that affects the horizontal position of the display. Any shift resulting from the timing of this signal can be compensated for with the horizontal timing value in the H Position register.

Video Input Signal Processing

The Comp Video input is AC coupled to the device where the sync tip is internally clamped to a fixed reference voltage by means of a dual clamp. Initially, the unlocked signal is clamped using a simple clamp. Improved impulse noise performance is then achieved after the internal sync circuits lock to the incoming signal. Noise rejection is obtained by making the clamp operative only during the sync tip. The clamped composite video signal is fed to both the Data Slicer and Sync Slicer blocks.

The Data Slicer generates a clean CMOS level data signal by slicing the signal at its midpoint. The slice level is established on an adaptive basis during Line 21. The resultant value is stored until the next occurrence of that Line 21. A high level of noise immunity is achieved by using this process.

The Sync Slicer processes the clamped Comp Video signal to extract Comp Sync. This signal is used to lock the internally generated sync to the incoming video when the video lock mode of operation has been enabled. Sync slicing is performed in two steps. In the non-locked mode, the sync is sliced at a fixed offset level from the sync tip. When proper lock operation has been achieved, the slice level voltage switches from a fixed reference level to an adaptive level. The slice level is stored on the sync slice capacitor, CSYNC.

The Data Clock Recovery circuit operates in conjunction with the Digital H Lock circuit. They produce a 32H clock signal (DCLK) that is locked in phase to the clock run-in burst portion of the sliced data obtained from the Data Slicer. When Line 21 code appears, DCLK phase lock is achieved during the clock run-in burst and used to reclock the sliced data. After phase lock is established it is maintained until a change in video signal occurs.

The Digital H Lock circuit produces the video timing gates, PG, STG, and so on, which are locked in phase with HSYNC, the video timing signal, no matter which H lock mode is used in the display generation circuits. This independent phase lock loop is able to respond quickly to changes in video timing, without concern for display stability requirements.

VCO and One Shot

All internal timing and synchronizing signals are derived from the on-board 12-MHz VCO. Its output is the Dot Clk signal used to drive the Horizontal and Vertical counter chains and for display timing. The One Shot circuit produces a horizontal timing signal derived from the incoming video and qualified by the Copy Guard logic circuits.

The VCO can be locked in phase to two different sources. For television operation, where a good horizontal display timing signal is available, the VCO is locked to the HIN input through the action of the Phase Detector (PH2). When a proper HIN signal is not available, such as in a VCR, the VCO can be locked to the incoming video through the Phase Detector (PH1). In this case, the frequency detector (FR) circuit is activated as required to bring the VCO within the pull-in range of PH1.

Z86129/130/131 BLOCK DIAGRAM DESCRIPTION (Continued)

Timing and Counting Circuits

The Dot Clk is first divided down to produce the character timing clock CHAR CLK. This signal is then further divided to generate the horizontal timing signals, H, 2H and HSQR. These timing signals are used in the data output (display) circuits.

The H signal is further divided in the LINE and FLD CNTR to produce the various decodes used to establish vertical lock and to time the display and control functions required for proper operation. The H signal is also used to generate the Smooth Scroll timing signal for display.

The V Lock circuits produce a noise free vertical pulse derived from the horizontal timing signal. When the user selects Video as the vertical lock source, the internal synchronizing signals are phased up with the incoming video by comparing the internally generated vertical pulse to an input vertical pulse derived from the Comp Sync signal provided by the Sync Slicer. In the vertical lock set to V_{IN} mode the V_{IN} signal is used in place of the signal derived from Comp Sync. In either case, when proper phasing has been established, this circuit outputs the LOCK signal which is used to provide additional noise immunity to the slicing circuits.

The LOCKed state is established only after several successive fields have occurred in which these two vertical pulses remain in sync. When LOCKed, the internal timing flywheels until such time as the two vertical pulses lose coincidence for a number of consecutive fields. Until LOCK is established, the decoder operates on a pulse for pulse basis.

Command Processor

The Command Processor circuit controls the manipulation of the data for storage and display. It processes the Control Port input commands to determine the display status desired and the data channel selected. During the display time (lines 43–237), this information is used to control the loading, addressing and clearing of the Display RAM and the operations of the Character ROM and Output Logic circuits.

During data recovery time (TV lines 21–42), the Command Processor, in conjunction with the data recovery circuits, recovers the XDS data and the data for the selected data channel. Data is sent to the RAM for storage and display and/or to the serial port, as appropriate. Where necessary, the Command Processor converts the input data to the appropriate form.

Output Logic (Z86129 only)

The output logic circuits operate together to generate the output color signals RED, GREEN and BLUE and the Box signal. When MONOchrome mode is selected all three color outputs carry the Luminance information. These outputs are positive output logic signals.

The character ROM contains the dot pattern for all the characters. The output logic provides the hardware underline, graphics characters and the Italics slant generator circuits. The smooth scroll display is achieved by the smooth scroll counter logic controlling the addressing of the Character ROM.

Decoder Control Circuit

The Decoder Control circuit block is the users communications port. It converts the information provided to the control port into the internal control signals required to establish the operating mode of the decoder. This port can be operated in one of two serial modes. The SMS pin is used to establish the serial control mode to be used.

In the two-wire (I^2C) control mode, the Z86129/130/131 respond to its slave address for both the read and write conditions. If the read bit is Low (indicating a WRITE sequence) then the Z86129/130/131 responds with an acknowledge. The master should then send an address byte followed by a data byte. If the read bit is High (indicating a READ sequence) then the Z86129/130/131 responds with an acknowledge followed by a status byte then a data byte. Read data is only available through indirect addressing. Write addressing exhibits both indirect and direct modes. The busy bit in the status byte indicates if the write operation has been completed or if read data is available.

The SPI mode is a three wire bus with the Z86129/130/131 performing as the slave device. Communication is synchronized by the SCK signal generated by the master. Typically, the serial data output is transmitted on the falling edge of SCK and the received data is captured on the rising edge of SCK. All data is exchanged as 8-bit bytes.

Voltage/Current Reference

The Voltage/Current reference circuit uses an externally connected resistor to establish the reference levels that are used throughout the Z86129/130/131. The use of an external resistor provides improved internal precision at minimal additional cost.

Z86129/130/131 FUNCTIONAL DESCRIPTION

As discussed, the Z86129/130/131 are defined differently for the requirements of Line 21 Data applications. However the part number, Z86129, is used for the Z86129/130/131 functional descriptions. In this description, there are some descriptions that are not applicable to the Z86130/131 for the feature differences listed on page 1.

The Z86129 provides full function NTSC, Line 21 performance. Input commands are included to enable the decoder to process and display any of the eight Caption/Text data channels (CC1, CC2, CC3, CC4, T1, T2, T3 or T4) contained in Line 21 of either field of the incoming video. XDS data can also be selected for display. The DECODER ON/OFF commands control whether or not the Line 21 data in the selected channel is actually displayed. When switched to the DECODER OFF (TV) state, incoming data in the selected channel is still processed, but not displayed.

The Z86129/130/131 can also be configured to operate with PAL or SECAM video signals. It decodes information encoded into its VBI in Line 22. The encoded data must conform to the waveform and command structure defined for NTSC Line 21 operation.

VCO Lock

The design includes a VCO with stable gain characteristics and good power supply rejection. The internal horizontal and vertical synchronizing circuits provide a high degree of noise immunity. There are options for both horizontal and vertical lock. The VCO can be phase locked either to the horizontal signal derived from the video input signal (VIDEO) or to the externally supplied HIN signal, typically horizontal flyback.

HIN lock is used to provide a display having a minimum of observable jitter. This condition requires an HIN signal derived from the TV display and of the proper polarity. Such a signal is readily available in a television receiver. VIDEO lock mode enables the VCO to lock in phase to the incoming video signal, thus providing good operation in an application where no display related HIN signal is available, such as in a VCR.

Video Timing

Timing signals are derived from the VCO for use in the line counting and display circuits. Line counting requires proper identification of the input signal's vertical pulse. Default operation uses the vertical sync signal derived from the video input signal as the source for vertical lock. This method results in locking characteristics having good performance and good noise immunity.

In the event that OSD operation is required under conditions when no input video is present, it would be necessary to set the Z86129 for V_{IN} lock. In this mode, the vertical timing is determined from the vertical pulse signal supplied to the V_{IN} pin.

The horizontal position of the caption display is determined by the internal timing circuits. A default condition has been established that should result in a well centered display in a typical application. However, because signal delays through video processing circuits can vary between designs, the Z86129 provides the user with the ability to change the default timing. No matter which of the horizontal lock modes are selected, the display horizontal position on the screen can be adjusted in quarter character (330 ns) steps by serial port commands.

Displayable Character Set (Z86129 only)

Normal Mode. Characters are displayed as white or colored dot matrix characters on an opaque background. The Box is normally black but the Z86129 can be set to a blue background Box with a serial command. The characters are described by a 12 by 18 dot pattern within a character cell which is 16 dots wide by 26 dots high per frame. The location of the character luminance within the character cell varies from character to character to allow for the display of lower case letters with descenders. All characters have at least a 1-dot border of black around each character. Underline is also provided. Figure 7 illustrates the Z86129 standard character map and font.

The character ROM consists of a 12 by 18 dot matrix pattern per character. Alternate rows and columns are read out in each field to produce an interleaved and rounded character. A display row contains a maximum of 32 characters plus a leading and trailing black box, each a character cell in width, making the overall width of a display row 34 x 8 = 272 dots. Successive display rows are butted together so that the total display occupies 195 dots high.

The black box 34 character cells wide by 195 dots high results in a box size of 45.018 µs in width by 195 scan lines in height. The Box starts in scan line 43 and extends to scan line 237. Theoretically, the display is horizontally centered in the video display when the Box starts 13.2 µs after the leading edge of H.

The default setting of the Z86129 places the center of the Box at about 13.5 µs to allow for some delay in the normal video path. However, the Box horizontal position can be adjusted by the user in 330 ns increments. The display is approximately within the safe title area for NTSC receivers.

Z86129/130/131 FUNCTIONAL DESCRIPTION (Continued)

Character width is 42.37 µs also centered on the screen, resulting in a leading and trailing 1.32 µs black border.

An optional Caption display mode, Drop Shadow, can be selected by the user through the serial port. This display mode eliminates the black box around the characters and places a 2-dot black shadow to the right and below the character luminance dots when in the 15 scan line per row mode. This display mode is usable in Captions, Text and OSD displays. Figure 8 illustrates the characters with shadowing added.

Extended Features

EIA–608 defined new extended features such as optional Background and Foreground display attributes and optional Extended Characters. The Z86129 always responds to the Extended Characters but the Extended Background/Foreground response can be controlled by the user. The Background and Foreground attributes add codes for background colors, black foreground as well as transparent, opaque and semi-transparent background. The BOX signal output pin is set to a tri-state condition whenever one of the semi-transparent attribute codes is active. The external keying circuits can then use this condition to implement the intended video display.

The font for the Extended Characters are illustrated in Figure 9. The accented capital letters have been implemented by placing the accent marks above the character cell. When selected, this mode results in the accent marks being written into the character cell space of the row above. In some operating modes, the Z86129 expands the size of the overall box height by adding two additional scan lines at the top and one additional line at the bottom. This addition makes room for the accent marks in the topmost row and add a black line below the descenders of any lowercase characters in the last row.

This approach is desirable because shrinking the capitals to make room for the accent mark within the character cell makes poor quality characters and in some cases there would be no differentiation between the capital and lower case letter. It also has the advantage of minimizing the ROM size and providing a good readable font that closely matches what is normally seen in print.

In the unlikely case of a conflict between an accented capital letter in one row and a lower case descender in the same character position in the row above, the descender is given priority. The improved readability of this approach over shrunk capital letters far outweighs this potential conflict and results in a cost-effective compromise for providing a full, extended features implementation.

The Extended Characters share their address space with the OSD Graphics Characters. When a BOX display is used the Extended Character set is in force. However, if a Drop Shadow display is used the Graphics Characters are in force. For Caption and Text display modes, if Drop Shadow is set, the user must also command the Z86129 to switch back to Extended Characters.

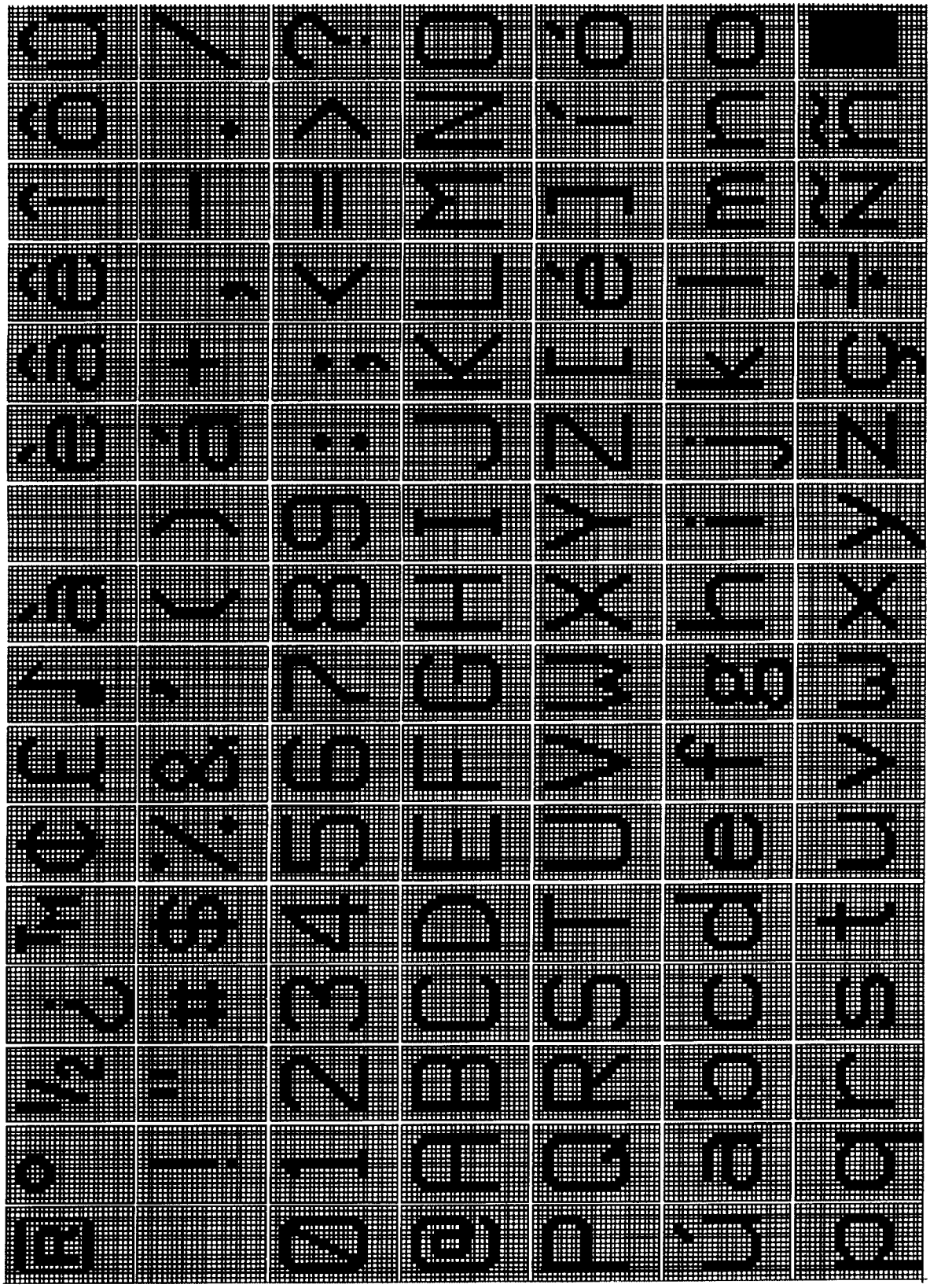


Figure 7. Z86129 Standard Character Map and Font

Z86129/130/131 FUNCTIONAL DESCRIPTION (Continued)

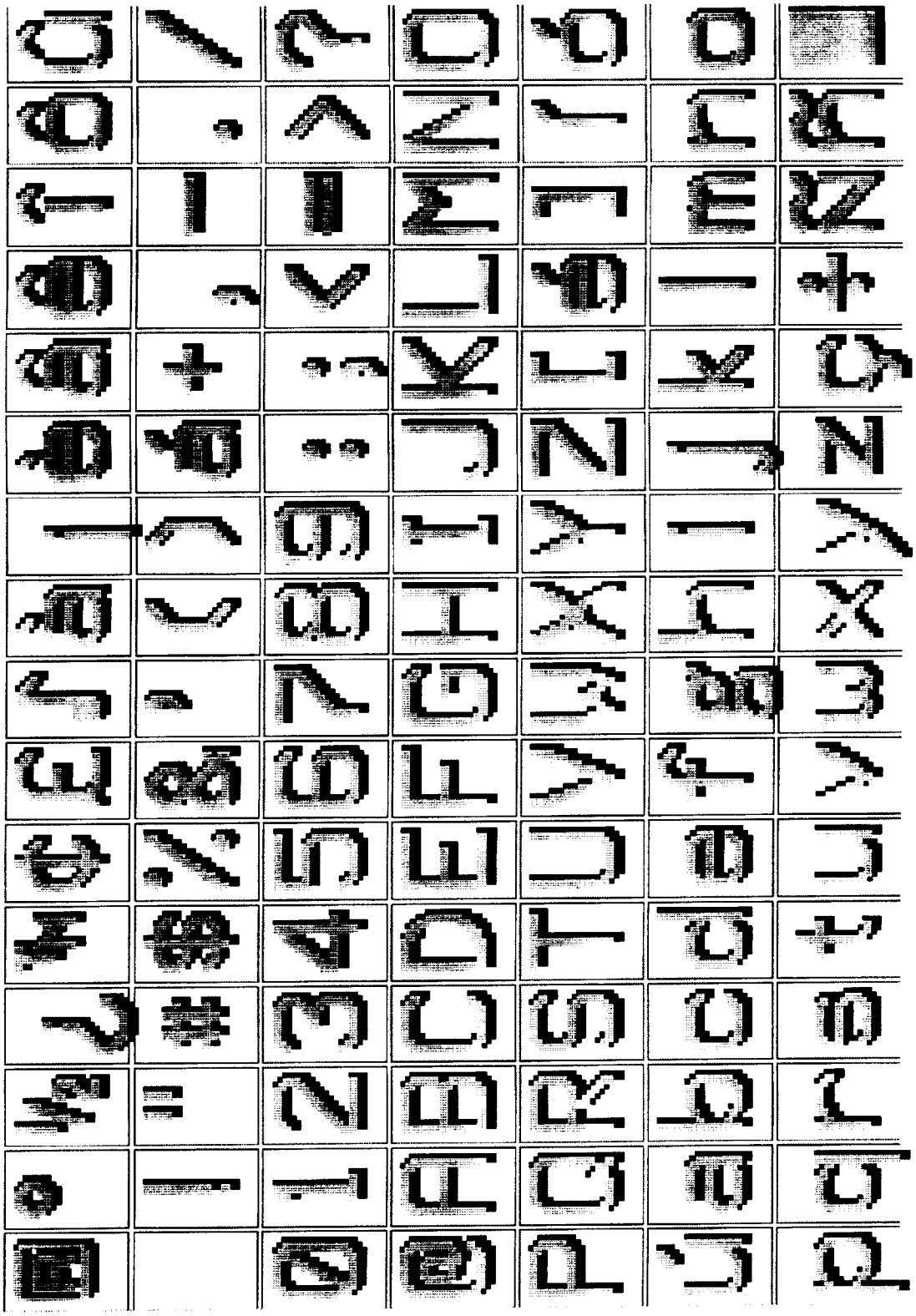


Figure 8. Caption Display Mode, Drop Shadow

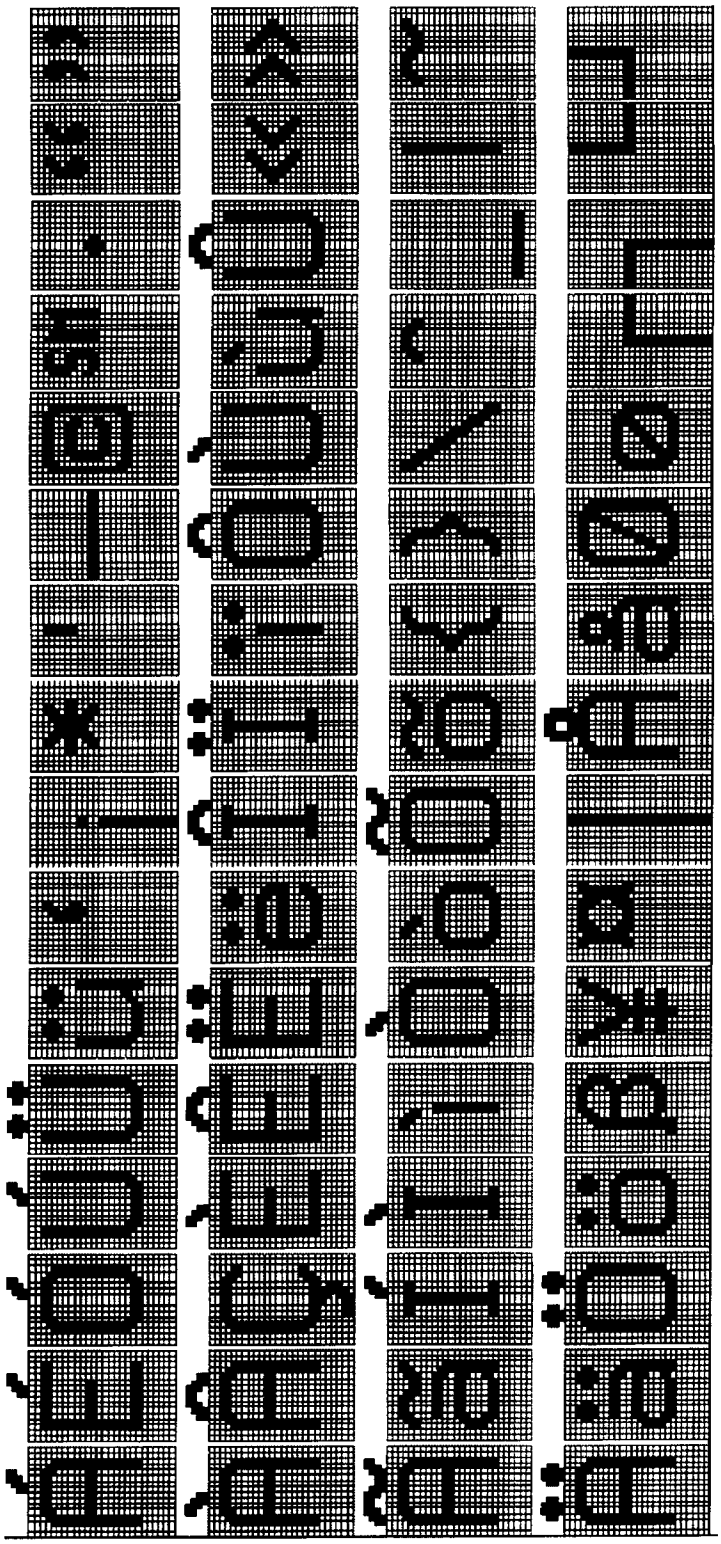


Figure 9. Extended Characters Font

Z86129/130/131 FUNCTIONAL DESCRIPTION (Continued)

Text Mode Display (Z86129 Only)

When TEXT mode is selected, a black box is displayed as long as valid Line 21 code in the field selected is being detected. The Z86129 provides the option to make the box blue instead of black. This option holds for Captions as well as Text.

The default TEXT display mode uses a 15 row by 34 character black box. TEXT characters are displayed as they are received starting in the top row. Successive carriage returns move the display down successive rows until all 15 rows have been displayed. Thereafter, the text scrolls up as new characters are added to the bottom row.

If the data for the selected channel is interrupted by a command for another channel, data processing stops, but the display remains. When a Resume Text command is received, data processing resumes and the new characters are added starting at the position that the display row/column pointer was in at the interruption of data processing. If a Start Text command is received, the display is cleared and new characters are displayed starting in row 1, column 1 (left side).

The number of display rows and the location (base row) of the TEXT box, can be altered by the user. In this way, the user can decide how much of the screen can be covered when displaying non-program related information.

When scrolling, the display shifts one scan line per frame until a complete row has been scrolled. If a carriage return is received before scrolling is complete, the display immediately completes the "scroll" by jumping up the remaining scan lines and start displaying the new text.

Caption Mode Display (Z86129 Only)

According to the FCC specifications Caption data can appear in any of the 15 display rows but a single caption may consist of no more than 4 rows. The form of the caption display depends on the caption mode indicated by the transmitted caption command, Pop-on, Paint-on or Roll-up. The Z86129 can display a single caption having as many as eight rows. When any of the CAPTION display modes have been selected, the screen is transparent. (Display box is only present when a caption is being displayed.)

Pop-on captions work with two caption memories. One of them is normally displayed while the other is being used to accumulate new caption data. A new caption is popped-on by swapping the two memories with the End Of Caption (EOC) command. When the on-screen memory is erased, the screen is blank (transparent) and the memory defaults to the row/column pointer at row 1, column 1 and monochrome non-underlined.

When caption mode is selected, the decoder processes any data following the Resume Caption Loading (RCL) command (or the EOC). Normally, this command is followed by a Preamble Address Code (PAC) to indicate the row, column and character attributes to be used with the following data. If no PAC is received, the data is added to the location most recently indicated by the row/column pointer prior to the receipt of the RCL command.

Paint-on caption mode is essentially equivalent to the Pop-on mode except that the data received after the Resume Direct Captioning (RDC) command is written to the on-screen memory rather than the off-screen memory. All the rules for PACs, Midcodes, and so on, are otherwise the same.

Roll-up caption mode presents a "text" like display that is limited to 2, 3 or 4 rows, depending on the Resume Roll-up (RUn) command used. The PAC following the RUn command is used as the BASE ROW for the ROLL-UP display. The BASE ROW is the "bottom" row of the ROLL-UP display. In this case, the black box does not appear until characters are being displayed and the box is only wide enough to provide a leading and trailing box in each line. The new data appears in the bottom row and as each carriage return is received, the row scrolls up and the new data added to the bottom. When the number of rows indicated by the Resume command has been reached, the data in the top row scrolls off as new data is added to the bottom.

The TAB (INDENT) PAC permits placing Captions starting at 4 character boundaries in any caption row. The TAB OFFSET command provides the means for adjusting the starting position for a Caption at any column position in the current row.

XDS Display Modes (Z86129 Only)

Two preprogrammed XDS display modes are provided. One provides information about the current program that would be of interest for "channel grazing". The second display shows the grazing packets plus additional XDS packets which inform the viewer about the program content. Information is displayed as it is received. The displays use drop shadow mode with 15 scan lines per row.

The XDSG mode is the GRAZE (channel grazing) display (Figure 10). The display contains three rows of information at the top of the screen, formatted for easy reading. They contain the following XDS packet information:

OSD Row 1	Network Name, Call Letters (Green)
OSD Row 2	Program Name (Italics, Underline, White)
OSD Row 3	Program Length, Time In Show (Cyan)

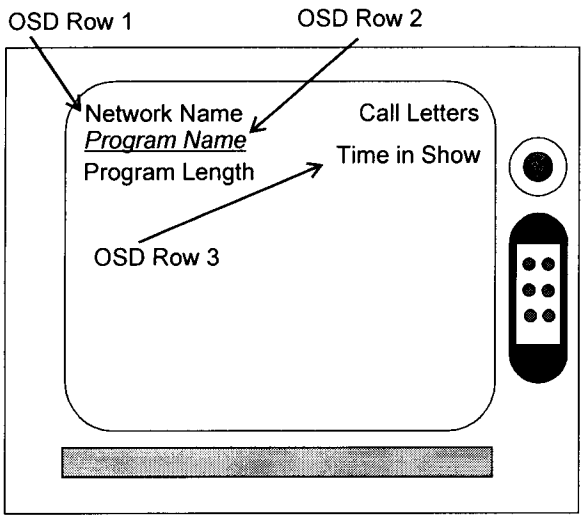


Figure 10. XDSG (Graze) Mode Sample Display

The XDSF mode is the FULL (information) display (Figure 11). This display shows the same information as the GRAZE display and adds the program type as well the first four program description rows (if transmitted). Although XDS defines eight program description rows, the first four are identified as containing the most important information. The display of Program Description is limited to the first four rows because eight rows would obscure much of the screen and because more than four rows is not likely to be sent due to the time required for transmission.

Because 15 scan lines per row mode are being used, rows 10–13 appears at the bottom of the screen.

OSD Row 1	Network Name, Call Letters (Green)
OSD Row 2	Program Name (Italics, Underline, White)
OSD Row 3	Program Length, Program Type, Time In Show (Cyan)
OSD Row 10	Program Description Row 1 (Yellow)
OSD Row 11	Program Description Row 2 (Yellow)
OSD Row 12	Program Description Row 3 (Yellow)
OSD Row 13	Program Description Row 4 (Yellow)

When an XDS display mode has been selected, the information is displayed as the appropriate packets are received. The display remains on-screen as long as valid XDS data continues to be received. If the 16 Second Erase Timer is enabled (the default condition), the XDS display is erased when no valid XDS data has been received for 16 Seconds. If subsequent XDS data is received with displayable packets, that information reappears on the screen. XDS data recovery can be active in the XDS display mode.

The XDS display mode is turned off by selecting a different display mode.

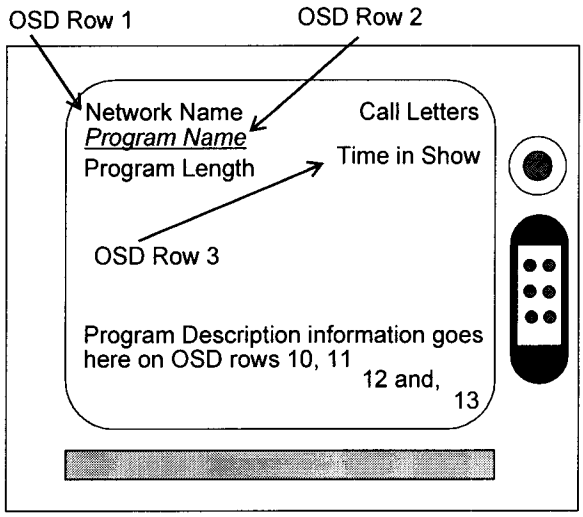


Figure 11. XDSF Mode Sample Display

Display Erase and Autoblanking (Z86129 Only)

The display is erased in the TEXT mode by the Start Text command (but the box is maintained) and in the CAPTION mode by the Erase Displayed Memory (EDM) command. The non-displayed memory can be erased by the Erase Non-displayed Memory (ENM) command.

Four other events can also cause the display to be erased.

1. A change in the display mode, such as from CC1 to T1, CC1 to XDSF, and so forth, clears the memory and hence the display.
2. A loss of video lock, such as on a channel change, causes the screen to be cleared. The current active display mode does not change. For example if CC1 was selected and ON before the channel change the device remains in the CC1/ON state after channel change.
3. The third action that clears the displayed memory is the activation of the autoblanking circuit. The autoblanking circuit monitors the presence of a Line 21 waveform in the video field corresponding to the data channel selected for display. The decoder is held in the Decoder OFF (TV) state until a Line 21 waveform is continuously detected for a period of 0.5 seconds. When a valid Line 21 waveform has been detected for 0.5 seconds, and assuming that the user has selected the Decoder ON state, the normal display for the data

Z86129/130/131 FUNCTIONAL DESCRIPTION (Continued)

channel selected is presented. The autoblanking circuit is not activate again until a valid Line 21 waveform has been lost for 1.5 seconds. Any data received during the 1.5-second period resets the counter so that autoblanking is only activated on continuous loss of the Line 21 waveform for 1.5 seconds.

Note: Valid Line 21 waveform is defined as the presence of a 7-cycle run-in clock and a start bit on Line 21 of the field being examined.

4. The fourth method of clearing the screen is by the action of the 16 Second Erase Timer. *This function is only active when a CAPTION or XDS display mode has been selected.* If no data is received for the display channel selected for a 16 second period, the on-screen memory is erased. The decoder is still in the selected channel and with the decoder ON, so that when data for the selected channels resumes, it is displayed.

Z86129/130/131 FEATURE SET

As discussed, the Z86129/130/131 are defined differently for the requirements of Line 21 Data applications. However the part number, Z86129, is used to describe the feature set of the Z86129/130/131. In this description, there are some descriptions not applicable to the Z86130/131 for the feature differences listed on page 1.

The primary features of the Z86129 are briefly described below. More complete descriptions can be found in later sections of this document.

VBI Data Processing

The Z86129 extracts the data in Line 21 of the incoming video. All data channels, in both video fields are supported. Specifically, the Z86129 can:

1. Process data from both fields of Line 21 simultaneously.
2. Output XDS data through the serial port while displaying selected data.
3. Output XDS data through the serial port raw or filtered.
4. XDS filters are selectable from a list of pre-programmed values including Program Rating and Time of Day/Local Time.
5. Output line 21 data through serial port raw(Z86130 only).
6. NTSC or PAL operation selectable.

The data extracted from Line 21 of the incoming video by the Z86129 may be displayed in different ways according to the user selection and the type of data. The display features available on the Z86129 only are:

1. Ten different Line 21 data display modes; CC1–CC4, T1–T4, plus two standard templates for XDS displays.
2. Pop-on, Paint-on and Roll-up CAPTION displays.
3. TEXT display default is a full screen, 15-row display.
4. User can vertically reduce and reposition the TEXT display as desired.
5. Color or Monochrome display mode selectable.
6. XDSG Display Mode (channel grazing): automatic display of Network Name, Call Letters, Program Name, Program Length, and Time In Show data packets.
7. XDSF Display Mode (full information): automatic display of XDSG Display Mode information plus: Program Type (only basic types), and Program Description.

General Purpose OSD Modes (Z86129 Only)

In addition to displaying data extracted from Line 21 of the incoming video, the Z86129 can display information supplied through its serial port. This mode is referred to as On-Screen Display (OSD) display mode. This mode provides:

1. Programmable Full Screen OSD: 15 display rows by 32 character columns.
2. Graphics characters.
3. Double-High and Double-Wide characters.
4. Fully programmable display positioning; information may be placed anywhere on the screen.
5. Accepts externally supplied, or internally generated VSYNC to enable OSD even when no video is present.

Character Set (Z86129 Only)

The Z86129 has a new character set with extended features, such as:

1. New font with descenders on lower case letters.
2. Optional display mode using drop shadow font (in other words, fringing appears on each character rather than a solid, "black box" background).
3. EIA–608 Extended Characters.
4. EIA–608 Background and Foreground attributes.
5. Special framing and graphics characters for OSD display.
6. Double-High and Double-Wide character display for OSD.
7. Fifteen scan lines per character row for OSD and TEXT.

Note: Contact the nearest ZiLOG Sales office for additional information on how to define your own custom OSD character set.

Serial Communications Interface

Communications and control of the Z86129/130/131 is through a serial control interface. Two Serial Control

Z86129/130/131 FEATURE SET (Continued)

Modes are available with the Z86129/130/131 performing as a slave device. These modes are:

1. A two wire, I^2C interface.
2. A three wire, serial peripheral interface (SPI).
3. A total of five device pins are dedicated to the serial control port function. These pins are designated as:

Table 11. Z86129/130/131 Serial Control Signals

Signal	SMS	SCK	SDA	SDO	SEN
Pin #	6	15	14	16	4
I/O	I	I	I/O	O	I
I^2C	0	CLK	Data	NA	1
SPI	1	CLK	Data In	Data Out	Enable

Notes:
SMS = Serial Mode Select High = SPI and Low = I^2C.
SCK = Serial port clock for either Serial Mode.
SDA = Serial port data for I^2C Mode and Data In for SPI Mode.
SDO = Serial Data Out for SPI Mode. Not used in I^2C Mode.
SEN = SPI Mode Enable signal. Must be High for I^2C Mode.

I^2C Mode. The I2C port on the Z86129/130/131 always acts as a slave device. I2C Mode is selected by bringing the SMS pin Low and the SEN pin High. SEN must remain High whenever I2C mode is desired. If the SEN pin is brought Low, with SMS also Low, the part is reset. SDA and SCK are the data and clock lines of the I2C port, respectively. During I2C mode operation the VIN/INTRO signal (pin 13), can be configured to generate interrupt requests to the master device on selected events (see Note, next column).

SPI Mode. SSPI Mode is selected by making the SMS pin High. In SPI mode the Z86129/130/131 acts as a slave device. All communications are clocked in and out as 8-bit bytes. SCK is the serial clock (input), SDA is Data-In and SDO is Data-Out. The SEN pin enables communication when High. When Low, the SDO pin is tri-stated.

When SEN is brought High the part is synchronized and waiting for a Command. If SEN is tied High, the part can also be synchronized by a command string. During SPI mode operation the V_{IN}/INTRO signal (pin 13), can be configured to generate interrupt requests to the master device on selected events (Z86129/131 only; see Note, next column).

Caution: When the SEN and SMS pins are made Low simultaneously, the part resets.

Interrupt Generation. The V_{IN}/INTRO signal (pin 13) in Z86129/131 can be configured to provide an interrupt output on selected events. The configuration of V_{IN}/INTRO (pin 13) is user programmable to be either of two states in Z86129/131:

1. An INPUT pin for acceptance of an external VSYNC timing signal(Z86129 only).
2. An OUTPUT pin for interrupt generation on a selected events(Z86129/131).

Note: Configuring V_{IN}/INTRO as an output for interrupt generation is particularly useful when implementing the *V-Chip* feature with Z86129 in TVs and VCRs. In this configuration, Pin 13 is used to interrupt the host processor when the XDS Program Rating data packet is found. As a result the host processor is not burdened with monitoring or filtering the line 21 data stream. The Z86129/131 filters the Line 21 data stream for the host processor, and generates an interrupt only when the desired packet is found. V_{IN}/INTRO pin becomes PB in Z86130 and it serves as Program Blocking output pin for *V-Chip* application.

Setup and Operational Control

The Z86129/130/131 is extremely flexible and fully programmable through its serial communication port. The following tables provide a *partial list* of User-Programmable Features, User Selectable Display Modes, and Default Conditions upon Reset.

Z86129/130/131 Programmable Features (OSD features are for the Z86129 Only)

- Decoder ON/OFF
- TV scan lines per OSD row (13 or 15)
- EIA–608 extended attributes ON/OFF
- OSD drop shadow ON/OFF
- Color/Monochrome
- OSD Horizontal start position
- Text box size (# of rows)
- Text box starting row position
- NTSC or PAL
- Vertical Lock Source: Video or External V_{IN}
- XDS Data Output, Raw or Filtered
- H Lock Source: Video or External HIN

In addition to the programmable features just listed, the Z86129 offers a choice of eleven display modes for user selection.

Table 12. Z86129 Display Modes

Display Mode	Display Data	NTSC Field	Language
CC1	L21 Closed Captions		
CC2	L21 Closed Captions	1 (odd)	I
CC3	L21 Closed Captions	1	II
CC4	L21 Closed Captions	2 (even)	I
T1	L21 TEXT	2	II
T2	L21 TEXT	1	I
T3	L21 TEXT	1	II
T4	L21 TEXT	2	I
XDSF	XDS	2	II
XDSG	XDS	2	N/A
OSD	User Defined via Serial Port	2	N/A

The Z86129/130/131 is initialized on RESET to the following default conditions:

Table 13. RESET Default Conditions

Parameter	Reset Condition
Display Channel	CC1
Decoder	OFF
TEXT Size	15 rows
Lines/Row	13
Background	BOX
EIA–608 Extended Attributes	ON
Data Outputs	OFF
Video Standard	NTSC
Data Outputs	OFF
VCO Lock	Video
BOX Timing	13.5usec
Vertical Lock	Video
V_{IN}/INTRO	INTRO & Disabled
Horizontal Lock	Video
Color/Mono	Color
OSD Display	Drop Shadow 15 lines/row

SERIAL COMMUNICATIONS INTERFACE

Commands and data are sent to and from the Z86129/130/131 through its serial communications interface. Two Serial Control Modes are available. One mode is a two wire I^2C bus interface. The other serial mode is a three wire, synchronous serial peripheral interface (SPI). In both cases the Z86129/130/131 acts as a slave device.

This port is the path for setting the configuration and operational modes of the device. It is also the port for outputting the recovered XDS data and for inputting the OSD data for display.

Five pins are dedicated to the control port function and one additional pin can be configured to provide an interrupt output. These pins are designated as indicated in Table 14.

Table 14. Z86129/130/131 Serial Control Signals

Signal	SMS	SCK	SDA	SDO	SEN
Pin #	6	15	14	16	4
I/O	I	I	I/O	O	I
I2C	0	CLK	Data	Hi-Z	1
SPI	1	CLK	Data In	Data Out	Enable

Notes:
SMS = Serial Mode Select High = SPI & Low = I^2C.
SCK = Serial port clock for either Serial Mode.
SDA = Serial port data for I^2C Mode and Data In for SPI Mode.
SDO = Serial Data Out for SPI Mode. Not used in I^2C Mode.
SEN = SPI Mode Enable signal. Must be High for I^2C Mode.

When the Vertical Lock = VIDEO, the V_{IN}/INTRO (pin13) is configured as an output, providing the INTRO signal. This interrupt operation is available in either serial control mode.

The Z86129/130/131 is able to interrupt on the occurrence of any of several events. The master device clears the interrupt by writing to the Interrupt Request Register.

I^2C Bus Operation

The serial control mode in use is selected by the state of the SMS pin. When SMS is set Low, the Z86129/130/131 is in the I^2C mode. In this mode, the Z86129/130/131 also supports a bidirectional two wire bus and data transmission protocol. The bus is controlled by the master device, which generates the serial clock (SCK), controls the bus access and generates the Start and Stop conditions. The SDA pin is the bidirectional Data line. In this mode, the SDO output is not used, and the pin is in its high-impedance state.

The Z86129/130/131 can receive or transmit data under control of the master device. The Z86129/130/131 is a slave device. Communication is initiated when the master device sends the start condition followed by the Z86129/130/131 Slave Address Read byte (29h) or Slave Address Write byte (28h). The Z86129/130/131 responds with an Acknowledge. The I^2C RD/nWR bit is the Least Significant Bit (LSB) of the I^2C addresses listed Table 15.

Table 15. Z86129/130/131 I^2C Slave Addresses

	READ	WRITE
I^2C Address	29h	28h

Note: When the SMS and SEN pins are both Low, the part is in the RESET state. Therefore the SEN pin can be used to reset the part while in the I^2C mode. The SEN pin may be tied to an NRESET signal or tied High if no reset is desired.

The I^2C Bus Protocol

1. Data transfer can only be started when the bus is not busy.
2. During data transfer, data transitions must not occur while the clock is High.

Bus Conditions

Bus Conditions are defined as:

Not Busy. Data and Clock lines both High.

Start. A High-to-Low transition of SDA line while SCK line is High.

Stop. A Low-to-High transition of SDA line while SCK line is High.

Acknowledge. When addressed, the receiving device must output an acknowledge after the reception of each byte. The master device must generate the clock for the acknowledge bit. Acknowledge is SDA=Low. Not Acknowledge (NACK) is SDA=High.

Data. The data (SDA) is output by the transmitting device on the falling edge of SCK, MSB first. The receiving device reads the data, MSB first, on the rising edge of SCK.

Communication with the Z86129/130/131 is initiated when the master device sends the Z86129/130/131 slave address following a start condition. The Z86129/130/131 has a preset, single, seven-bit slave address. The Z86129/130/131 responds with an acknowledge. The eighth bit of the slave address is driven High for Read operations and Low for Write operations.

Writing to the I²C Bus

All write commands are either one or two byte commands. The Z86129/130/131 is enabled when a Start condition followed by its Slave Address Write byte is received. It is disabled when it deems the command to have been completed or by a Stop condition. A new Start condition without a Stop condition begins a new sequence. Therefore, successive commands may be executed by successive strings of "Start—Slave Address—Command" sequences without any intervening Stop condition being sent.

Note: The number of data bytes to be received by the Z86129/130/131 is inherent in the command and the Z86129/130/131 responds with the acknowledge signal only for the number of bytes expected. If the master writes more bytes than expected, there is no acknowledge for the extra bytes.

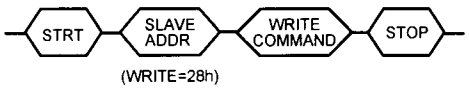
A write to the Z86129/130/131 should always be preceded by executing a Status read to verify that the Z86129/130/131 is not busy. The Status register data is output immediately following the reception of the Slave Address Read. If the RDY bit is set, the master device can initiate its write sequence, always beginning with the Start condition. The first byte of a two byte command is always written first.

An example of the master's sequence for writing a two-byte command (after RDY had been checked) would be:

Start
Slave Address
Write/Slave ACK COMMAND (master)/Slave ACK
DATA (master)/Slave ACK
Stop

I²C Two-Byte Write (Command & Data)

I²C One-Byte Write (Command)



Note: Status Register RDY bit must be read and checked prior to the STRT condition of either WRITE sequence. See One Byte Read (Status Only) in Figure 13 for more information on reading the Status Register.

Figure 12. I²C Bus WRITE (Command)

Reading Data Using the I²C Bus

With the exception of the Serial Status (SS) register, which may be read at any time, each read operation must be set up before the data can be read from the serial output registers of the Z86129/130/131. Data is set up for a read operation either automatically or manually. XDS data reads are set up automatically upon recovery by setting a valid XDS FILTER register selection. All other data read operations must be set up manually using the READ SELECT commands RDS1 and RDS2. These commands load the selected data byte or pair of bytes into the serial output register(s), set the SS register RD2 bit according to the number of data bytes requested and set the SS register DAV bit to indicate availability of data.

The Z86129/130/131 I²C Bus supports one, two and three byte read sequences. All read sequences output the SS register as the first output byte. If the serial status DAV bit is set, a two or three byte read sequence can then be initiated, beginning with a new STRT condition. If the DAV bit is not set, the I²C master device should not attempt to read any data bytes or the desired data can be lost from the Z86129/130/131output registers.

The number of data bytes available is indicated by the state of the RD2 bit of the serial status. In a typical read operation the status byte is read and the DAV and RD2 bits are examined. If one or two data bytes are available they are read in sequence separated by acknowledges.

Note: In all I²C Read operations (one, two, and three byte as defined in Figure 13) the most recent byte read from the Z86129/130/131 should be acknowledged by the master with a NACK (Not ACKnowledge). It is also necessary to read all available data in a read operation to clear the DAV bit and permit subsequent reads. DAV is cleared by the master clocking out the eighth bit of the most recent data-byte read. DAV is never cleared by just reading the SSB (one-byte read) alone. All data is output MSB first.

The master's sequence for reading two *data bytes* (total of three bytes including SSB) from the Z86129/130/131 is as:

Start
Slave Address Read/Slave ACK
SS Byte/Master ACK
Byte (slave)/Master ACK
Byte (slave)/Master NACK
Stop