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ZiLOG

Totally Logical

Z86229

NTSC LINE 21 CCD DECODER

FEATURES

Devices	Speed (MHz)	Pin Count/ Package Types	Standard Temp. Range	On-Screen Display & Closed Captioning	Automatic Data Extraction: Program Rating	Automatic Data Extraction: Time of Day
Z86229	12	18-Pin DIP, SOIC	0°C to +70°C	Yes	Yes	Yes

- Complete Stand-Alone Line 21 Decoder for Closed-Captioned and Extended Data Services (XDS)
- Preprogrammed to Provide Full Compliance with EIA–608 Specifications for Extended Data Services
- Automatic Extraction and Serial Output of Special XDS Packets (Time of Day, Local Time Zone, and Program Blocking)
- Programmable XDS Filter for a Specific XDS Packet
- Cost-Effective Solution for NTSC Violence Blocking inside Picture-in-Picture (PiP) Windows
- Minimal Communications and Control Overhead Provide Simple Implementation of Violence Blocking, Closed Captioning, and Auto Clock Set Features
- Programmable, On-Screen Display (OSD) for Creating Full Screen OSD or Captions inside a Picture-in-Picture (PiP) Window
- User-Programmable Horizontal Display Position for easy OSD Centering and Adjustment
- I^2C Serial Data and Control Communication
- Supports 2 Selectable I^2C Addresses

GENERAL DESCRIPTION

Capable of processing Vertical Blanking Interval (VBI) data from both fields of the video frame in data, the Z86229 Line 21 Decoder offers a feature-rich solution for any television or set-top application. The robust nature of the Z86229 helps the device conform to the transmission format defined in the Television Decoder Circuits Act of 1990, and in accordance with the Electronics Industry Association specification 608 (EIA–608).

The Line 21 data stream can consist of data from several data channels multiplexed together. Field 1 consists of four data channels: two Captions and two Texts. Field 2 consists of five additional data channels: two Captions, two Texts, and Extended Data Services (XDS). The XDS data structure is defined in EIA–608. The Z86229 can recover and display data transmitted on any of these nine data channels.

The Z86229 can recover and output to a host processor via the I^2C serial bus. The recovered XDS data packet is further defined in the EIA–608 specification. The on-chip XDS filters in the Z86229 are fully programmable, enabling recovery of only those XDS data packets selected by the user. This functionality allows the device to extract the required XDS information with proper XDS filter setup for compatibility in a variety of TVs, VCRs, and Set-Top boxes.

In addition, the Z86229 is ideally suited to monitor Line 21 video displayed in a PiP window for violence blocking, CCD, and other XDS data services. A block diagram of the Z86229 is illustrated in Figure 1.

GENERAL DESCRIPTION (Continued)

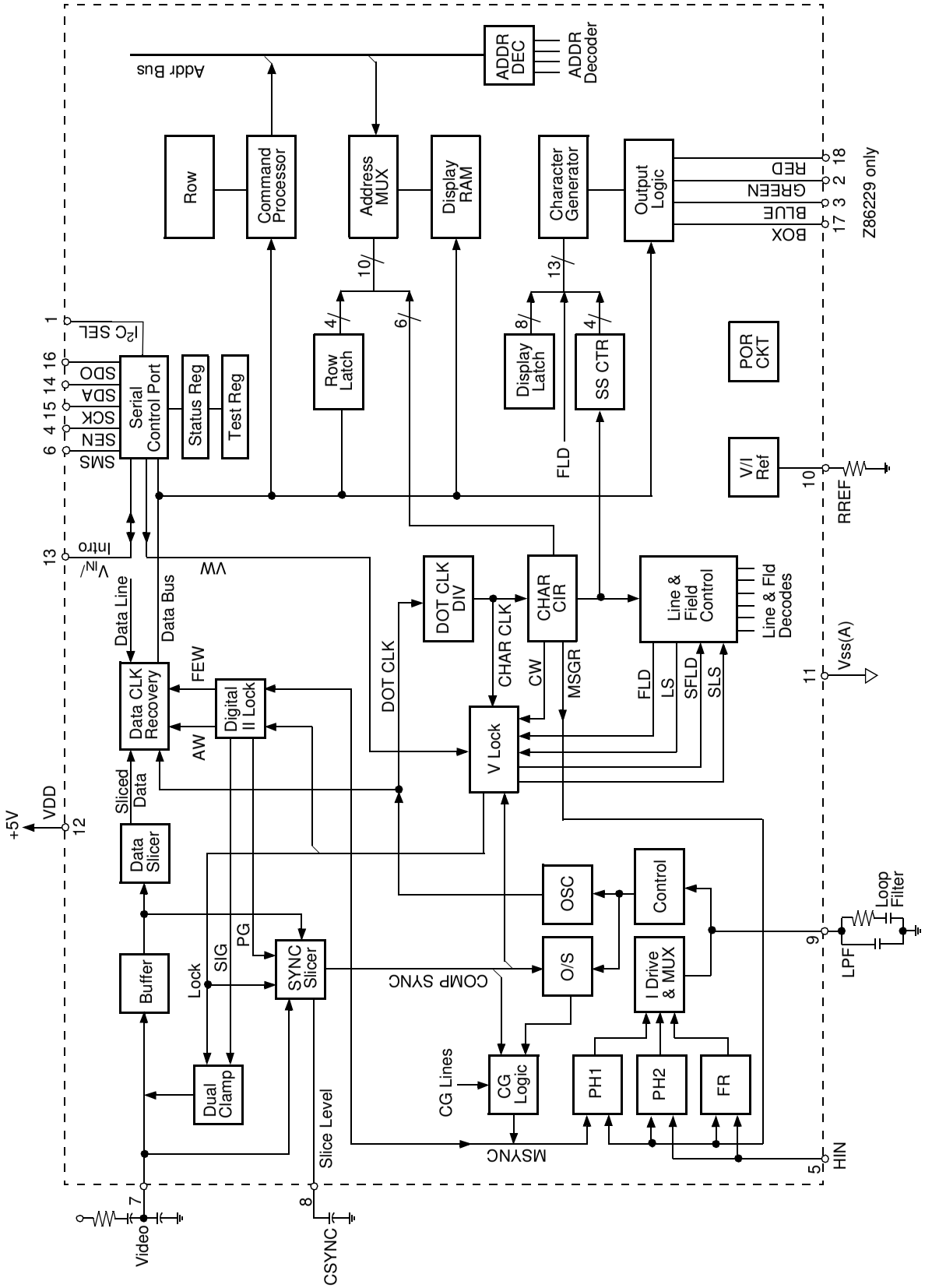


Figure 1. Z86229 Block Diagram

PIN DESCRIPTION

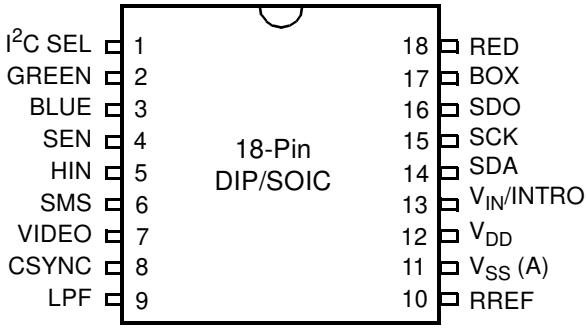


Figure 2. Z86229 Pin Configuration

Table 1. Z86229 Pin Identification*

No.	Symbol	Function	Direction
1	I^2C SEL	I^2C Address Selection	Input
2	GREEN	Video Output	Output
3	BLUE	Video Output	Output
4	SEN	Serial Enable	Input
5	HIN	Horizontal In	Input
6	SMS	Serial Mode Select	Input
7	VIDEO	Composite Video	Input
8	CSYNC	Composite Sync	Output
9	LPF	Loop Filter	Output
10	RREF	Resistor Reference	Input
11	V_{SS} (A)	Pwr. Supply (Analog) GND	
12	V_{DD}	Power Supply	
13	V_{IN}/INTRO	Vertical In/Interrupt Out	In/Output
14	SDA	Serial Data	In/Output
15	SCK	Serial Clock	Input
16	SDO	Serial Data Out	Output
17	BOX	OSD Timing Signal	Output
18	RED	Video Output	Output

Note: *DIP and SOIC pin configurations are identical.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to 6.0	V
V_{IN}	DC Input Voltage	–0.5 to V_{DD} +0.5	V
V_{OUT}	DC Output Voltage	–0.5 to V_{DD} +0.5	V
I_{IN}	DC Input Current per Pin	+10	mA
I_{OUT}	DC Output Current per Pin	+20	mA
I_{DD}	DC Supply Current	+30	mA
P_D	Power Dissipation per Device	300	mW
T_{STG}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

Notes:
*Voltages referenced to V_{SS} (A). Values beyond the maximum ratings listed above may cause damage to the device. Functional operation should be restricted to the limits specified in the DC and AC Characteristics tables or Pin Description section.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 3).

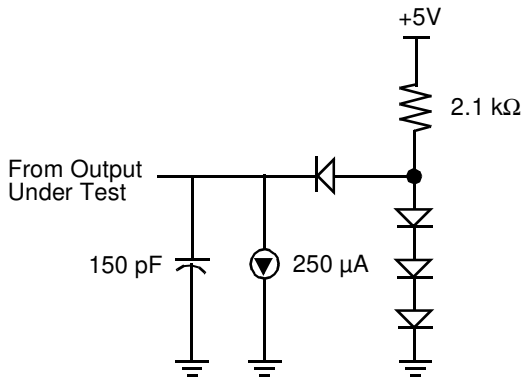


Figure 3. Standard Test Load

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{IL}	Input Voltage Low		0	0.2 V_{DD}	V
V_{IH}	Input Voltage High		0.7 V_{DD}	V_{DD}	V
V_{OL}	Output Voltage Low	I_{OL} = 1.00 mA	–	0.4	V
V_{OH}	Output Voltage High	I_{OH} = 0.75 mA	V_{DD} –0.4V	–	V
I_{IL}	Input Leakage	0V, V_{DD}	–3.0	3.0	µA
I_{DD}	Supply Current			30	mA

Notes: T_A = 0°C to +70°C; V_{DD} = +4.75V to +5.25V.

AC AND TIMING CHARACTERISTICS

Table 2. Composite Video Input

Parameter	Conditions
Amplitude	1.0V p-p ± 3 dB
Polarity	Sync tips negative
Bandwidth	600 kHz
Signal Type	Interlaced
Max Input R	470 ohms
DC Offset	Signal to be AC coupled with a minimum series capacitance of 0.1 µF.

ELECTRICAL CHARACTERISTICS

Nonstandard Video Signals must have the characteristics indicated in Tables 3–6.

Table 3. Non-Standard Video Signal Characteristics

Parameter	Conditions
Sync Amplitude	200 mV minimum
Vertical Pulse Width	3H ±0.5H
Vertical Pulse Tilt	20 mV maximum
H Timing	Phase Step (Head Switch) ±10 µs maximum Fh Deviation (long term) ±0.5% maximum Fh p-p Deviation (short term) ±0.3% maximum
Vertical Sync Signal	The internal sync circuits locks to all 525 or 625 line signals having a vertical sync pulse that meets the following conditions: • It is at least 3H +/– 0.5H wide. • It starts at the proper 2H boundary for its field. • If equalizing pulse serrations are present, they must be less than 0.125H in width.
Minimum Signal-to-Noise	The Z86229 functions down to a 25 dB signal-to-noise ratio (CCIR-weighted) with one error per row or better at that level.
Ratio to Composite Video	Input

Table 4. Horizontal Signal Input

Parameter	Conditions	
Amplitude	CMOS level signal where Low < = 0.2 V_{CC}	
Video-Lock Mode	Polarity Frequency	Any 15,734.263 Hz ±3%
HIN Lock Mode	Polarity Frequency	Any Same as Display Horizontal Flyback Pulse (HFB) pulse

Table 5. Line Input Parameters

Parameter	Conditions
Code Amplitude	50 IRE
Code Zero Level	5 IRE, + 15 IRE relative to Back Porch
Start of Code	10.5 ±0.5 µs (Measure from the midpoint of the leading edge of the composite video Hsync pulse to the midpoint of the rising edge of the first clock run-in cycle.)
Start of the Data	3.972 µs, –0.00 µs, + 0.30 µs (Measure from the midpoint of the falling edge of the most recent clock run-in cycle to the midpoint of the rising edge of the start bit.)
Note: Line 21 must be in its proper position to the leading edge of the Vertical Sync signal.	

ELECTRICAL CHARACTERISTICS (Continued)

Table 6. Timing Signals

Parameter	Conditions
Dot	768 x FH = 12.0839 MHz
Dot Period	82.75 ns
Character Cell Width	1.324 μs (tH/48)
Width of Row (Box)	45.018 µs (34 chars = 17/24 x tH)
Width of Row (Char)	42.370 µs (32 chars = 2/3 x tH)
Horizontal Display Timing	The timing of the output signals Box and RGB have been set to make a centered display. The positioning of these outputs can be adjusted in 330 ns increments by writing a new value to the Z86229 H Position Register (Address = 02h).

PIN DEFINITIONS

Inputs

I^2C SEL (Pin 1). This pin selects 28h for writing and 29h for reading when this input is Low(0). When the input is High(1), the device selects 2Ah for writing and 2Bh for reading.

SEN (Pin 4). This pin enables the signal for the SPI mode of operation on the Serial Control Port. When this pin is Low (0), the SPI port is disabled and the SDO pin is in the high-impedance state. Transitions on the SCK and SDA pins are ignored. SPI mode operation is enabled when SMS is High (1).

HIN (Pin 5). For this pin, the Horizontal Sync input signal at the CMOS level must be supplied. When the device is used in VIDEO-LOCK mode, the signal pulls the on-chip VCO within the proper range. The circuit uses the frequency of this signal, which must be within $\pm 3\%$ F_h, but the overall signal can be of either polarity. When used in the H-lock mode, the VCO phase locks to the rising edge of this signal. The HPOL bit of the H Position register can be set to operate with either polarity of input signal. This signal is usually the H Flyback signal. The timing difference between HIN rising edge and the leading edge of composite sync (of VIDEO input) is one of the factors which affects the horizontal position of the display. Any shift resulting from the timing of this signal can be compensated for with the horizontal timing value in the H Position Register. H-lock is intended for use when the part is generating an OSD display when no video signal is present.

SMS (Pin 6). This pin allows the mode select pin for the Serial Control Port. When this input is at a CMOS High state (1), the Serial Control Port operates in the SPI mode. When the input is Low (0), the Serial Control Port operates in the I^2C slave mode. In SPI mode, the SEN pin must be tied High. (See Reset Operation section.)

VIDEO (Pin 7). This pin is a composite NTSC video input, 1.0V p-p (nom), band limited to 600 kHz. The circuit operates with signal variation between 0.7–1.4V p-p. The polarity is sync tips negative. This signal pin should be AC coupled through a 0.1 µF capacitor, driven by a source impedance of 470 ohms or less.

SCK (Pin 15). This pin is an input for a serial clock signal from the master control device. In I^2C mode operation, the clock rate is expected to be within I^2C limits. In SPI mode, the maximum clock frequency is 10 MHz.

Reset Operation. When the SMS and SEN pins are both in the Low (0) state, the part is in the Reset state; therefore, in the I^2C mode, the SEN pin can be used as an NReset input. When SPI mode is used, if three wire operation is required, both SMS and SEN can be tied together and used as the NReset input. In either mode, NReset must be held Low (0) for at least 100 ns.

Input/Output

V_{IN}/INTRO (Pin 13). In external (EXT) vertical lock mode of operation, the internal vertical sync circuits lock to the V_{IN} input signal applied at this pin. The part locks to the rising or falling edge of the signal in accordance with the setting of the V Polarity command. The default is rising edge. The V_{IN} pulse must be at least 2 lines wide.

In INTRO Mode, when configured for internal vertical synchronization, this pin is an output pin providing an interrupt signal to the master control device in accordance with the settings in the Interrupt Mask Register.

SDA (Pin 14). When the Serial Control Port has been set to I^2C mode operation, this pin serves as the bidirectional data line for sending and receiving serial data. In SPI mode operation, the device operates as a serial data input. SPI mode output data is available on the SDO pin.

Outputs

RED, GREEN, BLUE (Pins 2, 3, 18). These pins are positive-acting CMOS-level signals.

- Color Mode: Red, Green, and Blue characters are incorporated as video outputs for use in a color receiver
- Mono Mode: In this mode, all three outputs carry the character luminance information

Note: The selection of Color/Mono Mode is user controlled in bit D_1 of the Configuration Register (Address=00h). (See Internal Registers section.)

CSync (Pin 8). Sync slice level. A 0.1 µF capacitor must be tied between this pin and analog ground V_{SS}(A). This capacitor stores the sync slice level voltage.

LPF (Pin 9). Loop Filter. A series RC low-pass filter must be tied between this pin and analog ground V_{SS}(A). There must also be second capacitor from the pin to V_{SS}(A).

PIN DEFINITIONS (Continued)

RREF (Pin 10). Reference setting resistor. Resistor must be 10 kOhms, ±2%.

SDO (Pin 16). This pin provides the serial data output when SPI mode communications have been selected. This pin is not used in I^2C mode operation.

BOX (Pin 17). Black box keying output is an active High, CMOS-level signal used to key in the black box for captions/text displays. This output is in a high-impedance state when the background attribute has been set to semi-transparent.

Power Supply

V_{SS} (Pins 11). These pins are the lowest potential power pins for the analog and digital circuits. They are normally tied to system ground.

V_{DD} (Pin 12). The voltage on this pin is nominally 5.0 Volts, and may range between 4.75 to 5.25 Volts with respect to the V_{SS} pins.

Note: The recommended printed circuit pattern for implementing the power connection and critical components is referenced in the Recommended Application Information section on page 49.

Z86229 BLOCK DIAGRAM DESCRIPTION

The Z86229 is designed to process both fields of Line 21 on a television VBI and provide the functional performance of a Line 21 Closed-Caption decoder and Extended Data Service decoder. This device requires two input signals, Composite Video and a horizontal timing signal (HIN), and several passive components for proper operation. A vertical input signal is also required if OSD display mode is required when no video signal is present. The Decoder performs several functions, including extraction of data from Line 21, separation of the normal Line 21 data from the XDS data, on-screen display of the selected data channel, and outputting of the XDS data through the serial communications channel.

Input Signals

The Composite Video input signal is rated at a nominal 1.0 Volt p-p, with sync tips negative and band-limited to 600 kHz. The Z86229 operates with an input level variation of ±3 dB.

The HIN input signal is necessary to bring the VCO close to the required operating frequency. This signal must be a CMOS-level signal. The HIN signal can have positive or negative polarity, and the signal is only required to be within 3% of the standard H frequency. When configured for EXT HLK operation, this signal should correspond to the H Flyback signal.

The timing difference between the HIN rising edge and the leading edge of composite sync (of VIDEO input) is one of the factors that affects the horizontal position of the display. Any shift resulting from the timing of this signal can be compensated for with the horizontal timing value in the H Position register.

Video Input Signal Processing

The Composite Video input is AC-coupled to the device. The sync tip is internally clamped to a fixed reference voltage by means of a dual clamp. Initially, the unlocked signal is clamped using a simple clamp. Improved impulse noise performance is then achieved after the internal sync circuits lock to the incoming signal. Noise rejection is obtained by making the clamp operative only during the sync tip. The clamped composite video signal is fed to both the Data Slicer and Sync Slicer blocks.

The Data Slicer generates a clean CMOS-level data signal by slicing the signal at its midpoint. The slice level is established on an adaptive basis during Line 21. The resulting value is stored until the next occurrence of Line 21. A high level of noise immunity is achieved by using this process.

The Sync Slicer processes the clamped Comp Video signal to extract Comp Sync. This signal is used to lock the internally generated sync to the incoming video when the video-lock mode of operation has been enabled. Sync slicing is performed in two steps. In the non-locked mode, the sync is sliced at a fixed offset level from the sync tip. When proper lock operation has been achieved, the slice level voltage switches from a fixed reference level to an adaptive level. The slice level is stored on the sync slice capacitor (CSYNC).

The Data Clock Recovery circuit operates in conjunction with the Digital H-lock circuit. The circuit produces a 32H clock signal (DCLK) that is locked in phase to the clock run-in burst portion of the sliced data obtained from the Data Slicer. When the Line 21 code appears, the DCLK phase lock is achieved during the clock run-in burst and is used to reclock the sliced data. After phase lock is established it is maintained until a change in the video signal occurs.

The Digital H-Lock circuit produces a variety of signals, including the video timing gates, PG and STG. These signals are all locked in-phase with the HSYNC and the video timing signal, no matter which H-lock mode is used in the display generation circuits. This independent phase lock loop is able to respond quickly to changes in video timing without concern for display stability requirements.

VCO and One Shot

All internal timing and synchronizing signals are derived from the on-board 12-MHz VCO. The VCO output is the DOT CLK signal used to drive both the Horizontal and Vertical counter chains and display timing. The One Shot circuit produces a horizontal timing signal which is derived from the incoming video, and qualified by a Copy Guard logic circuit.

The VCO can be locked in phase to two different sources. For television operation, where a good horizontal display timing signal is available, the VCO is locked to the HIN input through the action of the Phase Detector (PH2). When a proper HIN signal is not available (such as in a VCR), the VCO can be locked to the incoming video through the Phase Detector (PH1). In this case, the frequency detector (FR) circuit is activated (as required) to bring the VCO within the pull-in range of PH1.

Timing and Counting Circuits

The DOT CLK is first divided down to produce the character timing clock CHAR CLK. This signal is then further divided to generate the horizontal timing signals H, 2H and

Z86229 BLOCK DIAGRAM DESCRIPTION (Continued)

HSQR. These timing signals are used in the data output (display) circuits.

The H signal is further divided in the LINE and FLD CNTR to produce the various decodes used to establish vertical lock, time displays, and control functions required for proper operation. The H signal is also used to generate the Smooth Scroll timing signal for display.

The V Lock circuits produce a noise free vertical pulse derived from the horizontal timing signal. When the user selects Video as the vertical lock source, the internal synchronizing signals are phased up with the incoming video by comparing the internally generated vertical pulse to an input vertical pulse. These pulses are derived from the Comp Sync signal provided by the Sync Slicer. In the vertical lock set to V_{IN} mode, the V_{IN} signal is used in place of the signal derived from Comp Sync. In either case, when proper phasing has been established, this circuit outputs the LOCK signal which is used to provide additional noise immunity to the slicing circuits.

The LOCKed state is established only after several successive fields have occurred and the two vertical pulses remain in sync. When LOCKed, the internal timing will flywheel until the timing of the two vertical pulses lose coincidence for a number of consecutive fields. Until LOCK is established, the decoder operates on a pulse-by-pulse basis.

Command Processor

The Command Processor circuit controls the manipulation of the data for storage and display. This circuit processes the Control Port input commands to determine the display status required and the data channel selected. During the display time (lines 43–237), this information is used to control the loading, addressing, clearing of the Display RAM, and the operations of the Character ROM and Output Logic circuits.

During data recovery time (TV lines 21–42), the Command Processor, in conjunction with the data recovery circuits, recovers the XDS data and the data for the selected data channel. Data is sent to the RAM for storage and display and/or to the serial port, as appropriate. Where necessary, the Command Processor converts the input data to the appropriate form.

Output Logic

The Output Logic circuits operate together to generate the output color signals RED, GREEN and BLUE, and the Box signal. When MONOchrome mode is selected, all three color outputs carry the luminance information. These outputs are positive output logic signals.

The character ROM contains the dot pattern for all the characters. The output logic provides the hardware underline, graphics characters, and the Italics slant-generator circuits. The smooth scroll display is achieved by the smooth scroll counter logic, which controls the addressing of the Character ROM.

Decoder Control Circuit

The Decoder Control Circuit block is the users communications port. The circuit converts the information provided to the control port into the necessary internal control signals required to establish the operating mode of the decoder. This port can be operated in one of two serial modes. The SMS pin is used to establish either of the two serial control modes.

In the two wire (I^2C) control mode, the Z86229 responds to its slave address for both the read and write conditions. If the read bit is Low (indicating a WRITE sequence), then the Z86229 responds with an acknowledge. The master should then send an address byte followed by a data byte. If the read bit is High (indicating a READ sequence), then the Z86229 responds with an acknowledge followed by a status byte and a data byte, respectively. Read data, however, is only available through indirect addressing; write addressing exhibits both indirect and direct modes. The busy bit in the status byte indicates whether the write operation has been completed or if read data is available.

The SPI mode is a three wire bus with the Z86229 acting as the slave device. Communication is synchronized by the SCK signal generated by the master. Typically, the serial data output is transmitted on the falling edge of SCK and the received data is captured on the rising edge of SCK. All data is exchanged as 8-bit bytes.

Voltage/Current Reference

The Voltage/Current Reference circuit uses an externally-connected resistor to establish the reference levels that are used throughout the Z86229. For a minimal cost, an external resistor can provide improved internal precision.

Z86229 FUNCTIONAL DESCRIPTION

The Z86229 provides full function NTSC, Line 21 performance. Input commands are included to enable the decoder to process and display any of the eight Caption/Text data channels (CC1, CC2, CC3, CC4, T1, T2, T3 or T4) contained in Line 21 of either field of the incoming video. XDS data can also be selected for the display. The DECODER ON/OFF commands control whether or not the Line 21 data in the selected channel is actually displayed. When switched to the DECODER OFF (TV) state, incoming data in the selected channel is still processed, but not displayed.

The Z86229 can also be configured to operate with PAL or SECAM video signals. The device decodes information encoded into its VBI in Line 22. The encoded data must conform to the waveform and command structure defined for NTSC Line 21 operation.

VCO Lock

The Z86229 includes a VCO with stable gain characteristics and good power supply rejection. The internal horizontal and vertical synchronizing circuits provide a high degree of noise immunity. There are options for both horizontal and vertical lock. The VCO can be phase locked either to the horizontal signal derived from the video input signal (VIDEO) or to the externally supplied HIN signal, typically horizontal flyback.

A HIN lock is used to provide a display having a minimum amount of observable jitter. The low jitter requires a HIN signal derived from a TV display that exhibits proper polarity. This type of signal is readily available in a television receiver. Video-Lock mode enables the VCO to lock in-phase to the incoming video signal, thus providing good operation in an application where no display-related HIN signal is available (such as in a VCR).

Video Timing

Timing signals are derived from the VCO for use in the line counting and display circuits. Line counting requires proper identification of the input signal's vertical pulse. Default operation uses the vertical sync signal derived from the video input signal as the source for vertical lock. This method results in locking characteristics having good performance and good noise immunity.

In the event that OSD operation is required under conditions when no input video is present, it would be necessary to set the Z86229 for V_{IN} lock. In this mode, the vertical timing is determined from the vertical pulse signal supplied to the V_{IN} pin.

The horizontal position of the caption display is determined by the internal timing circuits. A default condition has been established that should result in a well centered display in a typical application; however, signal delays through video-processing circuits can vary between designs. The Z86229 provides the user with the ability to change the default timing. No matter which of the horizontal lock modes are selected, the display horizontal position on the screen can be adjusted in quarter character (330 ns) steps by serial port commands.

Displayable Character Set

Normal Mode. Characters are displayed as white or colored dot matrix characters on an opaque background. The Box is normally black, but the Z86229 can be set to a blue background Box with a serial command. The characters are described by a 12 by 18 dot pattern within a character cell which is 16 dots wide by 26 dots high per frame. The location of the character luminance within the character cell varies from character to character to allow for the display of lower case letters with descenders. All characters have at least a 1-dot border of black around each character. Underline is also provided. Figure 4 illustrates the Z86229 standard character map and font.

The character ROM consists of a 12 by 18 dot matrix pattern per character. Alternate rows and columns are read out in each field to produce an interleaved and rounded character. A display row contains a maximum of 32 characters plus a leading and trailing black box, each a character cell in width, making the overall width of a display row 34 x 8 = 272 dots. Successive display rows are butted together so that the total display occupies 195 dots high.

The black box is 34 character cells wide by 195 dots high, resulting in a box size of 45.018 µs in width by 195 scan lines in height. The Box starts in scan line 43 and extends to scan line 237. Theoretically, the display is horizontally centered in the video display when the Box starts 13.2 µs after the leading edge of H.

The default setting of the Z86229 places the center of the Box at about 13.5 µs to allow for some delay in the normal video path. However, the Box horizontal position can be adjusted by the user in 330 ns increments. The display is approximately within the safe title area for NTSC receivers. Character width is 42.37 µs, also centered on the screen, resulting in a leading and trailing 1.32 µs black border.

An optional Caption display mode, Drop Shadow, can be selected by the user through the serial port. This display mode eliminates the black box around the characters, placing a 2-dot black shadow to the right and below the character luminance dots when the 15 scan line per row mode is active. This display mode is usable in Captions, Text, and

Z86229 FUNCTIONAL DESCRIPTION (Continued)

OSD displays. Figure 5 illustrates the characters with a drop-shadow added.

Extended Features

The EIA–608 specification has defined new extended features such as optional Background and Foreground display attributes and optional Extended Characters. The Z86229 always responds to the Extended Characters, but the Extended Background/Foreground response can be controlled by the user. The Background and Foreground attributes add codes for background colors, black and transparent foreground, opaque, and semi-transparent backgrounds. The BOX signal output pin is set to a tri-state condition whenever one of the semi-transparent attribute codes is active. The external keying circuits can then use this condition to implement the intended video display.

The font for the Extended Characters are illustrated in Figure 6. The accented capital letters have been implemented by placing the accent marks above the character cell. When selected, this mode results in the accent marks being written into the character cell space of the row above. In some operating modes, the Z86229 expands the size of the overall box height by adding two additional scan lines at the top and one additional line at the bottom. There is now room for the accent marks in the topmost row and an added black line below the descenders of any lowercase characters in the last row.

This approach is desirable because shrinking the capitals to make room for the accent mark within the character cell makes poor quality characters. In some cases, there would be no differentiation between the capital and lower case letter. Extended characters also have the advantage of minimizing the ROM size and providing a good readable font that closely matches what is normally seen in print.

In the unlikely case of a conflict between an accented capital letter in one row and a lower case descender in the same character position in the row above, the descender is given priority. The improved readability of this approach over shrunk capital letters far outweighs this potential conflict and results in a cost-effective compromise for providing a full, extended features implementation.

The Extended Characters share their address space with the OSD Graphics Characters. When a BOX display is used, the Extended Character set is in force; however, if a Drop Shadow display is used, the Graphics Characters are in force. For Caption and Text display modes, if the Drop Shadow is set, the user must also command the Z86229 to switch back to Extended Characters.

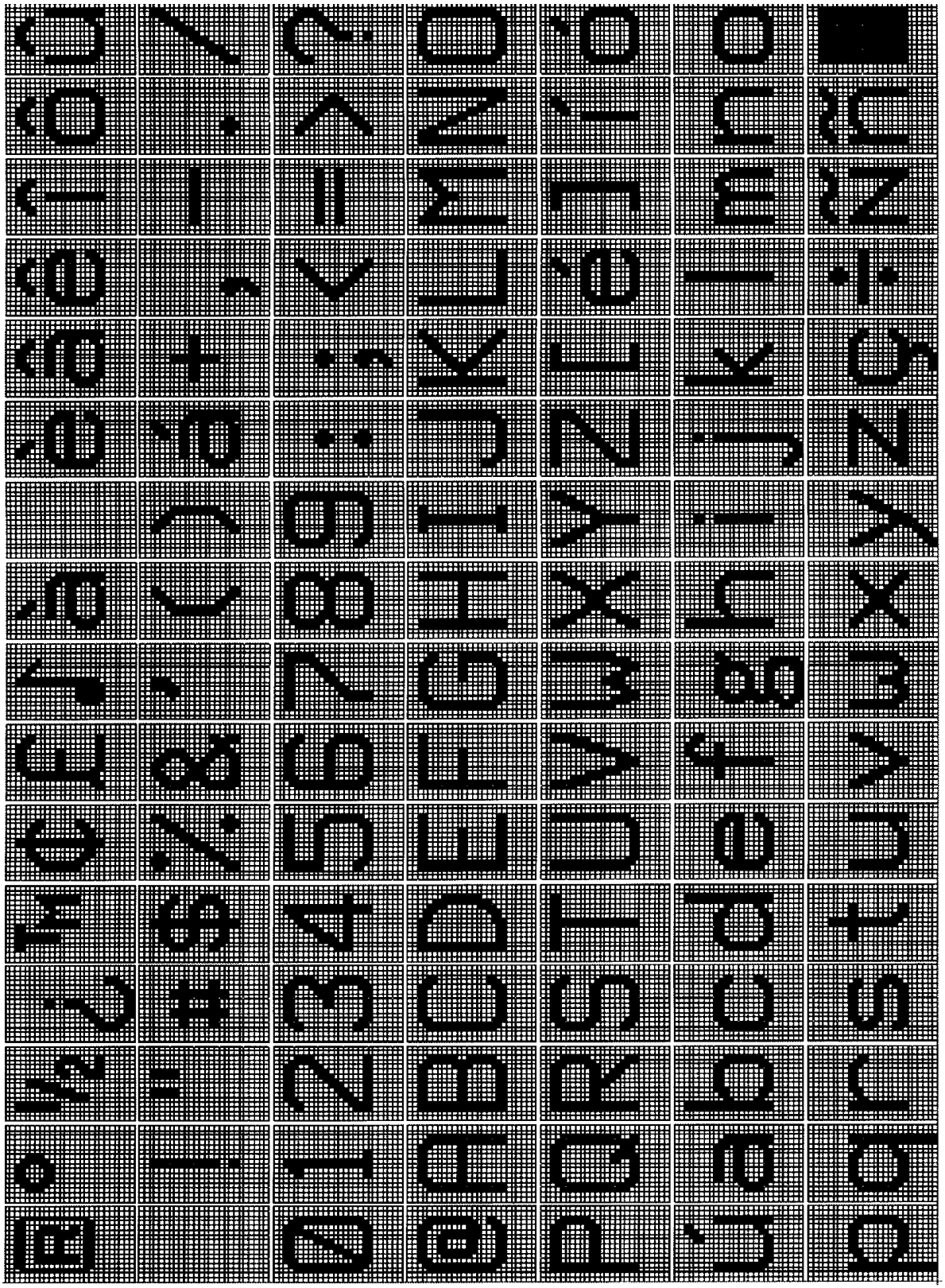


Figure 4. Z86229 Standard Character Map and Font

Z86229 FUNCTIONAL DESCRIPTION (Continued)

Figure 5. Caption Display Mode, Drop Shadow

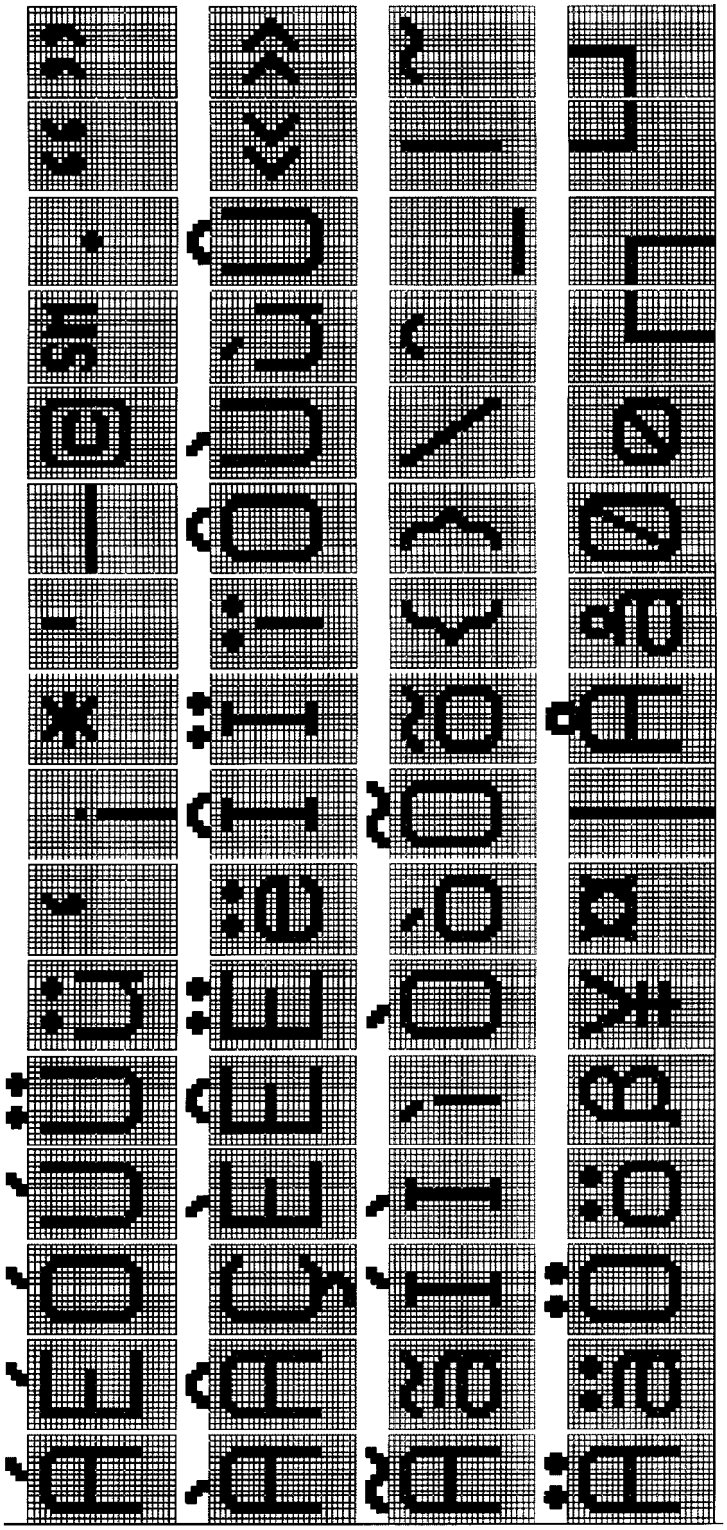


Figure 6. Extended Characters Font

Z86229 FUNCTIONAL DESCRIPTION (Continued)

Text Mode Display

When the Text mode is selected, a black box is displayed as long as a valid Line 21 code in the specified field is being detected. The Z86229 provides the option to make the box blue instead of black. This option holds for captions and text.

The default Text display mode uses a 15 row by 34 character black box. Text characters are displayed as they are received starting at the top row. Successive carriage returns move the display down successive rows until all 15 rows have been displayed. Thereafter, the text scrolls up as new characters are added to the bottom row.

If the data for the selected channel is interrupted by a command for another channel, data processing stops; however, the display remains. When a Resume Text command is received, data processing resumes and the new characters are added.

Note: The data processing begins at the position that the display row/column pointer was in at the interruption of data processing.

If a Start Text command is received, the display is cleared, and the new characters are displayed starting in row 1, column 1 (left side).

The number of display rows and the location (base row) of the Text box can be altered by the user. In this way, the user can decide how much of the screen can be covered when displaying non-program related information.

When scrolling, the display shifts one scan line per frame until a complete row has been scrolled. If a carriage return is received before scrolling is complete, the display immediately completes the "scroll" by jumping up the remaining scan lines and starting the display of the new text.

Caption Display Mode

According to FCC specifications, caption data can appear in any of the 15 display rows, but a single caption may consist of no more than 4 rows. The form of the caption display depends on the caption mode indicated by the transmitted caption command, Pop-on, Paint-on, or Roll-up. The Z86229 can display a single caption having as many as eight rows. When any of the caption display modes are selected, the screen becomes transparent

Note: Display box is only present when a caption is being displayed.

Pop-on captions work with two caption memories. One of them is normally displayed while the other is being used to accumulate new caption data. A new caption is popped-on by swapping the two memories with the End Of Caption (EOC) command. When the on-screen memory is erased, the screen is blank (transparent), and the memory defaults to the row/column pointer at row 1, column 1, and monochrome are non-underlined.

When caption mode is selected, the decoder processes data following the Resume Caption Loading (RCL) command (or the EOC). Normally, this command is followed by a Preamble Address Code (PAC) to indicate the row, column, and character attributes to be used with the following data. If no PAC is received, the data is added to the location most recently indicated by the row/column pointer prior to the receipt of the RCL command.

The Paint-on caption mode is essentially equivalent to the Pop-on mode; however, the data received after the Resume Direct Captioning (RDC) command is written to the on-screen memory rather than the off-screen memory. All the rules for PACs, Midcodes, and so on, are otherwise the same.

The Roll-up caption mode presents a "text" like display that is limited to 2, 3, or 4 rows, depending on the Resume Roll-up (RUn) command used. The PAC following the RUn command is used as the BASE ROW for the ROLL-UP display. The BASE ROW is the "bottom" row of the ROLL-UP display. In this case, the black box does not appear until characters are being displayed, and the Box is only wide enough to provide a leading and trailing box in each line. The new data appears in the bottom row, and as each carriage return is received, the row scrolls up and the new data is added to the bottom. When the number of rows indicated by the Resume command have been reached, the data in the top row scrolls off as new data is added to the bottom.

The TAB (INDENT) PAC permits placing captions starting at 4 character boundaries in any caption row. The TAB OFFSET command provides the means for adjusting the starting position for a caption at any column position in the current row.

XDS Display Modes

Two preprogrammed XDS display modes are provided. One provides information about the current program that would be of interest for "channel grazing". The second display shows the grazing packets, plus additional XDS packets which informs the viewer about the program content. Information is displayed as it is received. The displays use a drop-shadow mode with 15 scan lines per row.

The XDSG mode is the GRAZE (channel grazing) display (Figure 7). The display contains three rows of information at the top of the screen that have been formatted for easy reading. They contain the following XDS packet information:

OSD Row 1	Network Name, Call Letters (Green)
OSD Row 2	Program Name (Italics, Underline, White)
OSD Row 3	Program Length, Time In Show (Cyan)

When an XDS display mode has been selected, the information is displayed as the appropriate packets are received. The display remains on-screen as long as valid XDS data continues to be received. If the 16-Second Erase Timer is enabled (the default condition), the XDS display is erased when no valid XDS data has been received for 16 Seconds. If subsequent XDS data is received with displayable packets, that information reappears on the screen. XDS data recovery can be active in the XDS display mode.

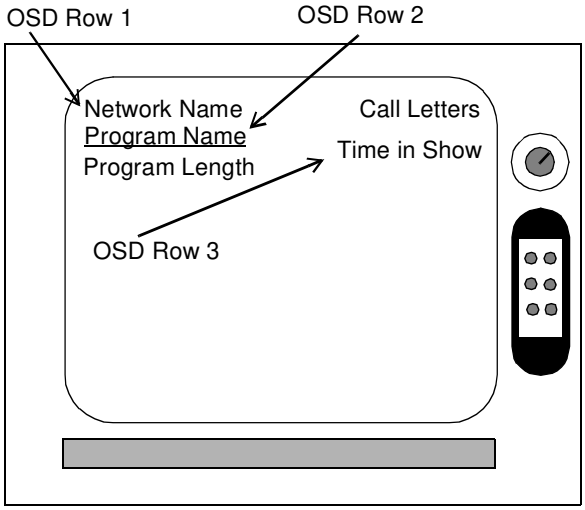


Figure 7. XDSG (Graze) Mode Sample Display

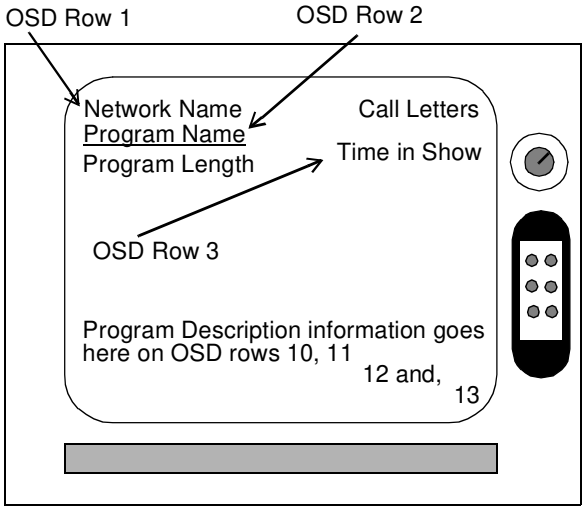


Figure 8. XDSF Mode Sample Display

The XDSF mode is the FULL (information) display (Figure 8). This display shows the same information as the GRAZE display; however, this display adds the program type as well the first four program description rows (if transmitted). Although XDS defines eight program description rows, the first four are identified as containing the most important information. The display of Program Description is limited to the first four rows. This limitation occurs because:

1. Eight rows would obscure much of the screen.
2. More than four rows are not likely to be sent due to the time required for transmission.

Because 15 scan lines per row mode are being used, rows 10–13 appear at the bottom of the screen.

OSD Row 1	Network Name, Call Letters (Green)
OSD Row 2	Program Name (Italics, Underline, White)
OSD Row 3	Program Length, Program Type, Time In Show (Cyan)
OSD Row 10	Program Description Row 1 (Yellow)
OSD Row 11	Program Description Row 2 (Yellow)
OSD Row 12	Program Description Row 3 (Yellow)
OSD Row 13	Program Description Row 4 (Yellow)

The XDS display mode is turned off by selecting a different display mode.

Display Erase and Autoblanking

The display is erased in the Text mode by the Start Text command (but the box is maintained) and in the CAPTION mode by the Erase Displayed Memory (EDM) command. The non-displayed memory can be erased by the Erase Non-displayed Memory (ENM) command.

Four other events can also cause the display to be erased.

1. The first action is a change in the display mode, such as from CC1 to T1 or CC1 to XDSF. A change in display mode clears the memory and the display.
2. A loss of video lock, such as on a channel change, can cause the screen to be cleared. The current active display mode is not changed. For example, if CC1 is selected and ON before the channel change, the device will remain in the CC1/ON state after the channel change.
3. The third action that clears the displayed memory is when the autoblanking circuit is activated. The autoblanking circuit monitors the presence of a Line

Z86229 FUNCTIONAL DESCRIPTION (Continued)

21 waveform in the video field corresponding to the data channel selected for display. The decoder is held in the Decoder OFF (TV) state until a Line 21 waveform is continuously detected for a period of 0.5 seconds. After a valid Line 21 waveform has been detected for 0.5 seconds, and assuming that the user has selected the Decoder ON state, the normal display for the data channel selected is presented. The autoblanking circuit is not activated again until a valid Line 21 waveform has been lost for 1.5 seconds. Any data received during the 1.5-second period resets the counter. As a result, autoblanking is only activated on continuous loss of the Line 21 waveform for 1.5 seconds.

Note: A valid Line 21 waveform is defined as the presence of a 7-cycle run-in clock, in addition to a start bit on Line 21 of the field being examined.

4. The fourth method of clearing the screen is by the action of the 16-Second Erase Timer. This function is only active when a CAPTION or XDS display mode has been selected. If no data is received for the display channel selected for a 16-Second period, the on-screen memory is erased; however, the decoder is still on the selected channel (with the decoder ON), allowing data for the selected channel to be displayed.

Z86229 FEATURE SET

The primary features of the Z86229 are summarized below. More complete descriptions can be found in later sections of this document.

VBI Data Processing

The Z86229 extracts Line 21 data from the incoming video signal. All data channels in both video fields are supported. Incorporating the VBI decoding feature, the Z86229 can perform the following:

- Process data from both fields of Line 21 simultaneously
- Output XDS data through the serial port while displaying selected data
- Output XDS data through the serial port raw or filtered
- Select XDS filters from a list of pre-programmed values including Program Rating and Time of Day/Local Time
- Select NTSC or PAL operation

The video data extracted from Line 21 may be displayed in different ways according to the user selection and the type of data. Display choices include:

- Ten different Line 21 data-display modes; CC1–CC4 and T1–T4, plus two standard templates for XDS displays
- Pop-on, Paint-on, and Roll-up CAPTION displays
- Text display default as a full screen, 15 row display
- User can vertically reduce and reposition the Text display as required
- Color or Monochrome display mode selectable
- XDSG Display Mode (channel grazing): automatic display of Network Name, Call Letters, Program Name, Program Length, and Time In Show data packets
- XDSF Display Mode (full information): automatic display of XDSG Display Mode information in addition to Program Type (only basic types) and Program Description

General Purpose OSD Modes

Apart from displaying data extracted from Line 21 of the incoming video, the Z86229 can also display information supplied through its serial port. This condition is referred to as On-Screen Display (OSD) mode. This mode provides:

- Programmable Full Screen OSD: 15 display rows by 32 character columns
- Graphics characters
- Double-High and Double-Wide characters
- Fully programmable display positioning (information may be placed anywhere on the screen)
- Accepts externally supplied (or internally generated VSYNC to enable OSD even when no video is present)

Character Set

The Z86229 has a new character set with extended features, such as:

- New font with descenders on lower case letters
- Optional display mode using the drop-shadow font (in other words, fringing appears on each character rather than a solid, “black box” background)
- EIA–608 Extended Characters
- EIA–608 Background and Foreground attributes
- Special framing and graphics characters for OSD display
- Double-High and Double-Wide character display for OSD
- Fifteen scan lines per character row for OSD and Text

Note: Contact the nearest ZiLOG Sales office for additional information on how to define your own custom OSD character set.

Serial Communications Interface

Communications and control of the Z86229 is possible through a serial control interface. Two Serial Control Modes are available with the Z86229 performing as a slave device. These modes are:

1. A two wire, I^2C interface.
2. A three wire, Serial Peripheral Interface (SPI).

A total of five device pins are dedicated to the serial control port function. These pins are indicated in Table 7.

Z86229 FEATURE SET (Continued)

Table 7. Z86229 Serial Control Signals

Signal	SMS	SCK	SDA	SDO	SEN
Pin #	6	15	14	16	4
I/O	I	I	I/O	O	I
I^2C	0	CLK	Data	NA	1
SPI	1	CLK	Data In	Data Out	Enable

Notes:
SMS = Serial Mode Select High = SPI and Low = I^2C.
SCK = Serial port clock for either Serial Mode.
SDA = Serial port data for I^2C Mode and Data In for SPI Mode.
SDO = Serial Data Out for SPI Mode. Not used in I^2C Mode.
SEN = SPI Mode Enable signal. Must be High for I^2C Mode.

I^2C Mode. The I^2C port on the Z86229 always acts as a slave device. I^2C Mode is selected by bringing the SMS pin Low and the SEN pin High. SEN must remain High whenever I^2C mode is required. If the SEN pin is brought Low, with the SMS also Low, the part is reset. SDA and SCK are the data and clock lines of the I^2C port, respectively. During I^2C mode operation, the V_{IN}/INTRO signal (pin 13), can be configured to generate interrupt requests to the master device on selected events (see Note paragraph page 22).

SPI Mode. SPI Mode is selected by making the SMS pin High. In SPI mode, the Z86229 acts as a slave device. All communications are clocked in and out as 8-bit bytes. SCK is the serial clock (input), SDA is Data-In, and SDO is Data-Out. The SEN pin enables communication when High. When Low, the SDO pin is tri-stated.

When SEN is brought High, the part is synchronized and waiting for a Command. If SEN is tied High, the part can also be synchronized by a command string. During SPI mode operation, the V_{IN}/INTRO signal (pin 13) can be configured to generate interrupt requests to the master device on selected events

Caution: When the SEN and SMS pins are made Low simultaneously, the part is reset.

Interrupt Generation. The V_{IN}/INTRO signal (pin 13) can be configured to provide an interrupt output on selected events. The configuration of V_{IN}/INTRO (pin 13) is user programmable to be either:

1. An INPUT pin for acceptance of an external VSYNC timing signal.
2. An OUTPUT pin for interrupt generation on selected events.

Note: Configuring V_{IN}/INTRO as an output for interrupt generation is particularly useful when implementing the Program Blocking feature with the Z86229 in TVs and VCRs. In this configuration, Pin 13 is used to interrupt the host processor when the XDS Program Rating data packet is found. As a result, the host processor is not burdened with monitoring or filtering the line 21 data stream. The Z86229 filters the Line 21 data stream for the host processor, and generates an interrupt only when the required packet is found.

Setup and Operational Control

The Z86229 is extremely flexible and fully programmable through its serial communication port. The following tables provide a partial list of User-Programmable Features, User Selectable Display Modes, and Default Conditions upon Reset.

Z86229 Programmable Features

- Decoder ON/OFF
- TV scan lines per OSD row (13 or 15 lines)
- EIA–608 extended attributes ON/OFF
- OSD drop shadow ON/OFF
- Color/Monochrome
- OSD Horizontal start position
- Text box size (# of rows)
- Text box starting row position
- NTSC or PAL
- Vertical Lock Source: Video or External V_{IN}
- XDS Data Output, Raw or Filtered
- H-lock Source: Video or External HIN

In addition to the programmable features just listed, the Z86229 offers a choice of eleven display modes for user selection.

Table 8. Z86229 Display Modes

Display Mode	Display Data	NTSC Field[1]	Language[2]
CC1	L21 Closed Captions	1	I
CC2	L21 Closed Captions	1	II
CC3	L21 Closed Captions	2	I
CC4	L21 Closed Captions	2	II
T1	L21 Text	1	I
T2	L21 Text	1	II
T3	L21 Text	2	I
T4	L21 Text	2	II
XDSF	XDS	2	N/A
XDSG	XDS	2	N/A
OSD	User Defined via Serial Port	N/A	N/A

Notes:
1. In NTSC-interlaced mode, there are two fields, or horizontal pixel-display lines, exhibiting alternate refreshes to the display.
2. Language I refers to synchronous captioning, and language II refers to supplementary captioning.

The Z86229 is initialized on RESET to the following default conditions:

Table 9. RESET Default Conditions

Parameter	Reset Condition
Display Channel	CC1
Decoder	OFF
Text Size	15 rows
Lines/Row	13
Background	BOX
EIA–608 Extended Attributes	ON
Data Outputs	OFF
Video Standard	NTSC
Data Outputs	OFF
VCO Lock	Video
BOX Timing	13.5 μsec
Vertical Lock	Video
V_{IN}/INTRO	INTRO & Disabled
Horizontal Lock	Video
Color/Mono	Color
OSD Display	Drop Shadow 15 lines/row

SERIAL COMMUNICATIONS INTERFACE

Commands and data are sent to and from the Z86229 through its serial communications interface. Two Serial Control Modes are available. One mode is a two wire I^2C bus interface. The other serial mode is a three wire, synchronous serial peripheral interface (SPI). In both cases, the Z86229 acts as a slave device.

The serial communications port is the path for setting the configuration and operational modes of the device. It is also the port for outputting the recovered XDS data and for inputting the OSD data for display.

When the Vertical Lock = VIDEO, the V_{IN}/INTRO (pin13) is configured as an output, providing the INTRO signal. This interrupt operation is available in either serial control mode.

The Z86229 is able to generate an interrupt on the occurrence of any set of specified events. The master device clears the interrupt by writing to the Interrupt Request Register.

I^2C Bus Operation

The serial control mode in use is selected by the state of the SMS pin. When SMS is set Low, the Z86229 is in the I^2C mode. In this mode, the Z86229 also supports a bidirectional two wire bus and data transmission protocol. The bus is controlled by the master device, which generates the serial clock (SCK), controls the bus access, and generates the Start and Stop conditions. The SDA pin is the bidirectional data line. In this mode, the SDO output is not used, and the pin is in its high-impedance state.

The Z86229 can receive or transmit data under the control of a master device. Remember that the Z86229 is a slave device. Communication is initiated when the master device sends the start condition followed by the Z86229 Slave Address Read byte (29h or 2Bh) or Slave Address Write byte (28h or 2Ah). The Z86229 responds with an Acknowledge. The I^2C RD/nWR bit is the Least Significant Bit (LSB) of the I^2C addresses (Table 10).

Table 10. Z8612 I^2C Slave Addresses*

	READ	WRITE
1st I^2C Address	29h	28h
2nd I^2C Address	2Bh	2Ah

Note: *When the SMS and SEN pins are both Low, the part is in the Reset state. Therefore, the SEN pin can be used to reset the part while in the I^2C mode. The SEN pin may be tied to a NReset signal or tied High if no reset is required. The I^2C Address is selected by pin 1 input. When pin 1 input is Low(0), it selects the 1st address. When pin 1 input is High(1), it selects the second address.

The I^2C Bus Protocol

Under the I^2C bus protocol, the following conditions must be present:

1. Data transfer can only be started when the bus is not busy.
2. During data transfer, data transitions must not occur while the clock is High.

Bus Conditions are Defined as:

Not Busy. Data and Clock lines are both High.

Start. A High to Low transition of an SDA line while the SCK line is High.

Stop. A Low to High transition of an SDA line while the SCK line is High.

Acknowledge. When addressed, the receiving device must output an acknowledge after the reception of each byte. The master device must generate the clock for the acknowledge bit. Acknowledge is SDA=Low. A Not ACKnowledge result (NACK) is SDA=High.

Data. The data (SDA) is output by the transmitting device on the falling edge of SCK, MSB first. The receiving device reads the data, MSB first, on the rising edge of SCK.

Communication with the Z86229 is initiated when the master device sends the Z86229 slave address following a start condition. The Z86229 has a single preset, consisting of a seven-bit slave address. The Z86229 responds with an acknowledge. The eighth bit of the slave address is driven High for Read operations and Low for Write operations.

Writing to the I^2C Bus

All write commands are either one- or two-byte commands. The Z86229 is enabled when a Start condition, followed by its Slave Address Write byte, is received. The Start condition is disabled when it deems the command to have been completed, or when a Stop condition occurs. A new Start condition without a Stop condition begins a new sequence. Therefore, successive commands may be executed by successive strings of "Start—Slave Address—Command" sequences without any intervening Stop condition being sent.

Note: The number of data bytes to be received by the Z86229 is inherent in the command. The Z86229 responds with the acknowledge signal only for the number of bytes expected. If the master writes more bytes than expected, there is no acknowledge for the extra bytes.

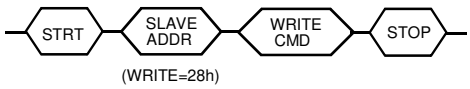
A write command to the Z86229 should always be preceded by executing a Status read to verify that the Z86229 is not busy. The Status register data is output immediately following the reception of the Slave Address Read. If the RDY bit is set, the master device can initiate its write sequence, always beginning with the Start condition. The first byte of a two-byte command is always written first.

An example of the master's sequence for writing a two-byte command (after RDY had been checked) would be:

Start
Slave Address Write/Slave ACK
CMD (master)/ Slave ACK
DATA (master)/Slave ACK
Stop

I2CTwo-Byte Write (Command & Data)

I2C One-Byte Write (Command)



Note: A Status Register RDY bit must be read and checked prior to the STRT condition of either WRITE sequence above. See the One-Byte Read (Status Only) in Figure 10 for more information on reading the Status Register.

Figure 9. I2C Bus WRITE (Command)

Reading Data Using the I2C Bus

With the exception of the Serial Status (SS) register, which may be read at any time, each read operation must be set up before the data can be read from the serial output registers of the Z86229. Data is set up for a read operation either automatically or manually. The XDS data reads are set up automatically upon recovery by setting a valid XDS FILTER register selection. All other data read operations must be set up manually using the READ SELECT commands RDS1 and RDS2. These commands load the selected data byte or pair of bytes into the serial output register(s), setting the SS register RD2 bit according to the number of data bytes requested. The SS register DAV bit is also set at that time to indicate the availability of data.

The Z86229 I2C Bus supports one-, two-, and three-byte read sequences. All read sequences output the SS register as the first output byte. If the serial status DAV bit is set, a two or three byte read sequence can then be initiated, beginning with a new STRT condition.

Caution: If the DAV bit is not set, the I2C master device should not attempt to read any data bytes. Attempting to read data bytes from the I2C master device may cause a loss of data from the Z86229 output registers.

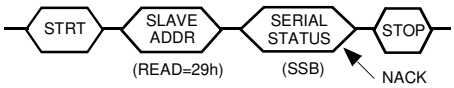
The number of data bytes available is indicated by the state of the RD2 bit of the serial status. In a typical read operation, the status byte is read, and the DAV and RD2 bits are examined. If one or two data bytes are available, the data is read in sequence, separated by acknowledges.

Note: In all I2C Read operations (one, two, and three byte as defined in Figure 10) the most recent byte read from the Z86229 should be acknowledged by the master with a NACK (Not ACKnowledge). It is also necessary to read all available data in a read operation to clear the DAV bit and permit subsequent reads. The DAV is cleared by the master clocking out of the eighth bit of the most recent data-byte read. The DAV is never cleared by just reading the SSB (one-byte read) alone. All data is first output as MSB.

The slave's sequence for reading two data bytes (total of three bytes including SSB) from the Z86229 is given as:

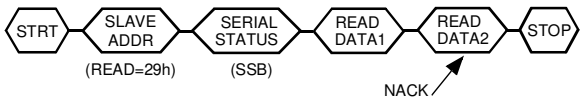
Start
Slave Address Read/Slave ACK
SS Byte/Master ACK
Byte (slave)/Master ACK
Byte (slave)/Master NACK
Stop

I2C One-Byte Read (Status Only)



I2C Two-Byte Read (Status & Data1)

I2C Three-Byte Read (Status, Data1, & Data2)



Note: In all I2C Read operations defined herein, the last byte read from the Z86229 must be acknowledged by the master with a NACK (Not ACKnowledge).

Figure 10. I2C Bus READ (Command)

SERIAL COMMUNICATIONS INTERFACE (Continued)

Clock and Data Transitions. The SCK and SDA bus lines are normally pulled High with a resistor. Data on the SDA bus may only change during SCK Low time periods. Data changes during SCK High periods indicate a start or stop condition (Table 11) defined as:

Start Condition. A High-to-Low transition of SDA, with a SCK High as a start condition which must precede any other command.

Stop Condition. A Low-to-High transition of SDA, with a SCK High as a stop condition which terminates all communications.

Acknowledge. All address and data words are serially transmitted to and from the Z86229 in eight-bit words. The instance of a ninth bit generates an acknowledge. The device acknowledges the data by pulling the SDA bus Low during the ninth bit. A Not AC-Knowledge (NACK) is given by SDA=High during the ninth clock time.

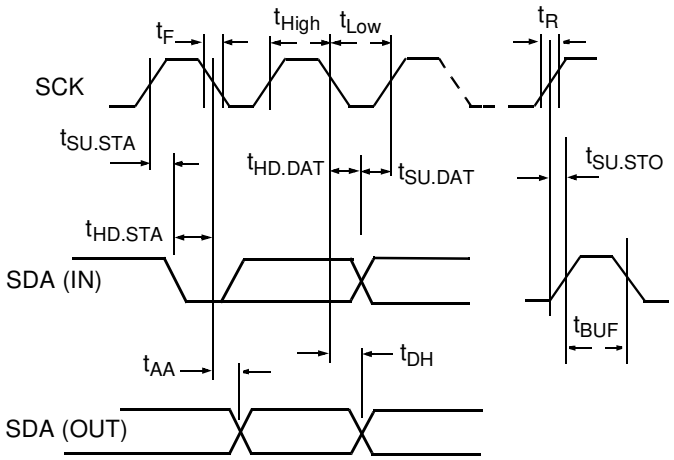


Figure 11. I^2C Serial Timing

Table 11. I^2C Serial Timing Min/Max

Symbol	Parameter	Min	Max	Units
f_{SCK}	Clock Frequency		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7	–	µs
t_{High}	Clock Pulse Width High	4.0	–	µs
t_R	SDA and SCL Rise Time	–	1.0	µs
t_F	SDA and SCL Fall Time	–	300	ns
t_{AA}	Clock Low to Data Out Valid	0.1	3.5	µs
t_{BUF}	Bus Free Time	4.7	–	µs
$t_{HD.STA}$	Start Hold Time	4.0	–	µs
$t_{SU.STA}$	Start Set-up Time	4.7	–	µs
$t_{HD.DAT}$	Data In Hold Time	0	–	µs
$t_{SU.DAT}$	Data In Set-up Time	250	–	ns
$t_{SU.STO}$	Stop Set-up Time	4.7	–	µs
t_{DH}	Data Out Hold Time	100	–	ns
t_I	Input Filter Time Constant		100	ns

SPI Bus Operation

When the SMS pin is High, the Z86229 is in the SPI serial control mode. The clock line should be tied to the SCK pin. The DATA IN signal and DATA OUT signal from the master device should be connected to the SDA and SDO pins, respectively. The SEN pin is used to select the Z86229 when there are multiple peripherals on the bus.

As noted above, when both the SMS and SEN pins are Low, the part is in the RESET state. When the SPI bus is used in a dedicated fashion between the master and the Z86229, both the SEN and SMS pins would be tied High. The RESET function would require that both of these pins be tied to the NReset signal. To ensure synchronization, the master device should send the serial synchronization signal after the reset is released.

When the SPI mode is used in a multiple peripheral environment, the SEN pin is used as the Z86229 enable signal. The SMS could then be used for the NReset signal as long as the reset was only applied while SEN is Low. In this case, there would be no requirement for the master device to send a serial synchronization string after reset if there was at least 100 ns between the end of the reset and the start of the port enable.

A command string can be interrupted at any time. The port is resynchronized by sending the Serial Sync signal or by activating the rising edge of SEN.

The SPI bus is a three-wire bus when used in a dedicated manner between the Z86229 and the master device. If other peripherals are connected to the bus, then the SEN pin must be used to place this device on the bus at the appropriate time. When SEN is Low, the SDO pin becomes tri-stated, transitioning on the SCK and SDA pins, which, as a result, are ignored.

If data output is not required from the Z86229, then control can be accomplished using only the SCK and SDA pins. Because this type of operation precludes the ability to check the RDY bit, it is very important that commands be spaced by at least two frames (66 msec) to ensure that one command has been executed before initiating another.

The bus is controlled by the master device, which generates the serial clock (SCK) and initiates all actions. Clocking data in on the SDA simultaneously produces a data out on the SDO. The master should always check for the appropriate handshake signal before executing any command other than a NOP.

Writing to the part requires that the RDY bit be set, while reading from the part requires checking the SS register to see if the DAV bit is set. Both of these bits are contained in the Serial Status (SS) register. Writing to the Z86229 concurrently outputs the contents of the SS register, MSB first, unless other data is being output as a result of one of the READ commands. If it is required to read the SS without executing a command, the NOP command can be written at any time, even if the serial status RDY bit is not set.

The RDY status bit is driven onto the SDO pin between command transmissions. The controlling MCU can test the state of this pin, without clocking, in order to determine if subsequent serial transfers are possible. The DAV bit can only be checked by outputting the contents of the SS register.

Writing to the SPI Bus

All write commands are either one or two-byte commands. The number of data bytes to be received by the Z86229 is inherent in the command. If the master device writes more bytes than expected, the command may be overwritten or corrupted by the extraneous bytes.

A write to the Z86229 should always be preceded by executing a Status read to verify that the device is ready. The serial status is output by the device, concurrent with the input of any command byte. If the RDY bit of the serial status register is set, the master device can write a new command.

The command and data bytes are written MSB first. Typically, the first byte of a two-byte command is sent first. The bits are clocked into the Z86229 by placing the data on the SDA input and bringing the SCK High.

Reading Data Using the SPI Bus

With the exception of the SS read, each read operation must be set up before the data can actually be read from the serial output registers of the device. Data is set up for a read operation either automatically or manually. The XDS data is set up for a READ automatically upon recovery by setting a valid XDS FILTER register selection. All other data read operations must be set up manually, using the READ SELECT commands RDS1 and RDS2. These commands load the selected data byte(or pair of bytes) into the serial output registers, set the SS register RD2 bit according to the number of data bytes requested, and set the serial status DAV bit to indicate the availability of data.

The Z86229 SPI Bus supports two and three byte read sequences. In SPI mode, the SS must be read before a read sequence is started, so that the DAV and RD2 bits can be checked. The number of data bytes available is indicated by the state of the RD2 bit. The special command, READ1 or READ2, is then used to read the one or two available data bytes. The serial status is clocked out during the write of the READ1 or READ2 command. The data byte or bytes are then clocked-out in sequence, MSB first, while the NOP commands are written into the device. Data bits are clocked-out on the rising edge of SCK. All available data bytes must be read to clear the DAV bit and permit subsequent reads.

The SPI Bus Protocol

The SPI Bus Protocol is defined as follows:

1. The first bit of the first output byte is driven out on the SDO. This action is followed by the rising edge of SCK on the last bit (LSB) of the READ1 or READ2 command.
2. A three-wire bus is defined with a Clock signal on the SCK pin, a Serial Data Input on the SDA pin, and a Serial Data Output on the SDO pin.
3. The SEN pin Low disables the port, placing the SDO pin in a tri-state. Signal transitions on SCK and SDA are ignored.
4. The SEN pin High enables the port for operation.
5. The SEN and SMS pins Low indicate a hardware reset for the part. These pins must be held Low for at least 100 ns.
6. Serial synchronization can be established by clocking in the minimum required SSR string of FFh, FFh, FEh. More than two bytes of FFh may be input, but the string must end with FEh.