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ZiLOG

Totally Logical

Z86230

ADVANCED PROGRAM BLOCKING AND NTSC LINE 21 XDS DECODER

PRELIMINARY PRODUCT SPECIFICATION

PS000401-TVC0699

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1. ARCHITECTURAL OVERVIEW

The Z86230 is a stand-alone integrated circuit, capable of processing Extended Data Services (XDS) in Field 2 of the Vertical Blanking Interval (VBI) of a video frame. This device conforms to the transmission format defined in the Television Decoder Circuits Act of 1990, in accordance with the Electronics Industry Association specification EIA-608A and EIA-744A.

The XDS data is processed to provide either a Program Blocking signal (PB) or a recovered XDS data packet. The PB matches the contents of the recovered Content Advisory packet to the user selections input on the decoder. On-chip XDS filters in the Z86230 are fully-programmable, enabling recovery of only those XDS data packets selected for use in TVs, VCRs, and Set-Top boxes.

In addition, the Z86230 is ideally suited to monitor Picture-In-Picture (PiP) window video for violence blocking and other XDS data services.

Highlights of the Z86230 include:

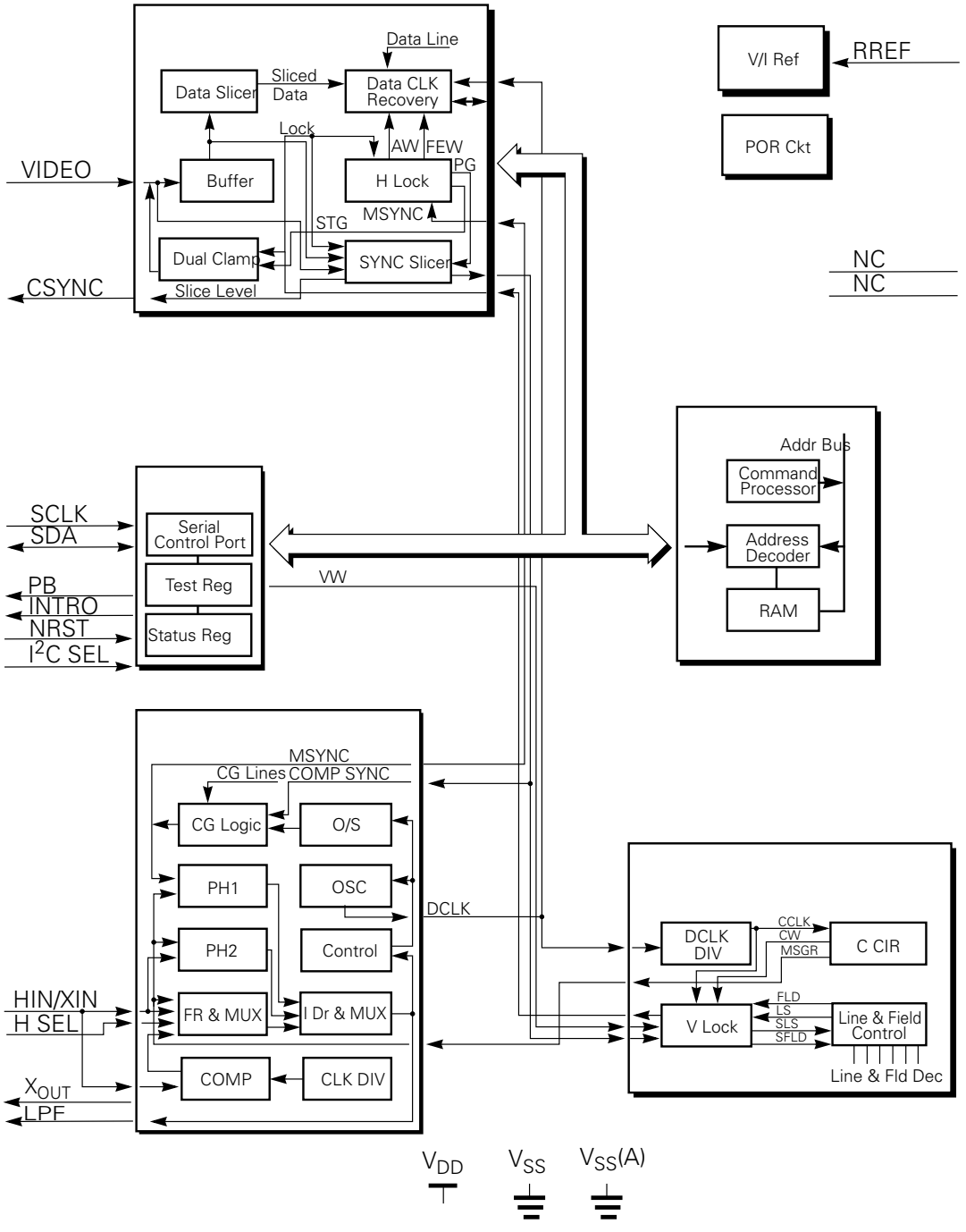
1. A stand-alone Line 21 Decoder for Extended Data Services (XDS).
2. Extractable XDS data from the input video.
3. Full output of a selectable V-Chip Program Blocking signal (PB).
4. Selectable XDS filter parameters from a list of preprogrammed values.
5. Minimal communications and control overhead that provides simple implementation of Violence Blocking and Auto Clock Set Features.
6. Full output of the recovered XDS data through the I^2C serial communication port.
7. Two different slave addresses that are selectable in the I^2C serial communication port.
8. Selectable NTSC or PAL operation.

1.1 BLOCK DIAGRAM AND OPERATIONAL OVERVIEW

The Z86230 is designed to process XDS data of the television VBI. The device requires both a Composite Video and a horizontal timing signal (HIN/XIN input). Several passive components are required for proper operation. Commands are input to enable the decoder to process and control the V-Chip response to the XDS Content Advisory packet. The Z86230 can also be configured to operate with PAL video signals. In PAL mode, the device decodes information encoded into VBI Line 22. The encoded data must conform to the waveform and command structure defined for NTSC Line 21 operation.

Figure 1 illustrates the Functional Block Diagram of the Z86230.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



1.1.1 Input Signals

The Composite Video input should be a signal which is nominally 1.0 Volt p-p, with sync tips negative and band limited to 600 kHz. The Z86230 operates with an input level variation of ±3 dB.

The HIN/XIN input signal is required to bring the voltage-controlled oscillator (VCO) close to the required operating frequency.

1.1.2 Video Input Signal Processing

The Composite Video input is AC-coupled to the device where the sync tip is internally clamped to a fixed reference voltage.

The Data Slicer extracts a clean CMOS-level data signal by slicing the signal at its midpoint. The slice level is established on an adaptive basis during Line 21.

The Sync Slicer processes the clamped Composite Video signal to extract Composite Sync. This signal is used to lock the internal logic to the incoming video. The slice level is stored on the sync slice capacitor, CSYNC.

The Data Clock Recovery circuit operates in conjunction with the Horizontal (H) Lock circuit. These circuits produce a data clock (DCLK) and, when Line 21 code appears, DCLK phase lock is achieved during the clock run-in burst (used to reclock the sliced data). When phase lock is established, DCLK is maintained until a change in the video signal occurs.

1.1.3 Voltage-Controlled Oscillator (VCO) and One-Shot

All internal timing and synchronizing signals are derived from the on-board 12-MHz VCO. Its output is the DCLK signal used to drive the Horizontal and Vertical counter chains.

The One-Shot circuit produces a horizontal timing signal derived from the incoming video.

The VCO exhibits stable gain characteristics and good power supply rejection.

1.1.4 Timing and Counting Circuits

The DCLK is divided to generate the horizontal timing signals H and 2H.The H signal is further divided in the line counter (LINE CNTR) and field counter (FLD CNTR) to produce the various decodes used to establish vertical lock and to time the control functions required for proper operation.

1.1.5 Command Processor

The Command Processor controls the manipulation of the data for storage. During the recovery time, the command processor, in conjunction with the data recovery circuits, recovers the XDS data.

1.1.6 Decoder Control Circuit

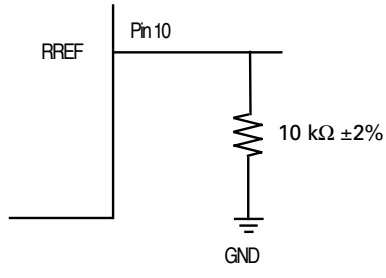
The Decoder Control circuit block is the users communications port. This circuit converts the information from the control port into the internal control signals required to establish the operating mode of the decoder.

The Z86230 responds to its slave address for both the READ and WRITE conditions. If the READ bit is Low (indicating a WRITE sequence), then the Z86230 responds with an Acknowledge. The master should then send an address byte followed by a data byte. If the READ bit is High (indicating a READ sequence), then the Z86230 responds with an Acknowledge followed sequentially by a status byte and a data byte. READ data is only available through indirect addressing. WRITE addressing exhibits both indirect and direct modes. The busy bit in the status byte indicates if the WRITE operation is completed or if READ data is available.

1.1.7 Voltage/Current Reference

The Voltage/Current reference circuit uses an externally connected resistor to establish the reference levels that are used throughout the Z86230. For a minimal investment, the use of an external resistor can also provide improved internal precision.

FIGURE 2. VOLTAGE/CIRCUIT REFERENCE



2. PIN DESCRIPTIONS

There are 2 different packages, 18-pin DIP and 18-pin SOIC, available in the Z86230.

FIGURE 3. 18-PIN DIP AND SOIC DEVICES

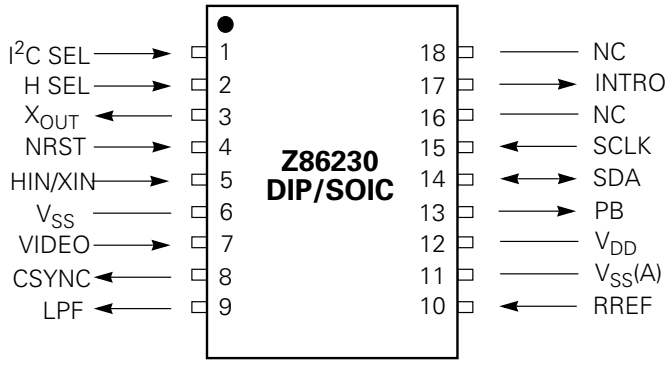


TABLE 1. PIN DESCRIPTIONS

Symbol	Pin #	Function	Direction	Description
I^2C SEL	1	I^2C Address Select	Input	Selects I^2C Address. Low(0) sets the slave address to `28h` for WRITE and `29h` for READ. HIGH(1) sets the slave address to `2Ah` for WRITE and `2Bh` for READ.
H SEL	2	HIN/XIN Select	Input	Selects the source of the horizontal frequency signal. Tying pin 2 HIGH(1) selects XIN mode. Tying pin 2 Low(0) selects HIN mode.
X_{OUT}	3	XTAL Output	Output	When operating in XIN mode this pin is the output pin for the XTAL circuit. In HIN mode, the X_{OUT} pin is a no connect (NC).
NRST	4	RESET	Input	Capable of being tied to an $\overline{\text{RESET}}$ signal if a Power-On Reset action is required. $\overline{\text{RESET}}$ must be held Low(0) for at least 100ns; otherwise, the pin must be tied HIGH(1).

TABLE 1. PIN DESCRIPTIONS

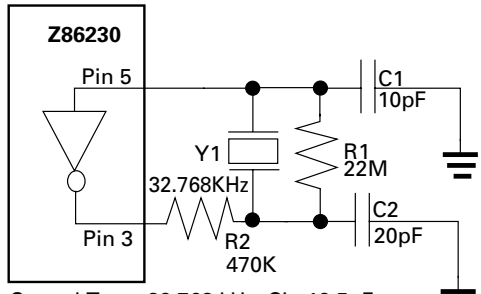
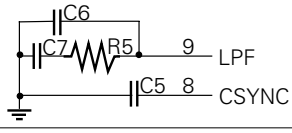
Symbol	Pin #	Function	Direction	Description
HIN/XIN	5	Horizontal In/XTAL In	Input	When XTAL mode is selected, the horizontal frequency signal may be generated on the chip using the external 32.768-kHz crystal circuit, as shown below. This circuit must be connected between pin 5 and 3.  Crystal Type: 32.768 kHz, CL=12.5pF Series Resistance < 35 kOhms (18 kOhms typ) Epson, C-001R 32.768 kHz or Fox, NC26, NC28 or equivalent When HIN mode is selected, a horizontal frequency signal must be supplied to the pin. This signal must be within +3% Fh; however, the frequency signal can exhibit any polarity and duty cycle. Alternatively, an external horizontal frequency signal may be used in XIN mode operation. In this case, the signal must exhibit a frequency of 32.768 KHz.
V_{SS}	6	Power Supply (digital) GND	N/A	This pin is the lowest potential power pin for the digital circuit that is typically tied to system ground.
VIDEO	7	Composite Video	Input	Composite NTSC video input, 1.0V p-p (nom), band limited to 600 kHz. The circuit operates with signal variation between 0.7–1.4V p-p. The polarity is sync tips negative. This signal pin should be AC-coupled through a 0.1 µF capacitor and driven by a source impedance of 470 ohms or less.
CSYNC	8	Composite Sync	Output	Sync slice level. A 0.1 µmF capacitor must be tied between this pin and analog ground V_{SS}(A). This capacitor stores the sync slice level voltage.

TABLE 1. PIN DESCRIPTIONS

Symbol	Pin #	Function	Direction	Description
LPF	9	Loop Filter	Output	Loop Filter. A series RC low-pass filter must be tied between this pin and analog ground V_{SS}(A). There must also be second capacitor from the pin to V_{SS}(A). 
RREF	10	Resistor Reference	Input	Reference setting resistor. This resistor must be 10 kOhms, ±2%.
V_{SS}(A)	11	Power Supply (Anlalog) GND	N/A	This pin is the lowest potential power pin for the analog circuit that is typically tied to system ground.
V_{DD}	12	Power Supply +5V	N/A	The voltage on this pin is nominally 5.0 Volts, and may range between 4.75 to 5.25 Volts with respect to the V_{SS} pins.
PB	13	Program Blocking	Output	This pin is HIGH(1) when the received Content Advisory packet matches the viewers selection as entered into the Content Advisory Rating Select registers.
SDA	14	Serial Data	In/Output	This pin is the bidirectional data line for sending and receiving serial data.
SCLK	15	Serial Clock	Input	This pin acts as an input pin for the serial clock signal from the I^2C master. The clock rate is expected to be within I^2C limits.
NC	16	No Connect	N/A	No Connect
INTRO	17	Interrupt Output	Output	This pin provides an interrupt signal to the master control device in accordance with the settings in the Interrupt Mask Register.
NC	18	No Connect	N/A	No Connect

3. Z86230 FEATURE SET

The primary features of the Z86230 are briefly described below. More complete descriptions can be found in later sections of this document.

3.1 VBI DATA PROCESSING

The Z86230 extracts the XDS data in Line 21 of the incoming video. Processing includes:

1. Extracting XDS data from the input video.
2. Outputting the V-Chip Program Blocking signal (PB).
3. Outputting the XDS data through the serial port (raw or filtered).
4. Selecting the XDS filter parameters from a list of preprogrammed values.
5. Selecting either NTSC or PAL operation.

3.2 SERIAL COMMUNICATIONS INTERFACE

Communications and control of the Z86230 is possible through the I^2C serial control interface, composed of:

1. A 2-wire I^2C interface.
2. Two available slave addresses.

TABLE 2. Z86230 SERIAL CONTROL SIGNALS

Signal	I^2C SEL	SCLK	SDA
Pin #	1	15	14
I/O	I	I	I/O
1st I^2C Address (28h(W)/29h(R))	0	CLK	Data
2nd I^2C Address(2Ah(W)/2Bh(R))	1	CLK	Data

3.3 SETUP AND OPERATIONAL CONTROL

The Z86230 is fully programmable through its flexible I^2C serial communication port. The following tables provide a *partial list* of User-Programmable Features and Default Conditions upon RESET.

TABLE 3. USER PROGRAMMABLE FEATURES

Feature	Parameters	RESET Condition
Video Standard	NTSC/PAL	NTSC
VCO Lock	Video/External HIN	Video
H Lock	Video/External HIN	Video
XDS Data Output	Raw/Filtered	OFF
Contents Advisory Rating Select	ON/OFF	OFF
Program Blocking	ON/OFF	ON
Blocking *No Rating* Programs	ON/OFF	OFF
Program Unblock Hold Off	Up to 254 Vertical Frames	0

4. SERIAL COMMUNICATIONS INTERFACE

Commands and data are sent to and from the Z86230 through its I²C serial communications interface. This port is the path for setting the configuration and operational modes of the device. The interface is also used as the port for outputting the recovered XDS data.

4.1 I²C BUS OPERATION

The Z86230 supports a bidirectional 2-wire bus and data transmission protocol. The bus is controlled by the master device, which generates the serial clock (SCLK), controls the bus access, and generates the START and STOP conditions. The serial data (SDA) pin is the bidirectional data line. The Z86230 is a slave device with two possible slave addresses. When the I²C SEL pin is Low, the slave address is 28h for WRITE and 29h for READ. When the I²C SEL pin is High, the slave address is 2Ah for WRITE and 2Bh for READ.

The Z86230 can receive or transmit data under control of the master device. Communication is initiated when the master device sends the START condition followed by the Z86230 Slave Address READ byte or Slave Address WRITE byte. The Z86230 responds with an Acknowledge.

The I²C RD/$\overline{WR}$ bit is the Least Significant Bit (LSB) of the I²C addresses listed below in Table 4.

TABLE 4. Z86230 I²C SLAVE ADDRESSES

	READ	WRITE
1st I²C Address	29h	28h
2nd I²C Address	2Bh	2Ah

NOTE: Low(0) on pin 1 selects the 1st I²C Address; HIGH(1) on pin 1 selects the 2nd I²C Address.

4.1.1 The I²C Bus Protocol

The Bus Protocol requires that:

1. Data transfer can only be started when the bus is not busy.
2. During data transfer, data transitions must not occur while the clock is High.

4.1.2 Bus Conditions

Bus Conditions are defined as:

Not Busy. Data and Clock lines are both High.

START. A High-to-Low transition of the SDA line while the SCLK line is High.

STOP. A Low-to-High transition of the SDA line while the SCLK line is High.

Acknowledge. When addressed, the receiving device must output an Acknowledge after the reception of each byte. The master device must generate the clock for the Acknowledge bit. Acknowledge is SDA = Low. Not Acknowledge (NACK) is SDA = High.

Data. The data (SDA) is output by the transmitting device on the falling edge of SCLK, MSB first. The receiving device interprets the data, MSB first, on the rising edge of SCLK.

Communication with the Z86230 is initiated when the master device sends the Z86230 slave address following a START condition. The Z86230 has a preset, single, seven-bit slave address. The Z86230 responds with an Acknowledge. The eighth bit of the slave address is driven High for READ operations and Low for WRITE operations.

4.1.3 Writing to the I2C Bus

Commands and data are written to the Z86230 using the I2C bus interface. The device is enabled when an I2C START condition, followed by its Slave Address WRITE byte, is received. A WRITE operation is ended and the bus is disabled upon the receipt of an I2C STOP condition. Any number of command bytes, up to 32, may be sent after the device is WRITE-enabled. Each of these commands is either 1 or 2 bytes in length. The device executes the commands in order of receipt.

Overflowing the 32 byte buffer causes improper operation. The RDY bit of the Serial Status Register (SSR) may be read to determine if there is room in the command buffer for at least 2 bytes of command data. The Status register data is output immediately following the receipt of the Slave Address READ.

The first byte of a 2-byte command is always written first. The master's sequence for writing a 2-byte command, followed by a 1-byte command is displayed in the following example:

Start

Slave_Address_Write/Slave ACK

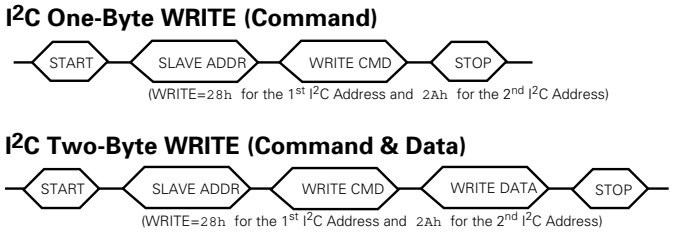
CMD1_Write/Slave ACK

DATA1_Write/Slave ACK

CMD2_Write/Slave ACK

Stop

FIGURE 4. I²C BUS WRITE (COMMAND)



NOTE: The Status Register RDY bit must be read and checked prior to the START condition of either WRITE sequence above. Refer to the One Byte READ (Status Only) in Figure 5 for more information on reading the Status Register.

4.1.4 Reading Data Using the I²C Bus

The Z86230 I²C bus supports READ sequences up to 34 bytes in length. All READ sequences output the Serial Status Register (SSR) as the first output byte. The data to be read is selected by sending the READ BANK SELECT (RBS) command. Four READ bank modes are available in the Z86230:

TABLE 5. Z86230 I²C READ BANK SELECT (RBS) COMMAND

RBS Command	Descriptions
Bank 0	A general-purpose bank used to read the Z86230-defined internal registers. The register to be read from Bank 0 is set up manually using the READ SELECT commands, RDS1 and RDS2. These commands load the selected data byte (or pair of bytes) into the first location(s) of Bank 0, and set the DAV bit to indicate the availability of data.
Bank 1	A special purpose bank provided to facilitate the reading of commonly accessed data. This bank contains the Program Blocking registers and permits direct, multibyte reading of internal registers 08h through 11h. These registers are described in the internal register section. When it is selected, the sequence of bytes read is SSR, followed by internal registers 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h, and 11h.
Bank 2	A special purpose bank provided to facilitate the reading of commonly accessed data. This bank contains the XDS Program Name data from the most recently received current class type 3 packet.
Bank 3	A special purpose bank provided to facilitate the reading of commonly accessed data. This bank contains the XDS Network Name and Call Letter data. The first 26 bytes has the XDS Network Name from the most recently received XDS channel class type 1 packet. Bytes 26 through 31 has the XDS Call Letters data from the most recently received XDS channel class type 2 packet

NOTE: Banks 2 and 3 are 33 bytes in length. Byte 32 of these banks contains an 8 bit checksum. The checksum is calculated such that the addition of the 32 data bytes and the checksum modulo 256 equals zero. The checksum should always be evaluated after reading this data to ensure that the XDS data is not being updated during the READ operation. The result is a meaningless combination of two unrelated XDS data packets. If a bad checksum is encountered, the READ operation should be repeated.

All READ sequences output the SSR first. If the Serial Status register DAV bit is set, a 2- or multiple-byte READ sequence can be initiated, beginning with a START condition. If the DAV bit is not set, the I2C master device should not attempt to read any data bytes or the required data can be lost from the Z86230 output registers. The I2C master device should end the READ sequence by failing to acknowledge the received byte. This sequence is repeated until the DAV bit becomes true.

NOTE: In all I2C READ operations (1-, 2- and 3-byte reads are illustrated in Figure 5), the most recent byte read from the Z86230 should be acknowledged by the master with a Not Acknowledge (NACK). The DAV bit of the Serial Status Register (SSR) is cleared by the master clocking out the eighth bit of the first data byte read. The DAV bit is never cleared by just reading the SSR (One Byte READ) alone. All data is output MSB first.

The master's sequence for reading two *data bytes* (total of 3 bytes including SSB) from the Z86230 is:

Start

Slave_Address_Read/Slave_ACK

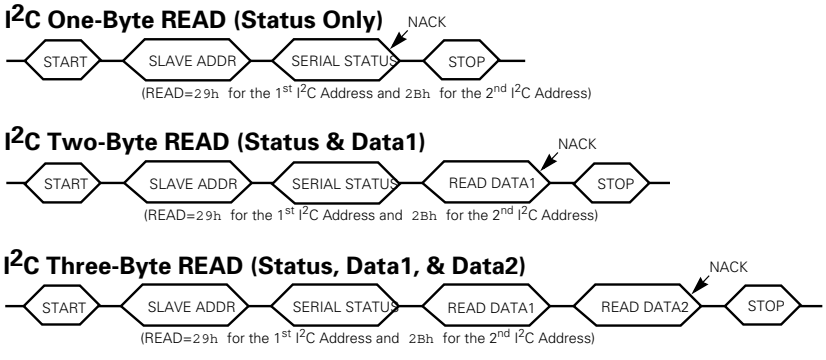
SS_Byte/Master ACK

First_Byte/Master ACK

Second_Byte/Master_NACK

Stop

FIGURE 5. I2C BUS READ (COMMAND)



NOTE: In all I2C READ operations, the most recent byte read from the Z86230 must be acknowledged by the master with a NACK (Not ACKnowledge).

4.1.5 Clock and Data Transitions

The SCLK and SDA bus lines are normally pulled High with a resistor. Data on the SDA bus may only change during SCLK Low time periods. Data changes during SCLK High periods indicate a START or STOP condition as defined in Table 6.

4.1.6 START Condition

A High-to-Low transition of SDA with SCLK High is a START condition which must precede any other command.

4.1.7 STOP Condition

A Low-to-High transition of SDA with SCLK High is a STOP condition which terminates all communications.

4.1.8 Acknowledge

All address and data words are serially transmitted to and from the Z86230 in eight bit words. A ninth bit time is used for the Acknowledge. The acknowledging device pulls the SDA bus Low during the ninth bit. A Not Acknowledge (NACK) is returned by SDA = High during the ninth clock time.

FIGURE 6. I²C SERIAL TIMING

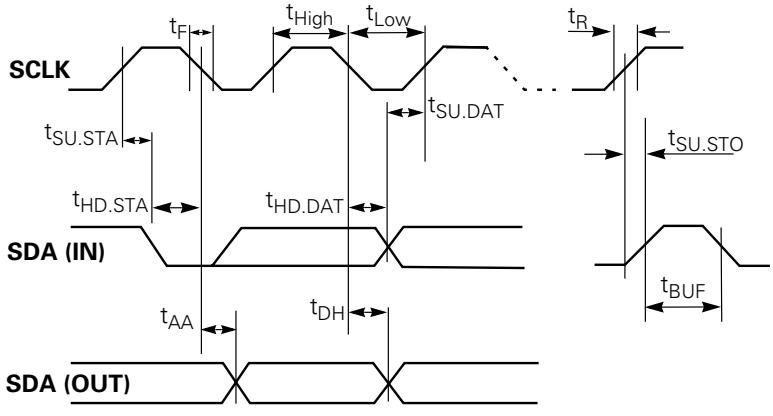


TABLE 6. I²C SERIAL TIMING MIN/MAX

Symbol	Parameter	Min	Max	Units
f_{SCLK}	Clock Frequency		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7	–	ms
t_{High}	Clock Pulse Width High	4.0	–	ms
t_R	SDA and SCL Rise Time	–	1.0	ms
t_F	SDA and SCL Fall Time	–	300	ns
t_{AA}	Clock Low to Data Out Valid	0.1	3.5	ms
t_{BUF}	Bus Free Time	4.7	–	ms
$t_{HD.STA}$	Start Hold Time	4.0	–	ms
$t_{SU.STA}$	Start Set-up Time	4.7	–	ms
$t_{HD.DAT}$	Data In Hold Time	0	–	ms
$t_{SU.DAT}$	Data In Set-up Time	250	–	ns
$t_{SU.STO}$	Stop Set-up Time	4.7	–	ms
t_{DH}	Data Out Hold Time	100	–	ns
t_I	Input Filter Time Constant		100	ns

5. COMMANDS

5.1 SERIAL PORT COMMANDS

The commands must be contained within the Start–Slave Address–etc. sequence.

NOTE: In the following Command descriptions, the letter h following a command code designates hexadecimal notation.

5.1.1 RESET = FBh

RESET is a 1-byte command. The RESET command establishes all of the specified default settings in the device, but it does not reset the serial port itself. The RESET command must be followed by a no operation (NOP) command, because RESET stays active until deactivated by the NOP. This sequence can be entered without the RDY bit being set.

5.1.2 NOP = 00h

NOP is a 1-byte command. The NOP command does not affect the status of the RDY bit in the Serial Status Register (SSR) and can be executed independent of the RDY status.

TABLE 7. BASIC SERIAL COMMANDS

Serial Command	Command Code
RESET	FBh
NOP	00h

5.2 READ AND WRITE COMMANDS

All register diagrams indicated in this section incorporate the following conventions, unless otherwise noted:

- R = Read, W = Write, X = Indeterminate, and *res* = Reserved
- All register bits marked as *res* must be set to Low(0)

5.2.1 READ Bank Select (RBS = FDh)

RDS1 is a 2-byte command to select the read data bank. The lower 2 bits of the second data byte select one of four banks of up to 33 bytes. A subsequent I^2C READ deciphers data from the specified bank.

5.2.2 READ SELECTs (RDS1 = 40h–51H)

RDS1 is a 1-byte command used to initiate a 1-byte READ sequence. This activity is performed by moving the contents of the register identified by the address field (AD00:04) of the command to the first location of READ bank 0. Addresses 00h–11h are valid in the RDS1 command field AD00:04.

TABLE 8. RDS1–READ ONE BYTE (RDS1 = 40h–51h)

Bit	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	0	1	0	AD04	AD03	AD02	AD01	AD00
R/W	W	W	W	W	W	W	W	W

5.2.3 RDS2 = 60h–70h

RDS2 is a 1-byte command which is used to initiate a 2-byte READ sequence by moving the contents of the two consecutive registers, starting with the one identified by the address portion of the command (AD00:AD04), to the first 2 locations of read bank 0. Only Addresses 00h–10h are valid in the RDS2 command field AD00:04.

NOTE: For XDS data recovery, when the XDS Filter Register (see Control Registers) is enabled for the required packets, the Z86230 automatically establishes the 2-byte recovery mode and moves the recovered data bytes to the first 2 locations of bank 0.

TABLE 9. RSD2–READ TWO BYTES (RDS2 = 60h–70h)

Bit	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	0	1	1	AD04	AD03	AD02	AD01	AD00
R/W	W	W	W	W	W	W	W	W

5.3 WRITING TO THE Z86230

5.3.1 WRxx = C0h–D1h

TABLE 10. WRXX–WRITE REGISTER XX (WRX = C0h–D1h)

Bit	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	1	1	0	AD04	AD3	AD2	AD1	AD0
R/W	W	W	W	W	W	W	W	W

The WRITE commands require 2 bytes to execute. The first byte is the write command and includes the Z86230 register address (AD00:04) being written. The second byte is the data to be written.

6. CONTROL REGISTERS

Information controlling the setup and operation of the Z86230 are maintained in several registers. The user may read or alter the contents of these registers as required.

All register diagrams indicated in this section incorporate the following conventions, unless otherwise noted:

- R = Read, W = Write, X = Indeterminate, and *res* = Reserved
- All register bits marked as *res* must be set to Low(0)

6.1 REGISTERS SUMMARY

6.1.1 Serial Status Register

TABLE 11. SERIAL STATUS REGISTER (ADDRESS NOT REQUIRED)

Bit	7	6	5	4	3	2	1	0
	RDY	DAV	res	WOVR	INTR	ROVR	FLD	LOCK
R/W	R	R	R	R	R	R	R	R

D_0–LOCK. Active High, indicating that the internal sync circuits are locked. May be used as an indication of the presence of a video signal.

D_1–FLD. Signals the current video field. Low = Field 2, High = Field 1.

D_2–ROVR. Active High, indicating that the data available in the output buffer is not read out and new data is written over it.

D_3–INTR. Active High, indicating that an interrupt other than DAV is pending. Reserved.

D_4–WOVR. Active High, indicating a serial input data overrun.

D_5-Res. Reserved.

D_6-DAV. Active High, indicating that data is available to be read out.

D_7–RDY. Active High, indicating that the port input buffer is empty. Only the NOP, RESET and READ instructions may be sent if RDY is Low.

6.1.2 Configuration Register

TABLE 12. CONFIGURATION REGISTER (ADDRESS = 00h)

Bit	7	6	5	4	3	2	1	0
	res	res	res	res	res	res	res	TVS
R/W	R	R	R	R	R	R/W	R	R/W