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Z86C91

CMOS Z8® ROMLess Microcontrollers

Product Specification

PS018501-1002

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Architectural Overview

ZiLOG's large Z8® family of 8-bit ROMless microcontrollers includes the Z86C91 product with 236 bytes of RAM. Each of these devices offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

For applications demanding powerful I/O capabilities, the Z86C91 offers 24 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines and is configurable under software control to proviide timing, status signals, serial or parallel I/O with or without handshake and an address/data bus for interfacing external memory. The Z86C91 MCU features three basic address spaces to support this wide range of configurations: Program Memory, Data Memory, and 236 General Purposes Registers.

The Z86C91 operates at 16 MHz with a voltage range of 4.5 to 5.5VDC.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z86C91 offers two on-chip counter/timers with a large number of user-selectable modes and a full-duplex hardware UART.

The Z86C91 is a ROMless part and offers the use of external memory, which enables this Z8® MCU to be used in high-volume applications, or where code flexibility is required.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Z86C91 Features

- Asynchronous receiver/transmitter UART
- 40-Pin DIP and 44-Pin PLCC and QFP Packages
- 4.5- to 5.5-Volt Operating Range
- Operating Temperature Ranges:
  - Standard: 0ºC to 70ºC
  - Extended: -40ºC to 105ºC
- 24 Input/Output Lines

- Six Vectored, Prioritized Interrupts from Eight Different Sources
- Two Programmable 8-Bit Counter/Timers, each with two 6-Bit Programmable Prescalers
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, or External Clock
- Two Standby Modes: STOP and HALT
- Auto Latches

Functional Block Diagrams

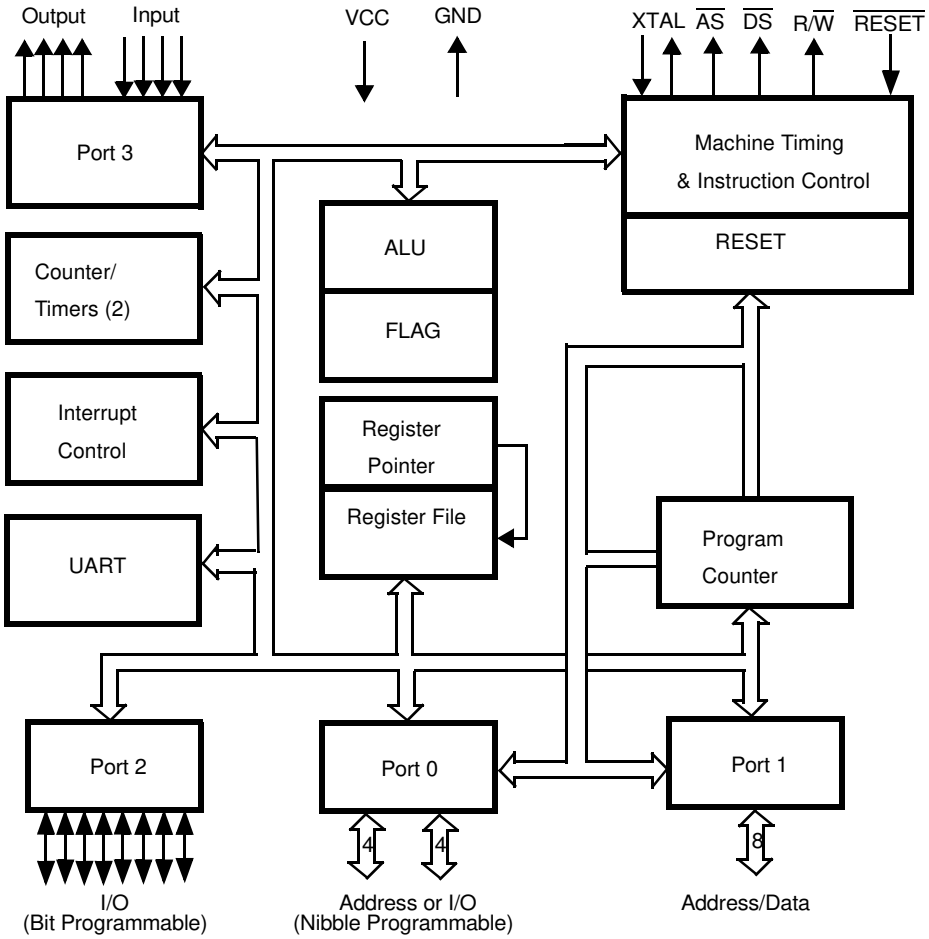

Figure 1. Z86C91 Functional Block Diagram

Pin Description

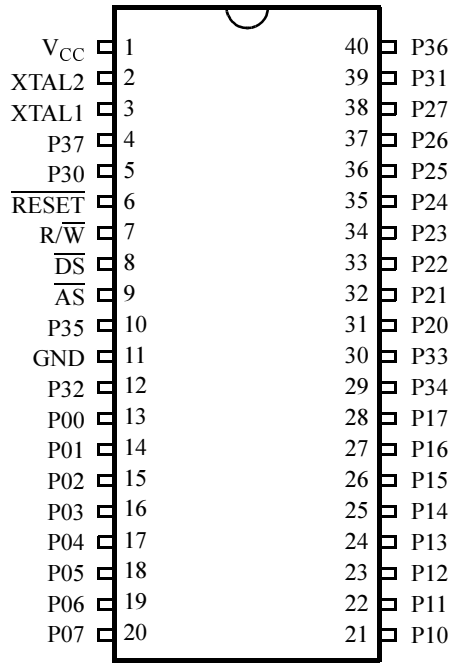

Figure 2. 40-Pin DIP Pin Configuration

Table 12. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	$\overline{RESET}$	Reset	Input
7	R/$\overline{W}$	Read/Write	Output
8	$\overline{DS}$	Data Strobe	Output
9	$\overline{AS}$	Address Strobe	Output
10	P35	Port 3, Pin 5	Output

Table 12. 40-Pin DIP Pin Identification (Continued)

Pin #	Symbol	Function	Direction
11	GND	Ground, V_{SS}	Output
12	P32	Port 3, Pin 2	Input
13-20	P00-P07	Port 0, Pins 0-7	Input/Output
21-28	P10-P17	Port 3, Pins 0-7	Input/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P20-P27	Port 2, Pins 0-7	Input/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

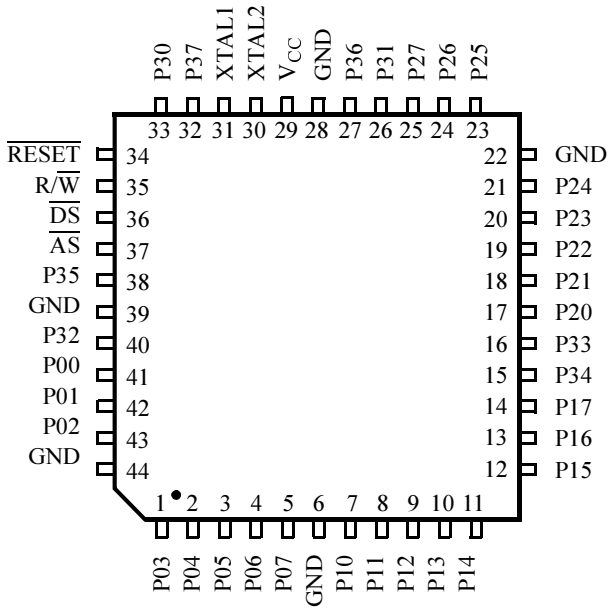

Figure 3. 44-Pin PQFP Pin Configuration

Table 13. 44-Pin PQFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0, Bits 3-7	Input/Output
6	GND	Ground	Output
7-14	P10-P17	Port 1, Bits 0-7	Input/Output
15	P34	Port 3, Bit 4	Output
16	P33	Port 3, Bit 3	Intput
17-21	P20-P24	Port 2, Bits 0-4	Input/Output
22	GND	Ground	Output
23-25	P25-P27	Port 2, Bits 5-7	Input/Output
26	P31	Port 3, Bit 1	Input
27	P36	Port 3, Bit 6	Output
28	GND	Ground	Output

Table 13. 44-Pin PQFP Pin Identification (Continued)

Pin #	Symbol	Function	Direction
29	V_{CC}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3, Bit 7	Output
33	P30	Port 3, Bit 0	Intput
34	$\overline{\text{RESET}}$	Reset	Input
35	R/$\overline{\text{W}}$	Read/Write	Output
36	$\overline{\text{DS}}$	Data Strobe	Output
37	$\overline{\text{AS}}$	Address Strobe	Output
38	P35	Port 3, Bit 5	Output
39	GND	Ground	Output
40	P32	Port 3, Bit 2	Input
41-43	P00-P02	Port 0, Bits 0-2	Input/Output
44	GND	Ground	Output

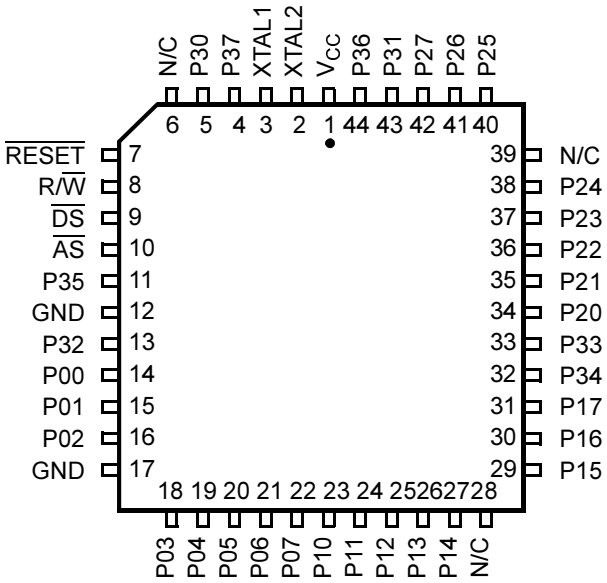

Figure 4. 44-Pin PLCC Configuration

Table 14. 44-Pin PLCC Configuration

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	
7	$\overline{RESET}$	Reset	Input
8	R/$\overline{W}$	Read/Write	Output
9	$\overline{DS}$	Data Strobe	Output
10	$\overline{AS}$	Address Strobe	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground V_{SS}	Output

Table 14. 44-Pin PLCC Configuration (Continued)

Pin #	Symbol	Function	Direction
13	P32	Port 3, Pin 2	Input
14-16	P00-P02	Port 0, Pins 0-2	Input/Output
17	GND	Ground	Output
18-22	P03-P07	Port 0, Pins 3-7	Input/Output
23-27	P10-P14	Port 1, Pins 0-4	Input/Output
28	N/C	Not Connected	
29-31	P15-P17	Port 1, Pins 5-7	Input/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P20-P24	Port 2, Pins 0-4	Input/Output
39	N/C	Not Connected	
40-42	P25-P27	Port 2, Pins 5-7	Input/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

Pin Functions

The following paragraphs describe the function of each available Z86C91 pin.

$\overline{\text{DS}}$ (output, active Low). The Data Strobe is activated one time for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). The Address Strobe is pulsed one time at the beginning of each machine cycle for external memory transfer. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and READ/WRITE.

XTAL1 (Crystal 1)Time-Based Oscillator Input. This pin connects a parallel-resonant crystal, ceramic resonator, LC network, or an external single-phase clock to the on-chip oscillatorand buffer.

XTAL2 (Crystal 2) Time-Based Oscillator Output. This pin connects a parallel-resonant crystal, ceramic resonant, LC network to the on-chip oscillator and buffer.

R/$\overline{\text{W}}$ (output, WRITE Low). The READ/WRITE signal is Low when the Z8 writes to external data memory.

$\overline{\text{RESET}}$ (input, Low). To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external XTAL clocks (4TpC). If the external $\overline{\text{RESET}}$ signal is less than 4TpC in duration, reset does not occur.

On the fifth clock after $\overline{\text{RESET}}$ is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external $\overline{\text{RESET}}$, whichever is longer. During the reset cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of TpC/2. When $\overline{\text{RESET}}$ is deactivated, program execution begins at location 000Ch. Power-Up reset time must be held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P00–P07). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03–P00 input/output and P07–P04 input/output), or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control $\overline{\text{DAV0}}$ and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04–P07. The lower nibble must indicate the same direction as the upper nibble.

For external memory references, Port 1 provides address bits A7–A0 (lower nibble) and Port 0 provides address bits A15–A8 (upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 is programmed independently as I/O while the lower nibble is used for addressing. If one or

both nibbles are required for I/O operation, they are configured by writing to the Port 01 mode register (P01M).

After a hardware RESET, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode.

Port 0 can be placed in a high-impedance state along with Port 1, $\overline{AS}$, $\overline{DS}$ and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 5). A hardware RESET is required to exit this high-impedance state.

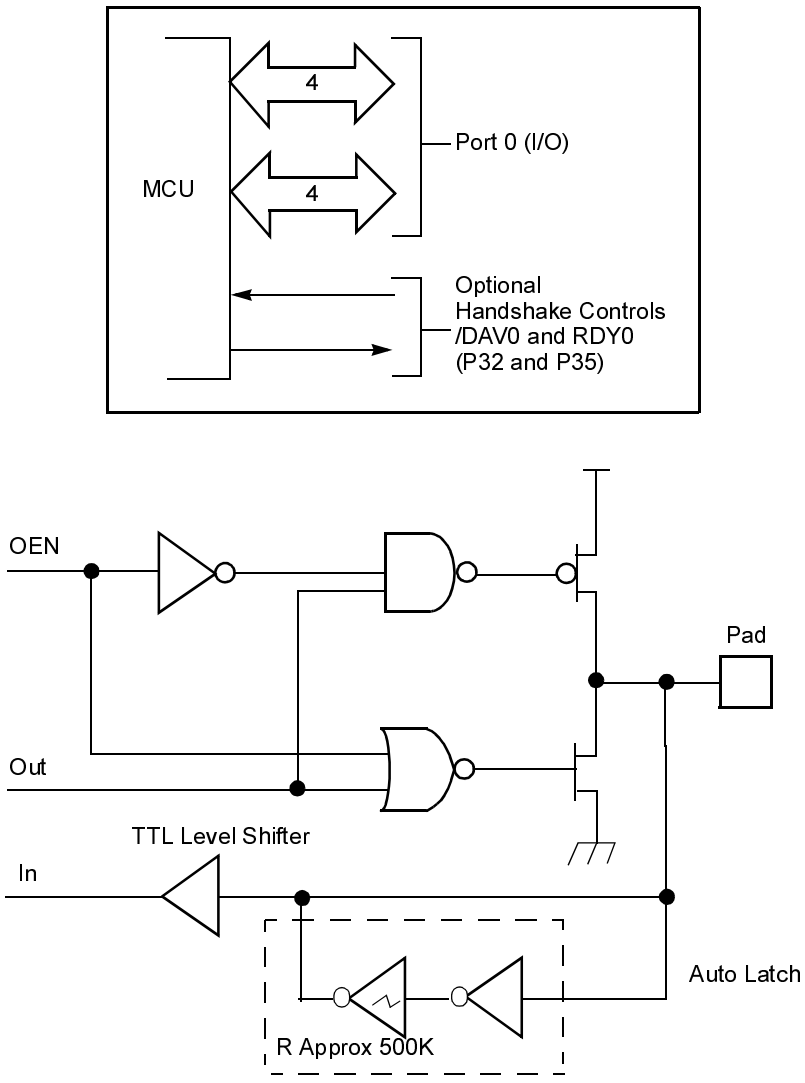

Figure 5. Port 0 Configuration

Port 1 (P17–P10). Port 1 is an 8-bit, TTL- compatible port (Figure 6), with multiplexed Address (A7–A0) and Data (D7–D0) ports for interfacing external memory. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 6). A hardware RESET is required to exit this high-impedance state.

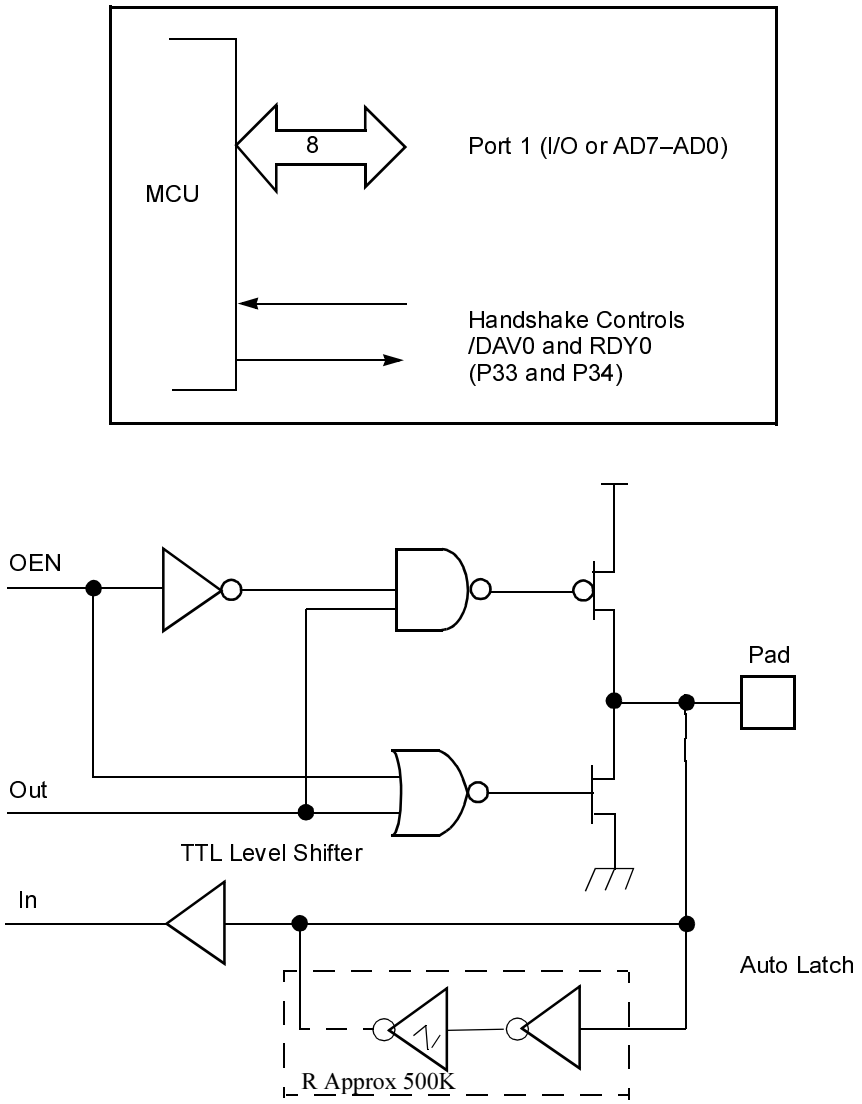

Figure 6. Port 1 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit programmable, bidirectional, TTL-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently or globally as an open-drain output. Port 2 is always available for I/O operation.When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines $\overline{\text{DAV2}}$ and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7). After a RESET, Port 2 is configured as an input port. The Port 2 output portion of the circuit has open-drain as it's default configuration.

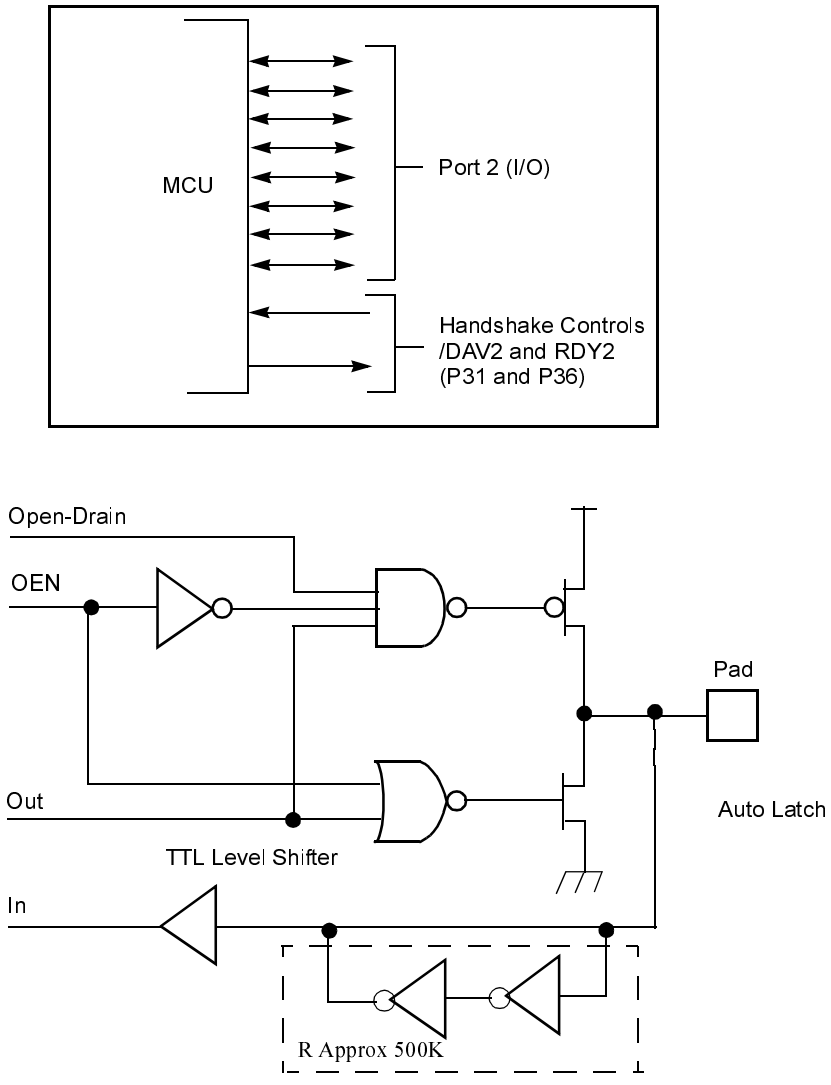

Figure 7. Port 2 Configuration

Port 3 (P37–P30). Port 3 is an 8-bit, TTL-compatible port, with four fixed inputs (P33–P30) and four fixed outputs (P34–P37). Port 3 is configured under software control for Input/Output, Counter/Timers, interrupt, UART, port handshake, and data Memory functions. Port 3, when used as serial I/O are programmed as serial in and serial out respectively (Figure 8).

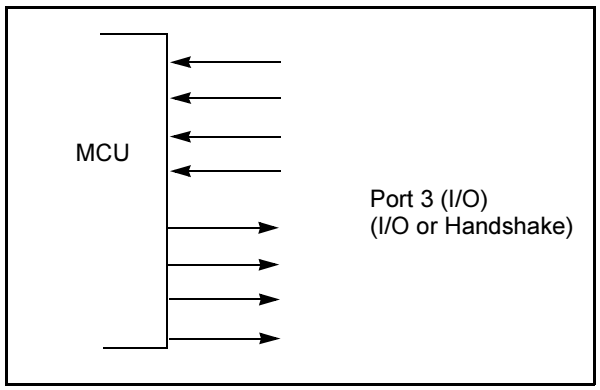

Figure 8. Port 3 Configuration

For interrupt functions, Port 3 inputs are falling-edge interrupt inputs. Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 ($\overline{DAV}$ and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals (T_{IN} and T_{OUT}); Data Memory Select.

P34 output is software-programmed to function as a Data Memory Select ($\overline{DM}$). The Port 3 Mode Register (P3M) bit D3,D4 selects this function. When accessing external data memory, P34 goes active Low; when accessing external program memory, P34 goes High.

An onboard UART is enabled by software setting bit D5 of the Port 3 Mode Register P3M. When enabled, P30 is the receive input and P37 is the transmit output.

Port 3, lines P30 and P37 are programmed as serial I/O for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer0.

The Z8 automatically adds a start bit and two stop bits to transmitted data. Serial Data formats are shown in Figure 9 and Figure 10. Odd parity is also available by setting bit D7 in the P3M register. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

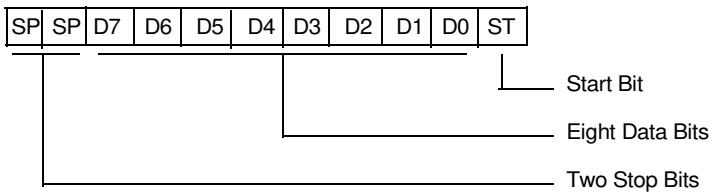

Figure 9. Transmitted Data (No Parity)

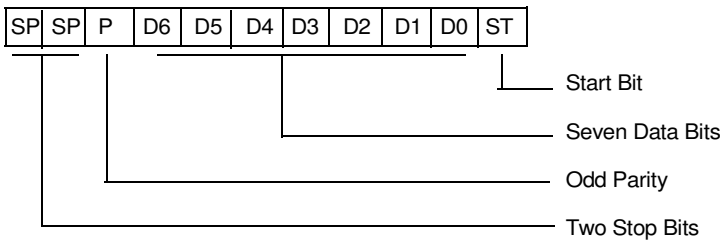

Figure 10. Transmitted Data (With Parity)

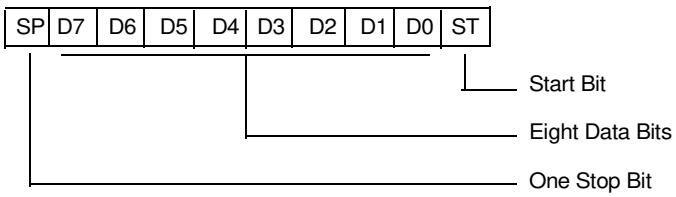

Figure 11. Received Data (No Parity)

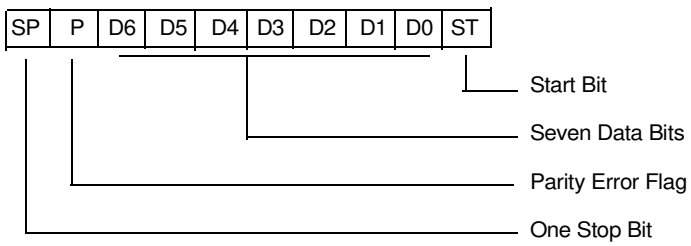

Figure 12. Received Data (With Parity)

Table 15. Port 3 Pin Assignments

Pin	I/O	Control Timer	Interrupt	P0 HS	P2 HS	Ext	UART
P30	IN		IRQ3				Serial In
P31	IN	T_{IN}	IRQ2		D/R		
P32	IN		IRQ0	D/R			
P33	IN		IRQ1				
P34	OUT					$\overline{DM}$	
P35	OUT			R/D			
P36	OUT	T_{OUT}			R/D		
P37	OUT						Serial Out

Notes:
HS = Handshake Signals
D = $\overline{DAV}$ (Data Available)
R = RDY (Ready)

Autolatch. The autolatch places valid CMOS levels on all inputs that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Autolatches are available on Port 0, Port 1, Port 2, and P3 inputs.

$\overline{RESET}$ (input, Low). Initializes the MCU. RESET occurs through external reset only. During Power-On Reset, the externally-generated reset drives the $\overline{RESET}$ pin Low for the POR time. Pull-up is provided internally.

Caution: $\overline{RESET}$ depends on oscillator operation to achieve full reset conditions.

$\overline{RESET}$ is a Schmitt-triggered input. During the RESET cycle, $\overline{DS}$ is held active Low while $\overline{AS}$ cycles at a rate of $T_PC \div 2$. Program execution begins at location `000Ch`, after the $\overline{RESET}$ is released.

When program execution begins, $\overline{AS}$ and $\overline{DS}$ toggles only for external memory accesses. The Z8 can only exit Stop Mode by using the $\overline{RESET}$ pin.The Z8 does reset all registers on a Stop-Mode Recovery operation out of STOP mode.

Functional Description

The Z8 MCU incorporates the following functions that enhance the standard Z8® architecture and provide the user with increased design flexibility:

- Reset
- Program Memory
- Data Memory
- Working Register
- General-Purpose Registers
- Stack Pointer
- Counter/Timers
- Interrupts
- Clock
- HALT and STOP Modes
- Port Configuration Register

RESET. The device is reset in the following condition:

- External Reset

Automatic Power-On Reset circuitry is not built into this Z8. This Z8 requires an external reset circuit to reset upon power-up. The internal pull-up resistor is on the $\overline{\text{RESET}}$ pin, so a pull-up resistor is not required; however, in a high-EMI (noisy) environment, it is recommended that a low-value pull-up resistor be used.

Program Memory. The Z86C91 can address up to 64 KB of external program memory. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at external location `000Ch` after reset. See Figure 13.

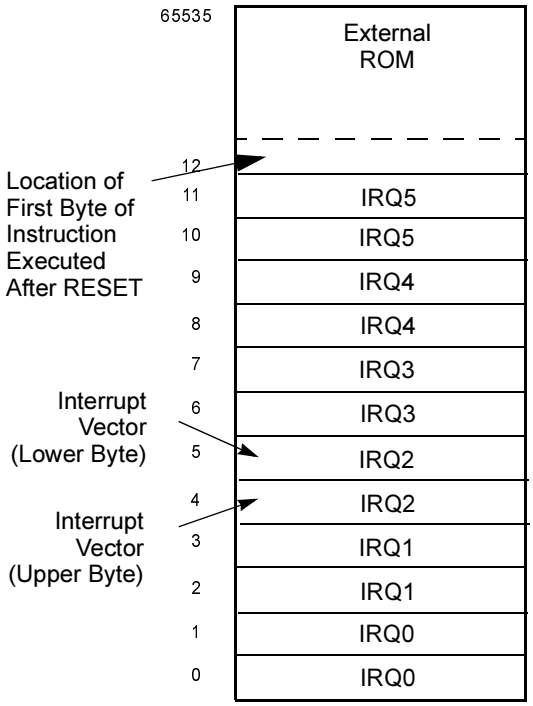

Figure 13. Program Memory Map

Data Memory ($\overline{DM}$). The Z86C91addresses up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that is programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC Op Code references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode.

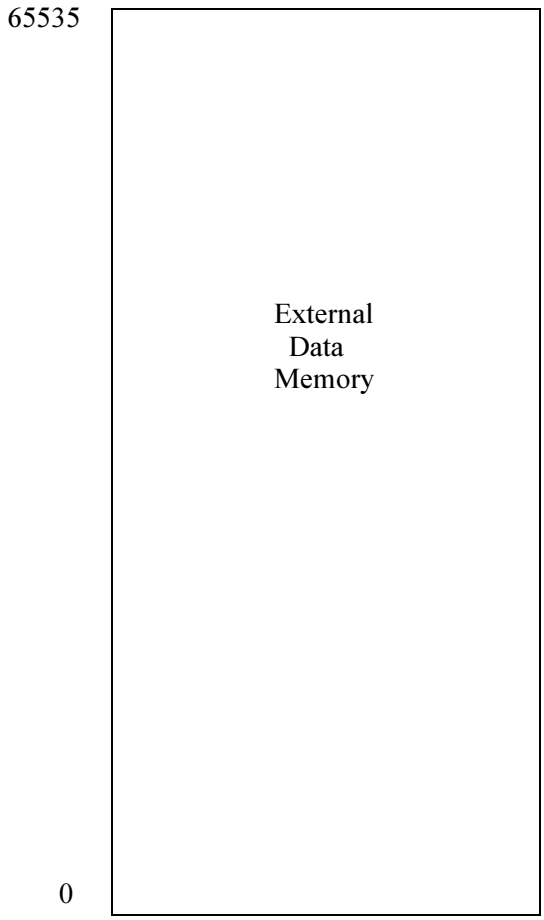

Figure 14. Data Memory Map

Register File. The register file contains three I/O port registers, 236 general-purpose registers, and 16 control and status registers (Figure 15). The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C91 also allows short 4-bit register addressing using the Register Pointer (Figure 16). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.