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Z86D86

28-Pin Low-Voltage OTP Microcontroller

Preliminary Product Specification

PS008905-0105

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Document Disclaimer

Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Document

Date	Revision Level	Section	Description	Page #
January 2005	05		Made minor corrections to Figure 23 Port 0 and 1 Mode Register.	29

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Features

Table 1 shows some of the features of the Z86D86 microcontroller.

Table 1. Z86D86 Features

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86D86	32	237	23	2.3 V to 5.5 V
Note: *General purpose				

- Low Power Consumption–40 mW (Typical)
- Three Standby Modes
  - STOP—2 µA
  - HALT—0.8 mA
  - Low Voltage
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers and Two Load Registers
  - One Programmable 16-Bit Counter/Timer with One 16-Bit Capture Register Pair and One 16-Bit Load Register Pair
  - Programmable Input Glitch Filter for Pulse Reception
- Six Priority Interrupts
  - Three External
  - Two Assigned to Counter/Timers
  - One Low Battery Detection Interrupt
- Low Battery Detection with Flag
- Programmable Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- Mask Selectable 200±50% KΩ Transistor Pull-Ups on Ports 0, 2.
- Programmable OTP Options:
  - Oscillator Selection: RC Oscillator vs. Crystal or Other Clock Source

  - Oscillator Operational Mode: Normal High Frequency Operation Enabled or 32 KHz Operation Enabled
  - Port 0: 0–3 Pull-Ups
  - Port 0: 4–7 Pull-Ups
  - Port 2: 0–7 Pull-Ups
  - Port 0: 0–3 Mouse Mode: Normal Mode (.5V_{DD} Input Threshold) vs. Mouse Mode (.4V_{DD} Input Threshold)
- Port 3 does not feature the pull-up option.

General Description

The Z86D86 is a 28-pin one-time programmable (OTP) infrared (IR) microcontroller. Based on a single-chip Z8 microcontroller (MCU) design, the Z86D86 features 237 bytes of general-purpose RAM and 32 KB of OTP ROM. ZiLOG's CMOS microcontrollers offer fast executing, efficient use of memory, sophisticated interrupts, input/output bit-manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z86L825 architecture is based on ZiLOG's 8-bit microcontroller core, featuring an Expanded Register File to allow access to register-mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and batter-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: program memory, register file, and Expanded Register File. The register file consists of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. (Register FEh (SPH) can be used as a general-purpose register.) The Expanded Register File consists of two additional register groups (F and D).

The Z86D86 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (Figure 9 on page 17).

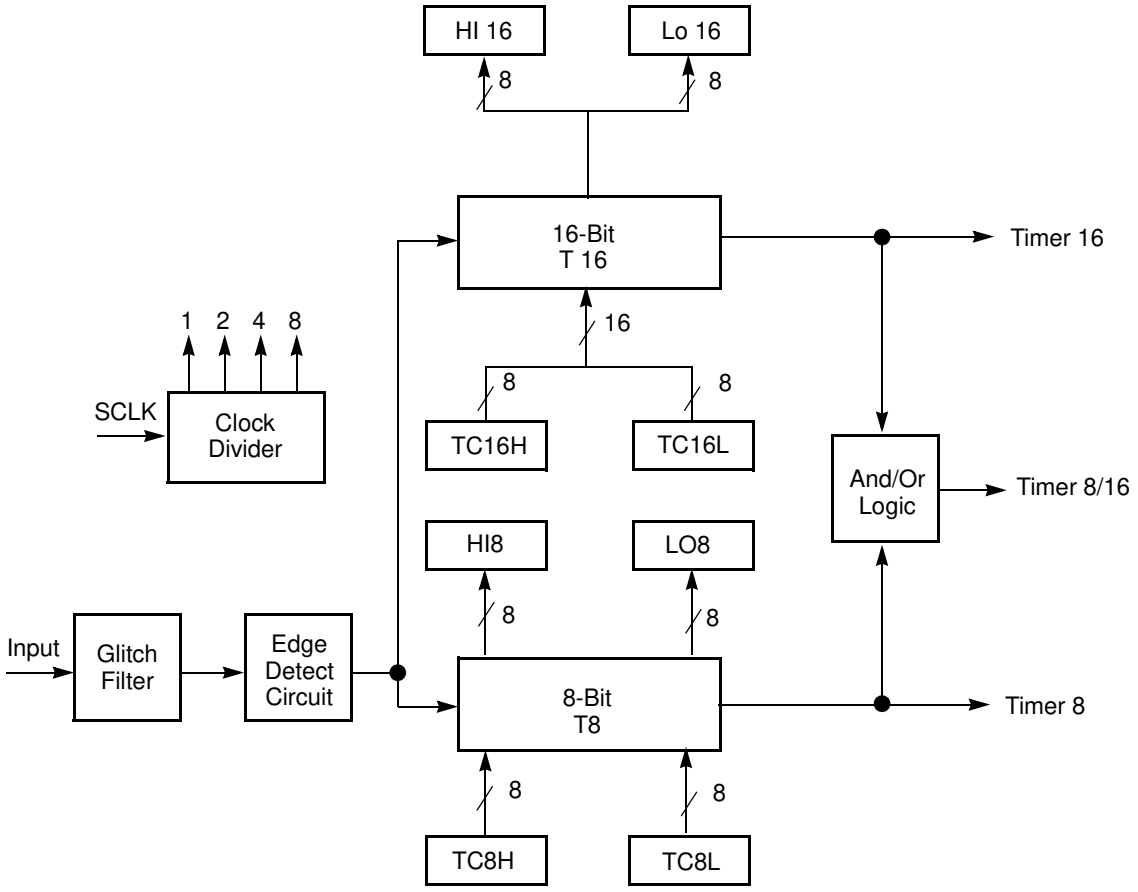

Figure 1. Counter/Timers Diagram

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Figure 2 shows the functional block diagram.

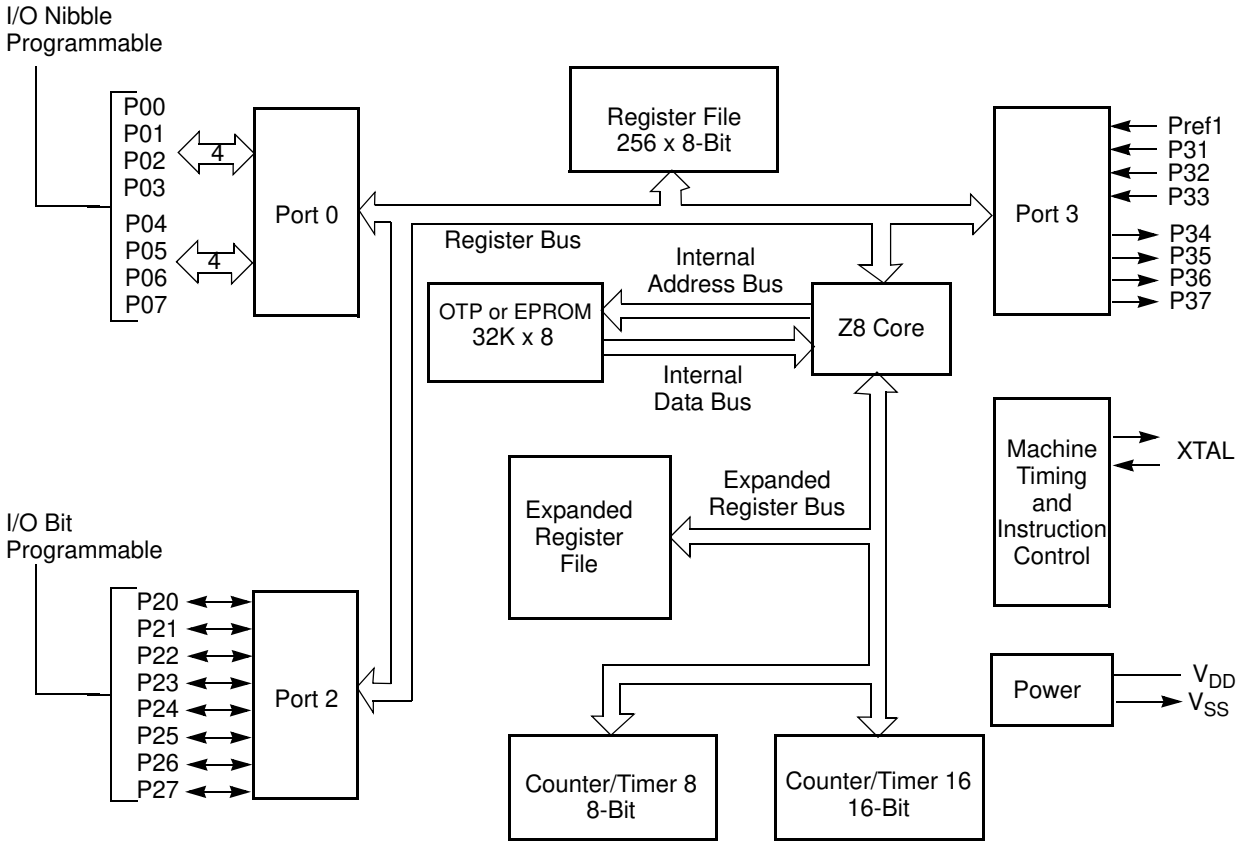

Figure 2. Functional Block Diagram

Pin Description

Figure 3 shows the pin assignment for the 28-pin dual in-line package (DIP)/small outline integrated circuit (SOIC). Table 2 identifies the pins.

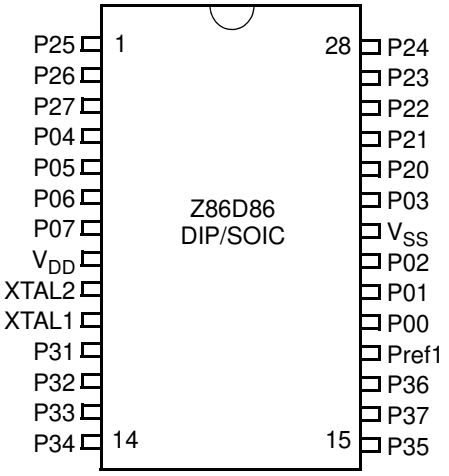

Figure 3. 28-Pin DIP/SOIC Pin Assignment

Table 2. 28-Pin DIP and SOIC Pin Identification

28-Pin DIP and SOIC	Standard Mode	Direction	Description
19	P00	Input/Output	Port 0 is nibble programmable.
20	P01	Input/Output	Port 0–3 can be configured as a
21	P02	Input/Output	mouse/trackball input.
23	P03	Input/Output	
4	P04	Input/Output	
5	P05	Input/Output	
6	P06	Input/Output	
7	P07	Input/Output	
24	P20	Input/Output	Port 2 pins are individually
25	P21	Input/Output	configurable as input or output.
26	P22	Input/Output	
27	P23	Input/Output	
28	P24	Input/Output	
1	P25	Input/Output	
2	P26	Input/Output	
3	P27	Input/Output	

Table 2. 28-Pin DIP and SOIC Pin Identification (Continued)

28-Pin DIP and SOIC	Standard Mode	Direction	Description
18	Pref1	Input	Analog ref input (must be pulled high externally, if not used)
11	P31	Input	IRQ2/modulator input
12	P32	Input	IRQ0
13	P33	Input	IRQ1
14	P34	Output	T8 output
15	P35	Output	T16 output
17	P36	Output	T8/T16 output
16	P37	Output	
10	XTAL1	Input	Crystal, oscillator clock
9	XTAL2	Output	Crystal, oscillator clock
8	V_{DD}		Power supply
22	V_{SS}		Ground

Absolute Maximum Ratings

Table 3 lists the absolute maximum ratings for the Z86D86 microcontroller.

Table 3. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{MAX}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65°	+150°	C
T_A	Oper. Ambient Temperature	0°	70°	C

Notes:
* Voltage on all pins with respect to GND

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 4).

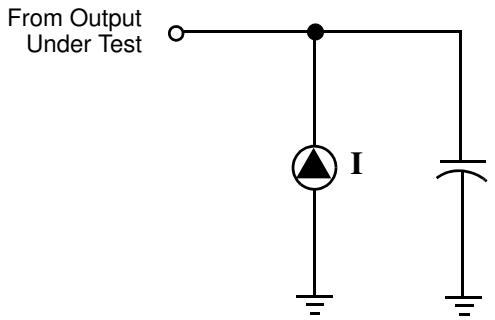

Figure 4. Test Load Diagram

Capacitance

Table 4 lists the capacitance for the Z86D86 microcontroller.

Table 4. Capacitance

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

Note: T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND.

DC Characteristics

Table 5 lists the direct current (DC) characteristics.

Table 5. DC Characteristics

			T_A = 0 °C to +70 °C				
Symbol	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage	2.3 V	0.8 V_{CC}	V_{CC} + 0.3	V	Driven by External Clock Generator	
		5.5 V	0.8 V_{CC}	V_{CC} + 0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.3 V	V_{SS}–0.3	0.2 V_{CC}	V	Driven by External Clock Generator	
		5.5 V	V_{SS}–0.3	0.2 V_{CC}	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.3 V	0.7 V_{CC}	V_{CC} + 0.3	V		
		5.5 V	0.7 V_{CC}	V_{CC} + 0.3	V		
V_{IL}	Input Low Voltage	2.3 V	V_{SS}–0.3	0.2 V_{CC}	V		
		5.5 V	V_{SS}–0.3	0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.3 V	V_{CC}–0.4		V	I_{OH} = –0.5 mA	
		5.5 V	V_{CC}–0.4		V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37, P00, and P01)	2.3 V	V_{CC}–0.8		V	I_{OH} = –7 mA	
		5.5 V	V_{CC}–0.8		V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.3 V		0.4	V	I_{OL} = 1.0 mA	
		5.5 V		0.4	V	I_{OL} = 4.0 mA	
V_{OL2}	Output Low Voltage	2.3 V		0.8	V	I_{OL} = 5.0 mA	1
		5.5 V		0.8	V	I_{OL} = 7.0 mA	1
V_{OL2}	Output Low Voltage (P00, P01, P36, and P37)	2.3 V		0.8	V	I_{OL} = 10 mA	
		5.5 V		0.8	V	I_{OL} = 10 mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.3 V		25	mV		
		5.5 V		25	mV		
V_{REF}	Comparator Reference Voltage	2.3 V	0	V_{CC}– 1.75	V		
		5.5 V	0	V_{CC}– 1.75	V		
I_{IL}	Input Leakage	2.3 V	–1	1	µA	V_{IN} = 0V, V_{CC}	
		5.5 V	–1	1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	2.3 V	–1	1	µA	V_{IN} = 0V, V_{CC}	
		5.5 V	–1	1	µA	V_{IN} = 0V, V_{CC}	

Table 5. DC Characteristics (Continued)

			T_A = 0 °C to +70 °C				
Symbol	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	2.3 V		10	mA	@ 8.0 MHz	2, 3
		5.5 V		15	mA	@ 8.0 MHz	2, 3
		2.3 V		250	µA	@ 32 kHz	2, 3, 4
		5.5 V		850	µA	@ 32 kHz	2, 3, 4
I_{CC1}	Standby Current (HALT Mode)	2.3 V		3	mA	V_{IN} = 0V, V_{CC} @ 8.0 MHz	2, 3
		5.5 V		5	mA	Same as above	2, 3
		2.3 V		2	mA	Clock Divide-by-16 @ 8.0 MHz	2, 3
		5.5 V		4	mA	Same as above	2, 3
I_{CC2}	Standby Current (STOP Mode)	2.3 V		8	µA	V_{IN} = 0V, V_{CC} WDT is not running	5, 6, 9
		5.5 V		10	µA	Same as above	5, 6, 9
		2.3 V		500	µA	V_{IN} = 0V, V_{CC} WDT is running	5, 6, 9
		5.5 V		800	µA	Same as above	5, 6, 9
I_{LV}	Standby Current (Low Voltage)			100	µA	Vcc < V_{LV}	7
T_{POR}	Power-On Reset	2.3 V	12	75	ms		
		5.5 V	5	20	ms		
V_{LV}	Low Voltage Protection		2	2.3	V	8 MHz max Ext. CLK Freq.	8
V_{LB}	Low Battery Detection Flag		2.4	2.7	V	V_{LB} = V_{LV} + 0.4 V	

Notes:
1. All outputs excluding P00, P01, P36, and P37
2. All outputs unloaded, inputs at rail
3. CL1 = CL2 = 100 pF
4. 32 kHz clock driver input
5. V_{LV} increases as the temperature decreases; inputs at V_{CC}
6. Oscillator stopped
7. Oscillator stops when V_{CC} falls below V_{LV} limit.
8. V_{LV} increases as the temperature decreases.
9. WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.

AC Characteristics

Figure 5 shows the timing diagram. Table 6 describes the alternating current (AC) characteristics.

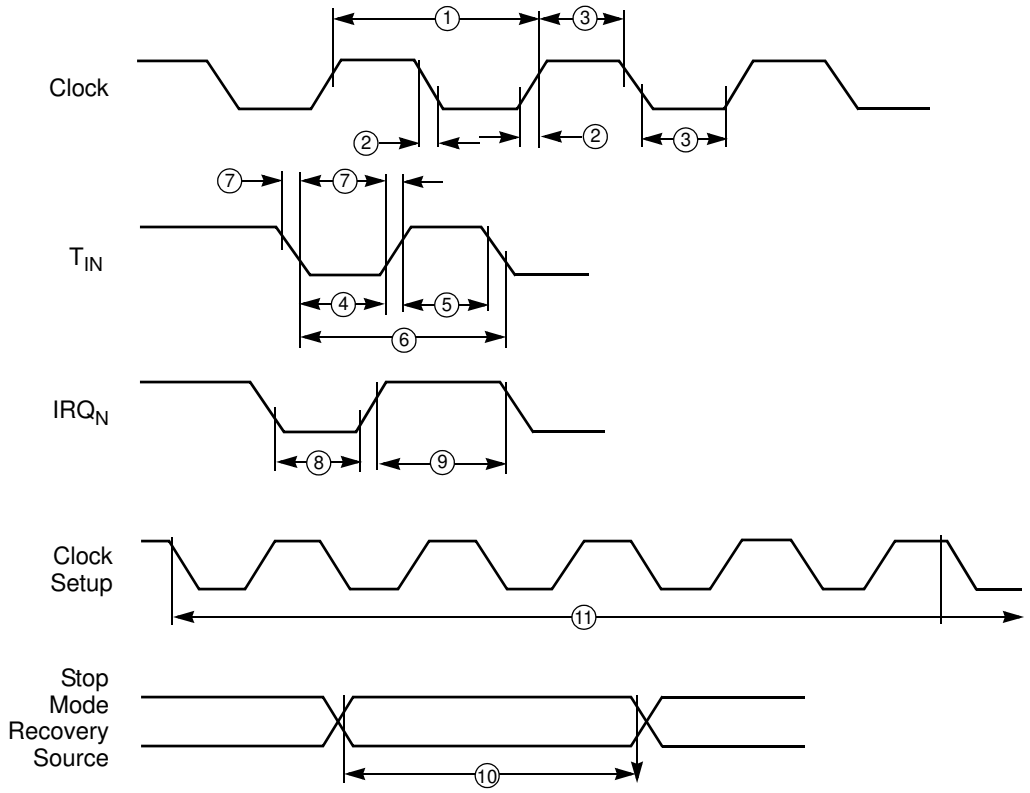

Figure 5. Timing Diagram

Table 6. AC Characteristics

				T_A = 0°C to +70°C 8.0 MHz				Stop-Mode Recovery (D1, D0)
Number	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**	
1	TpC	Input Clock Period	2.3 V	121	DC	ns	1	
			5.5 V	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.3 V		25	ns	1	
			5.5 V		25	ns	1	
3	TwC	Input Clock Width	2.3 V	37		ns	1	
			5.5 V	37		ns	1	
4	TwTinL	Timer Input Low Width	2.3 V	100		ns	1	
			5.5 V	70		ns	1	
5	TwTinH	Timer Input High Width	2.3 V	3TpC			1	
			5.5 V	3TpC			1	
6	TpTin	Timer Input Period	2.3 V	8TpC			1	
			5.5 V	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Times	2.3 V		100	ns	1	
			5.5 V		100	ns	1	
8A	TwIL	Interrupt Request Low Time	2.3 V	100		ns	1, 2	
			5.5 V	70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.3 V	5TpC			1, 2	
			5.5 V	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width Spec	2.3 V	12		ns		
			5.5 V	12		ns		
12	Twdt	Watch-Dog Timer Delay Time	2.3 V	12		ms	5	0, 0
			5.5 V	5		ms	5	
			2.3 V	24		ms	5	0, 1
			5.5 V	10		ms	5	
			2.3 V	48		ms	5	1, 0
			5.5 V	20		ms	5	
			2.3 V	192		ms	5	1, 1
			5.5 V	80		ms	5	

Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31)
3. N/A
4. SMR – D5 = 0.
5. For internal RC oscillator

Pin Functions (Standard Mode)

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator input. An external single-phase clock to the on-chip oscillator input is also an option.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open drain controlled by bit D2 in the PCON register.

If one or both nibbles are required for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An EPROM option is available to program 0.4 V_{CC} CMOS trip inputs on P00–P03. This allows direct interface to mouse/trackball IR sensors.

An optional 200 ±50%KΩs pull-up transistor is available as a mask option on all Port 0 bits with nibble select. See Figure 6.

Note: Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

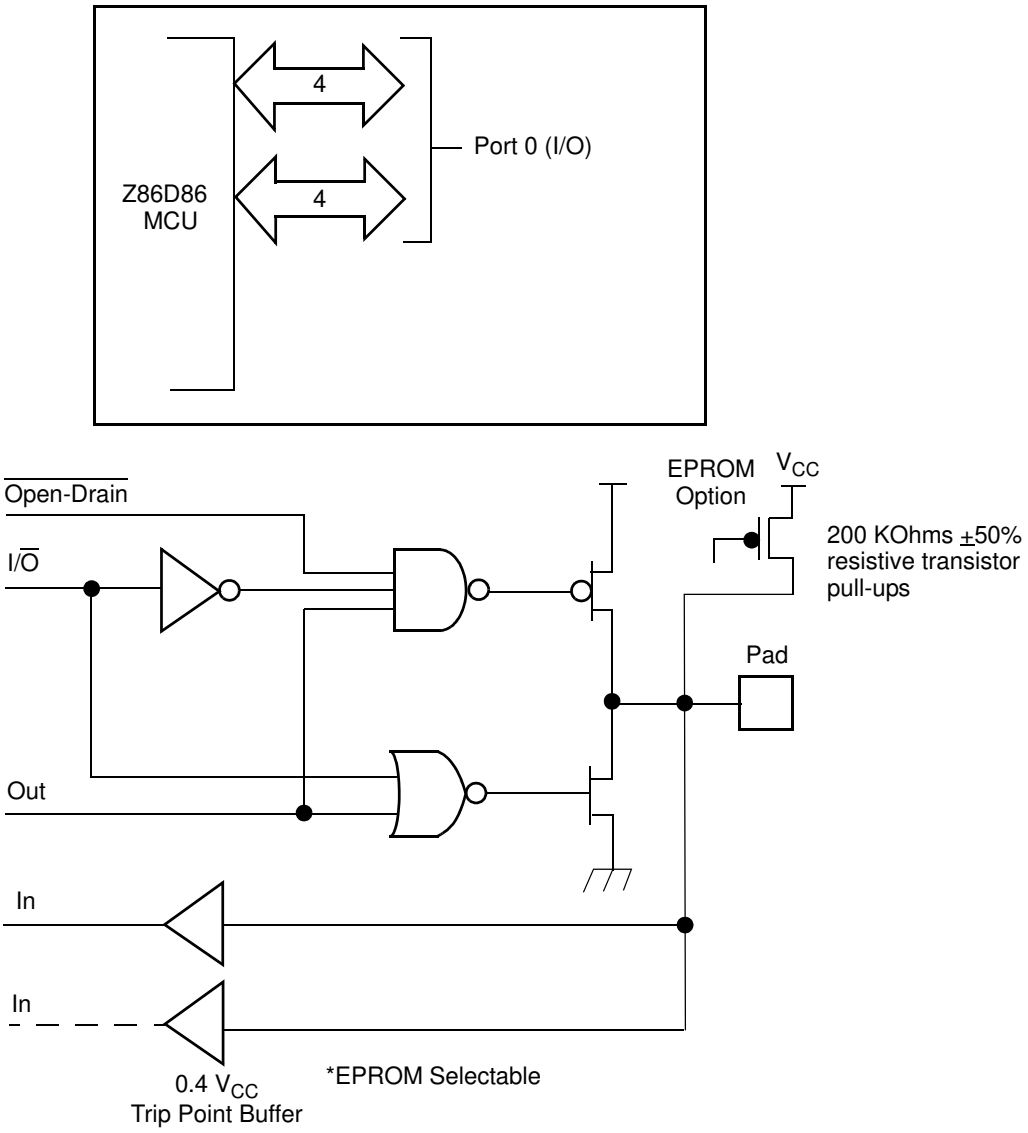

Figure 6. Port 0 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight 200 KΩ (±50%) pull-up transistors on this port. Bits programmed as outputs are

globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and an AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode. See Figure 7.

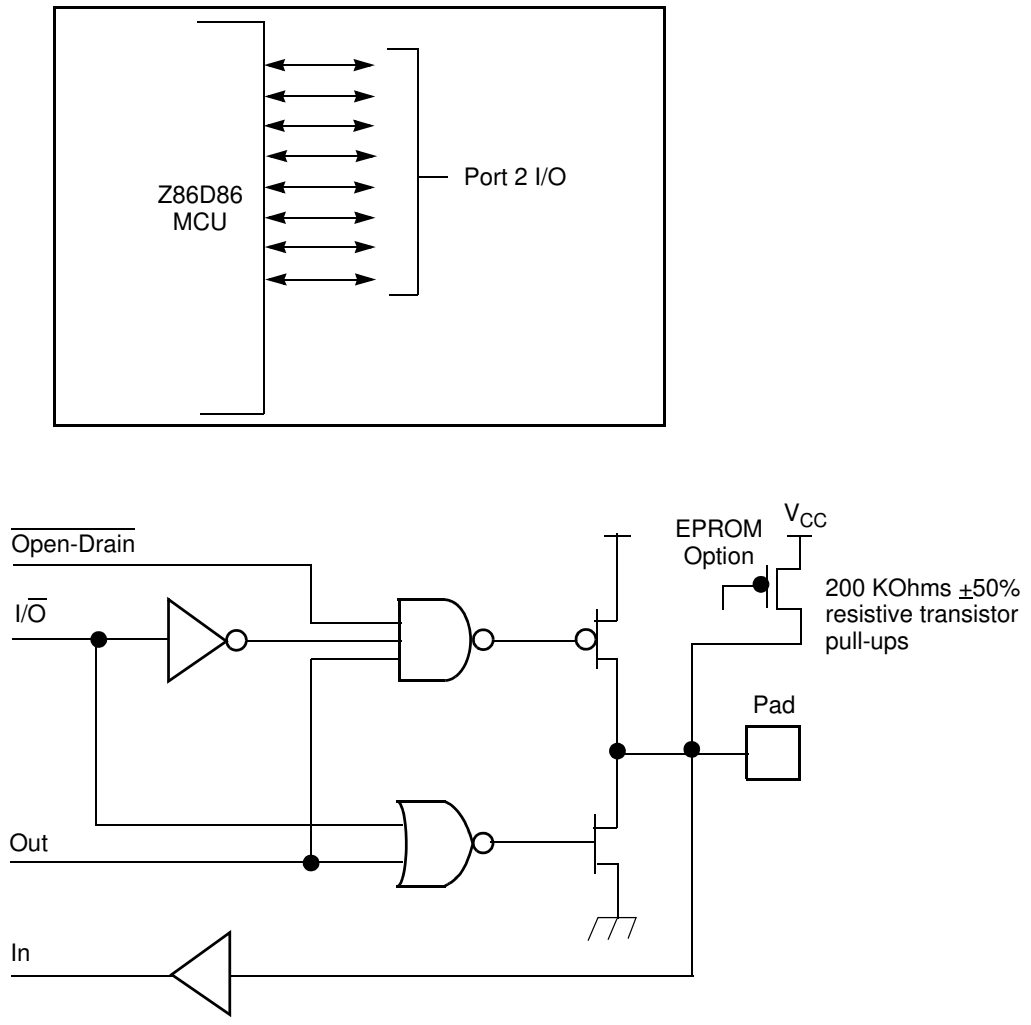

Figure 7. Port 2 Configuration

Port 3 (P37–P31)

Port 3 is a 7-bit, CMOS-compatible fixed I/O port (see Figure 8). Port 3 consists of three fixed input (P33–P31) and four fixed output (P37–P34) ports, and each can be configured under software control for interrupt, and output from the counter/

timers. P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

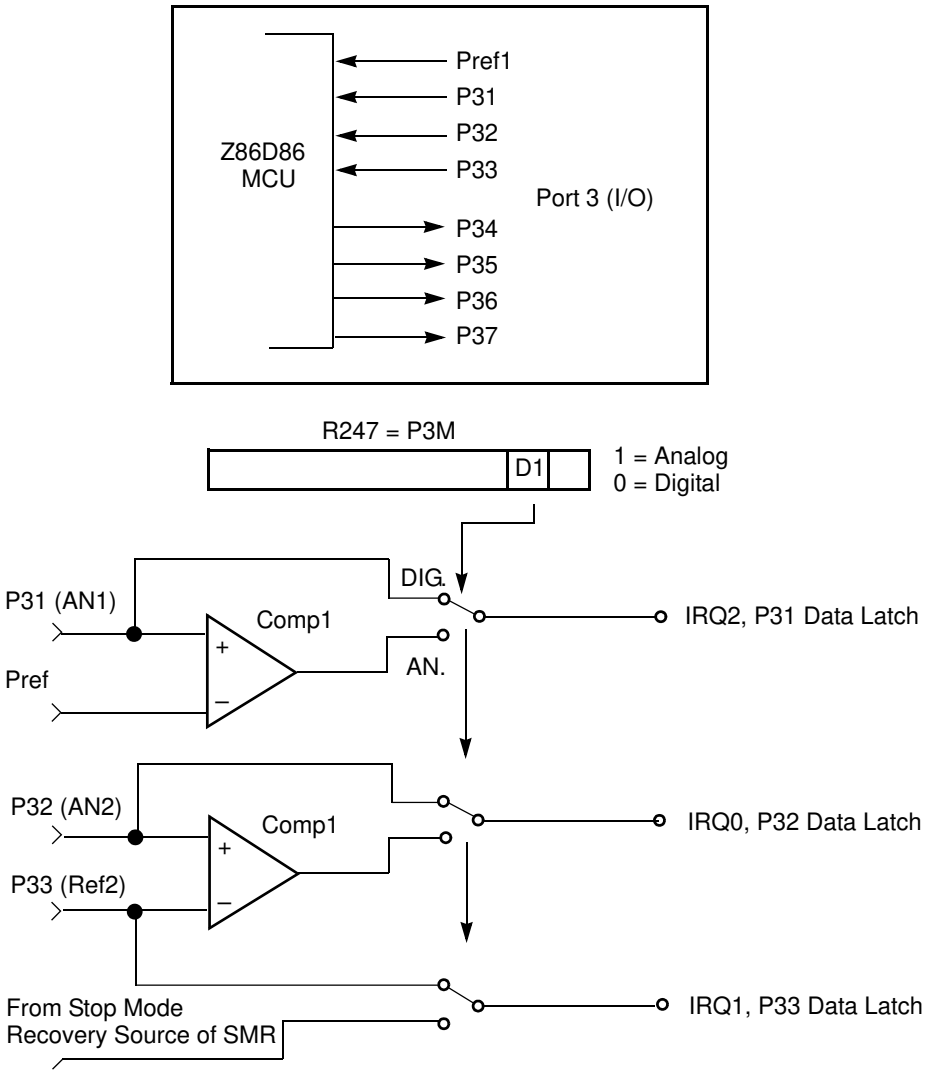

Figure 8. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge-triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the counter/timer edge-detection circuit is through P31 or P20 (see “CTR1 Counter/Timer T8 and

T16 Common Control Register" on page 39). Other edge-detect and IRQ modes are described in Table 7.

Table 7. Pin Assignments

Pin	I/O	C/T	Comp.	Int.
Pref1			RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for the counter/timers and the AND/OR logic. Control is performed by programming bits D5–D4 of CTR1 and bit 0 of CTR2.

Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 8 on page 15. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

Note: Comparators are powered down by entering STOP Mode. For P31–P33 to be used in a Stop-Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These outputs can be programmed to output on P34 and P37 through the PCON register (Figure 9).

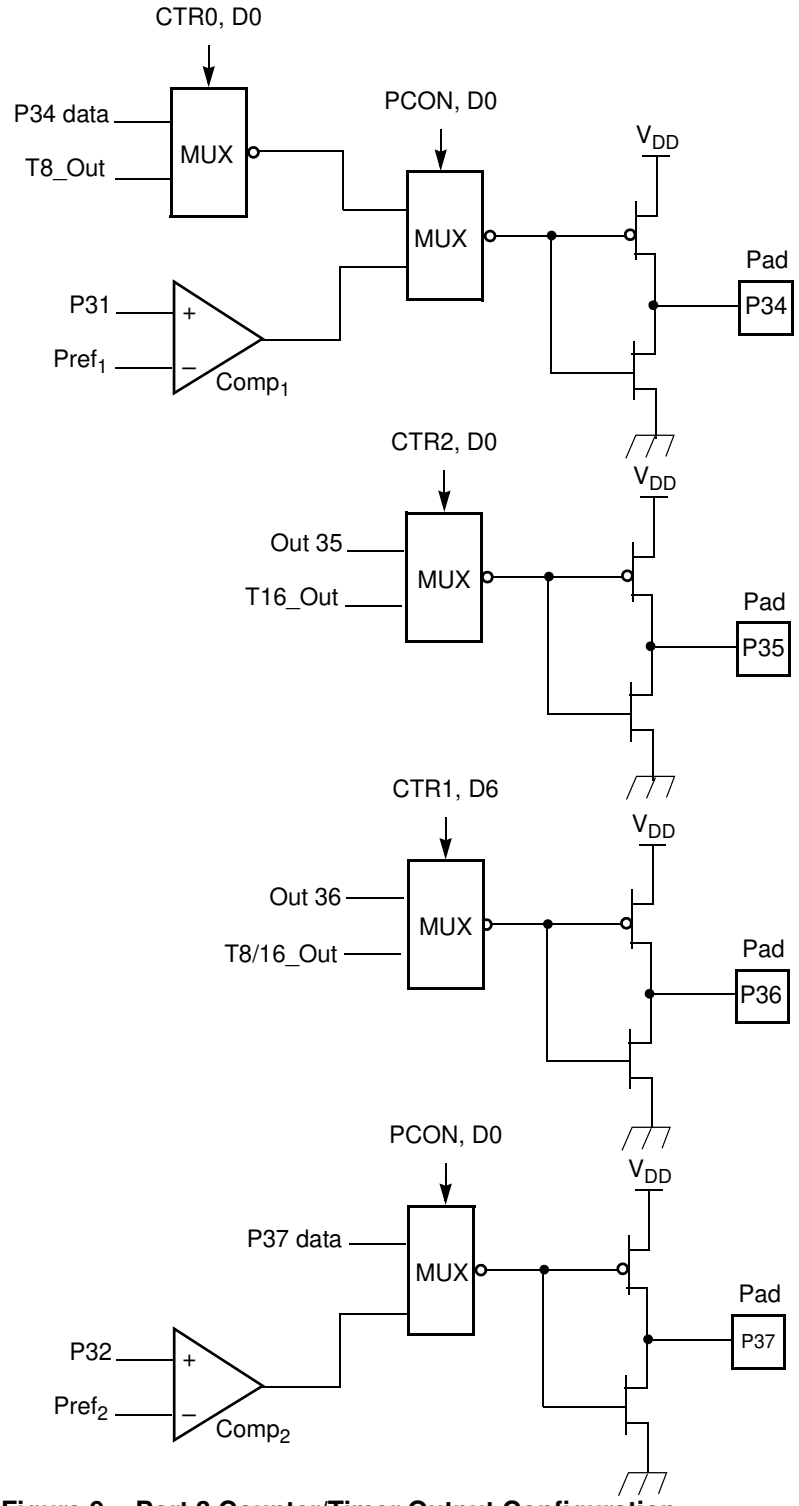

Figure 9. Port 3 Counter/Timer Output Configuration