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Z86E03/E06

CMOS Z8® 8-BIT OTP CCP™
CONSUMER CONTROLLER PROCESSORS

FEATURES

- The Z86E03/E06 Devices Have the Following General Characteristics:

Part	ROM	RAM	Speed
Z86E03	512 bytes	60	8 MHz
Z86E06	1 Kbyte	124	12 MHz

- 18-Pin Package (DIP, SOIC)
- 3.0 to 5.5 Volt Operating Range
- Operating Temperature: -40°C to +105°C
- Clock Speeds up to 8 MHz (E03) and 12 MHz (E06)
- Fast Instruction Pointer: 1.5 μ s @ 8 MHz (E03); 1.0 μ s @ 12 MHz (E06)
- Multiple Expanded Register File Control Registers and Two SPI Registers (Z86E06 only)
- One/Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Permanent Watch-Dog Timer Option
- Power-On Reset Timer
- Programmable Auto Latches
- Two Standby Modes: STOP and HALT
- Two Comparators with Programmable Interrupt Polarity
- 14 Input/Output Lines (Two with Comparator Inputs)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.
- Serial Peripheral Interface (SPI) (Z86E06 Only)
- Software Programmable Low EMI Mode
- EPROM Protect Option

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GENERAL DESCRIPTION

Zilog's Z86E03/E06 OTP (One-Time Programmable) CCP™ (Consumer Controller Processors) are members of the Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 512 and 1K bytes of EPROM and 60 and 124 bytes of general-purpose RAM, respectively. These low cost, low power consumption 18-pin CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86E03/E06 architecture is characterized by Zilog's 8-bit microcontroller core with the addition of an Expanded Register File to allow easy access to register mapped peripheral and I/O circuits. The Z86E03/E06 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, and industrial applications.

For applications demanding powerful I/O capabilities, the Z86E03/E06 provides 14 pins dedicated to input and output. These lines are grouped into two ports and are configurable under software control to provide timing, status signals, or parallel I/O.

GENERAL DESCRIPTION (Continued)

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File (Figure 1). The Register File is composed of 60/124 bytes of General-Purpose Registers, two I/O Port registers, and thirteen/fifteen Control and Status registers. The Expanded Register File consists of three control registers in the Z86E03, and four control registers, a SPI Receive Buffer, and a SPI compare register in the Z86E06.

With powerful peripheral features such as on-board comparators, counter/timer(s), Watch-Dog Timer (WDT), and serial peripheral interface (E06 only), the Z86E03/E06

meets the needs of a variety of sophisticated controller applications.

Notes:

All Signals with a preceding front slash, '/', are active Low, e.g. B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

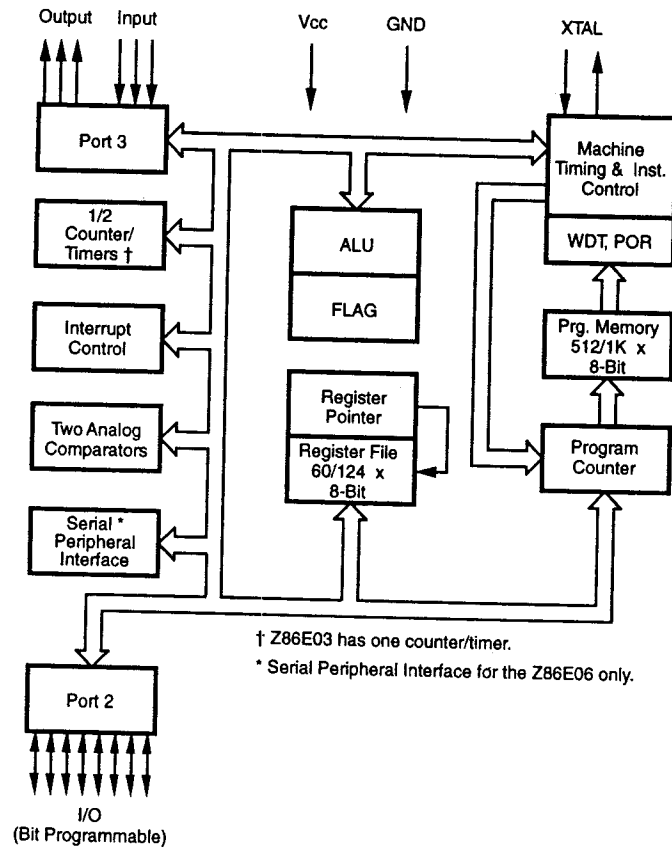


Figure 1. Z86E03/E06 Functional Block Diagram

PIN DESCRIPTION

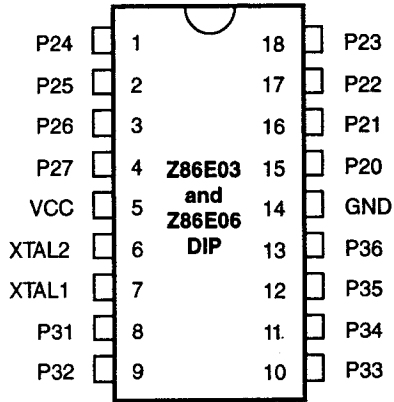


Table 1. 18-Pin DIP and SOIC Pin Identification

No	Symbol	Function	Direction
1-4	P24-27	Port 2, pins 4, 5, 6, 7	In/Output
5	V _{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-33	Port 3, pins 1, 2, 3	Fixed Input
11-13	P34-36	Port 3, pins 4, 5, 6	Fixed Output
14	GND	Ground	
15-18	P20-23	Port 2, pins 0, 1, 2, 3	In/Output

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Figure 2. 18-Pin DIP Pin Configuration

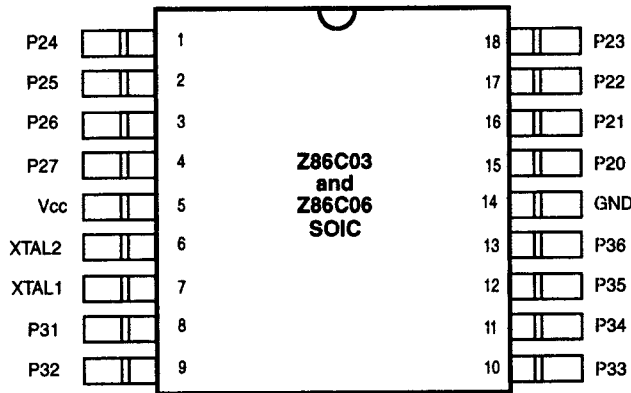


Figure 3. 18-Pin SOIC Pin Configuration

PIN FUNCTIONS

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered and contain Auto Latches. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 4a., 4b., and 4c.). Low EMI output buffers can be globally programmed by the software. In addition, when the SPI is enabled, P20 functions as data-in (DI), and P27 functions as data-out (DO) for the SPI (SPI on the Z86E06 only).

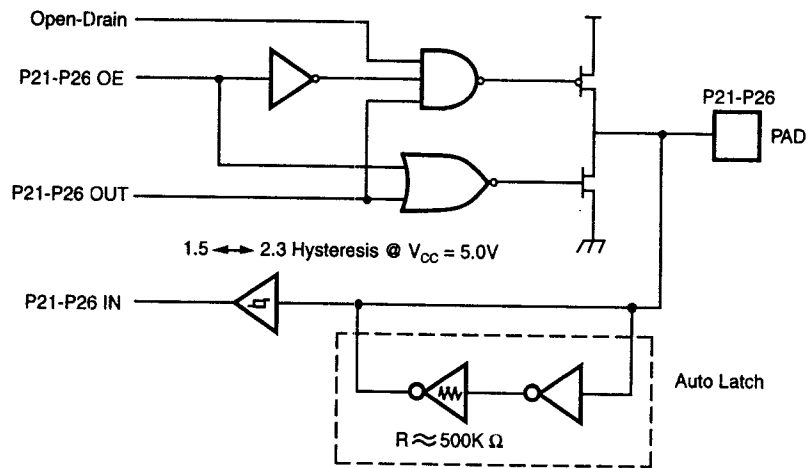
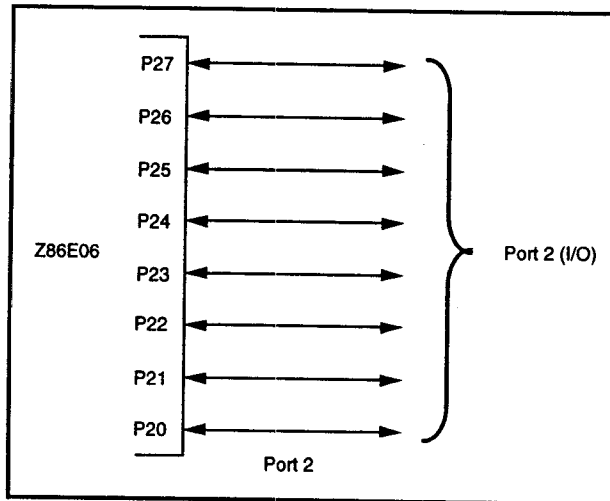


Figure 4a. Port 2 Configuration (Z86E06)

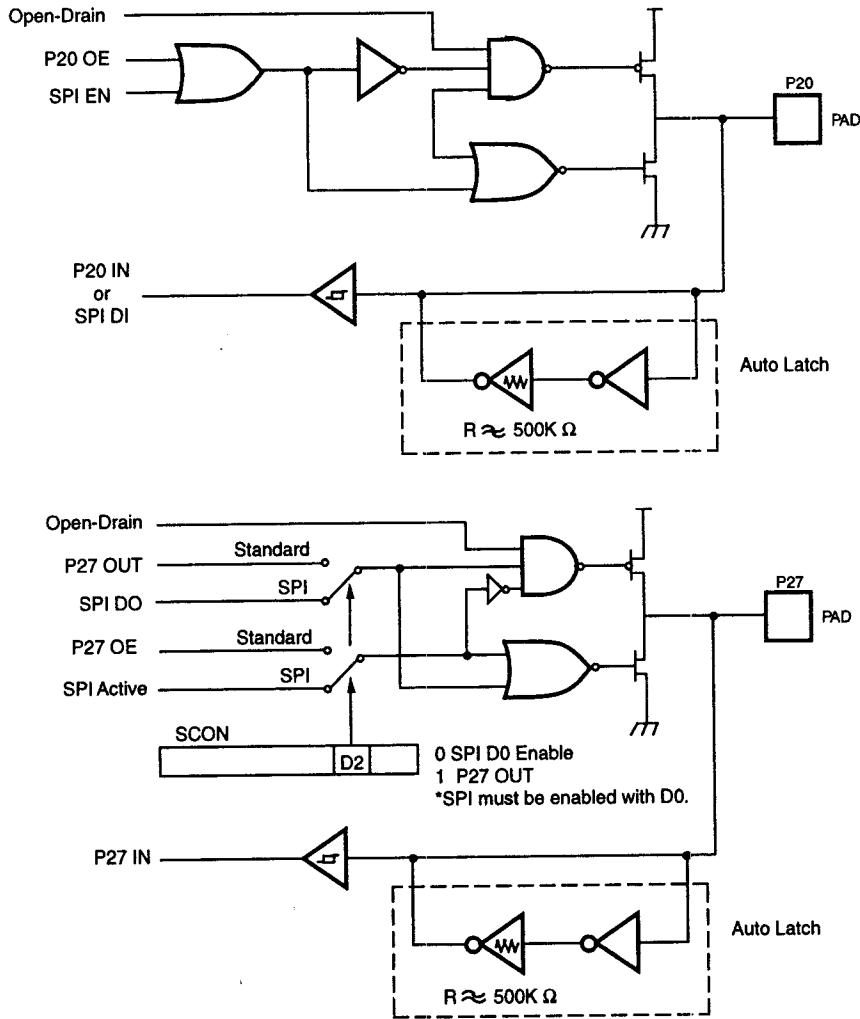


Figure 4b. Port 2 Configuration (Z86E06)

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PIN FUNCTIONS (Continued)

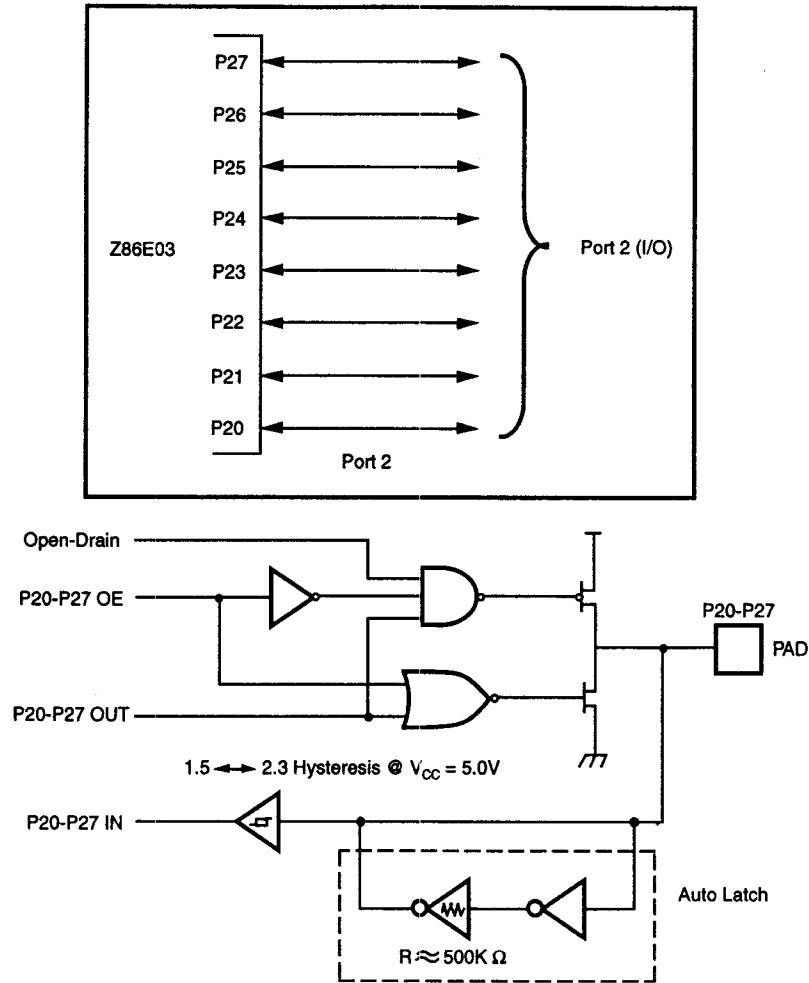


Figure 4c. Port 2 Configuration (Z86E03)

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Port 3 (P36-P31). Port 3 is a 6-bit, CMOS compatible port. These six lines consist of three fixed inputs (P31-P33) and three fixed outputs (P34-P36). Pins P31, P32, and P33 are standard CMOS inputs (no auto latches) and pins P34, P35, and P36 are push-pull outputs. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M-bit D1). Pins P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input when the analog mode is selected. P33 is a falling edge interrupt input only.

Note: P33 is available as an interrupt input only in the digital mode. P31 and P32 are valid interrupt inputs and P31 is the T_{IN} input when the analog or digital input mode is selected.

The outputs from the analog comparator can be globally programmed to output from P34 and P35 by setting PCON (F) 00 bit D0 = 1.

Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}).

In the Z86E06, pin P34 can also be configured as SPI clock (SK), input and output, and pin P35 can be configured as Slave Select (SS) in slave mode only, when the SPI is enabled (Figures 5a and 5b).

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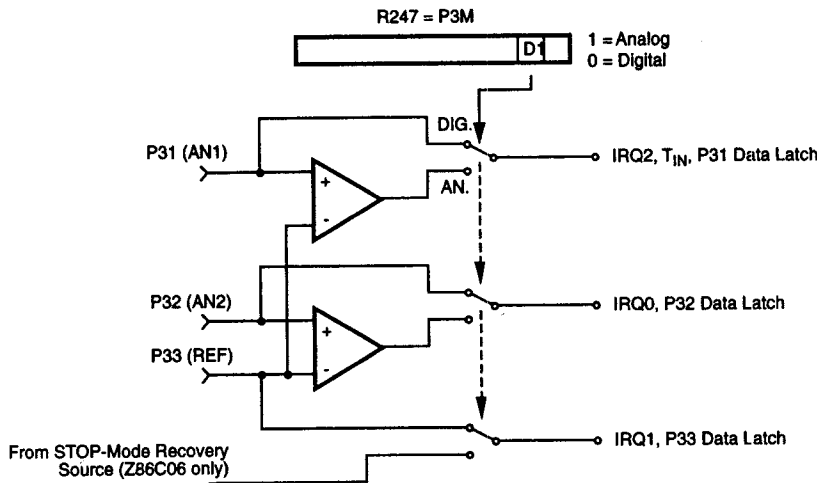
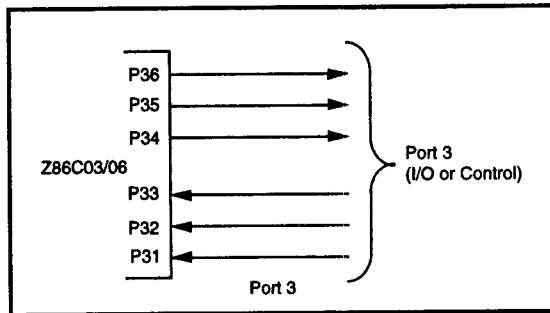


Figure 5a. Port 3 Configuration

PIN FUNCTIONS (Continued)

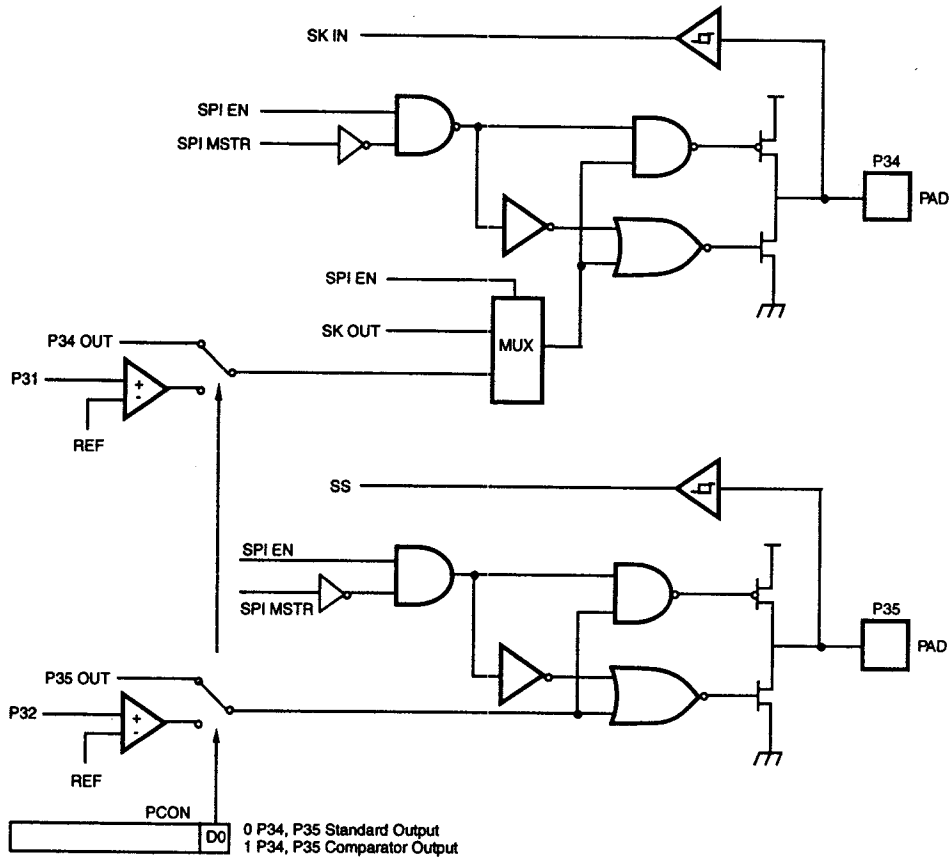


Figure 5b. Port 3 Configuration (Z86E06)

Low EMI Emission. The Z86E03/E06 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns (typical).
- Low EMI output drivers resistance of 200 ohms (typical).
- Low EMI oscillator.

- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz (250 ns cycle time) when the low EMI oscillator is selected and SCLK = External (SMR Register Bit D1=1).

Comparator Inputs. Port 3 Pin P31 and P32 each have a comparator front end. The comparator reference voltage pin P33 is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In digital mode, Pin P33 can be used as a P33 register input or IRQ1 source.

FUNCTIONAL DESCRIPTION

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- STOP-Mode Recovery Source
- Low Voltage Protection

Having the Auto Power-On Reset circuitry built-in, the Z86E03/E06 does not require an external reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles.

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a STOP-Mode Recovery operation.

Program Memory. Z86E03/E06 can address up to 512/1K bytes of internal program memory (Figure 6). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 511/1023 consists of on-chip, user program mask ROM.

EPROM Protect. The 512/1K bytes of Program Memory is mask programmable. A EPROM protect feature will prevent "dumping" of the EPROM contents by inhibiting execution of the LDC and LDCI instructions to program memory in all modes.

EPROM protect is EPROM-programmable. It is selected by the customer when the ROM code is submitted. **Selecting ROM protect disables the LDC and LDCI instructions in all modes. ROM lookup tables are not supported in this mode.**

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as

16 groups of 16 registers per group (Figure 7). These register groups are known as the Expanded Register File (ERF).

Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of the RP register select the working register group (Figure 7). For the Z86E03, three system configuration registers reside in the ERF address space Bank F. For the Z86E06, three system configuration registers reside in the ERF address space Bank F, while three SPI registers reside in Bank C. The rest of the ERF address space is not physically implemented and is open for future expansion.

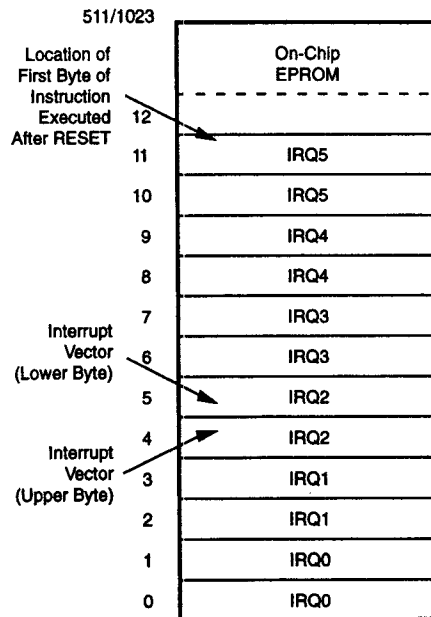


Figure 6. Program Memory Map

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FUNCTIONAL DESCRIPTION (Continued)

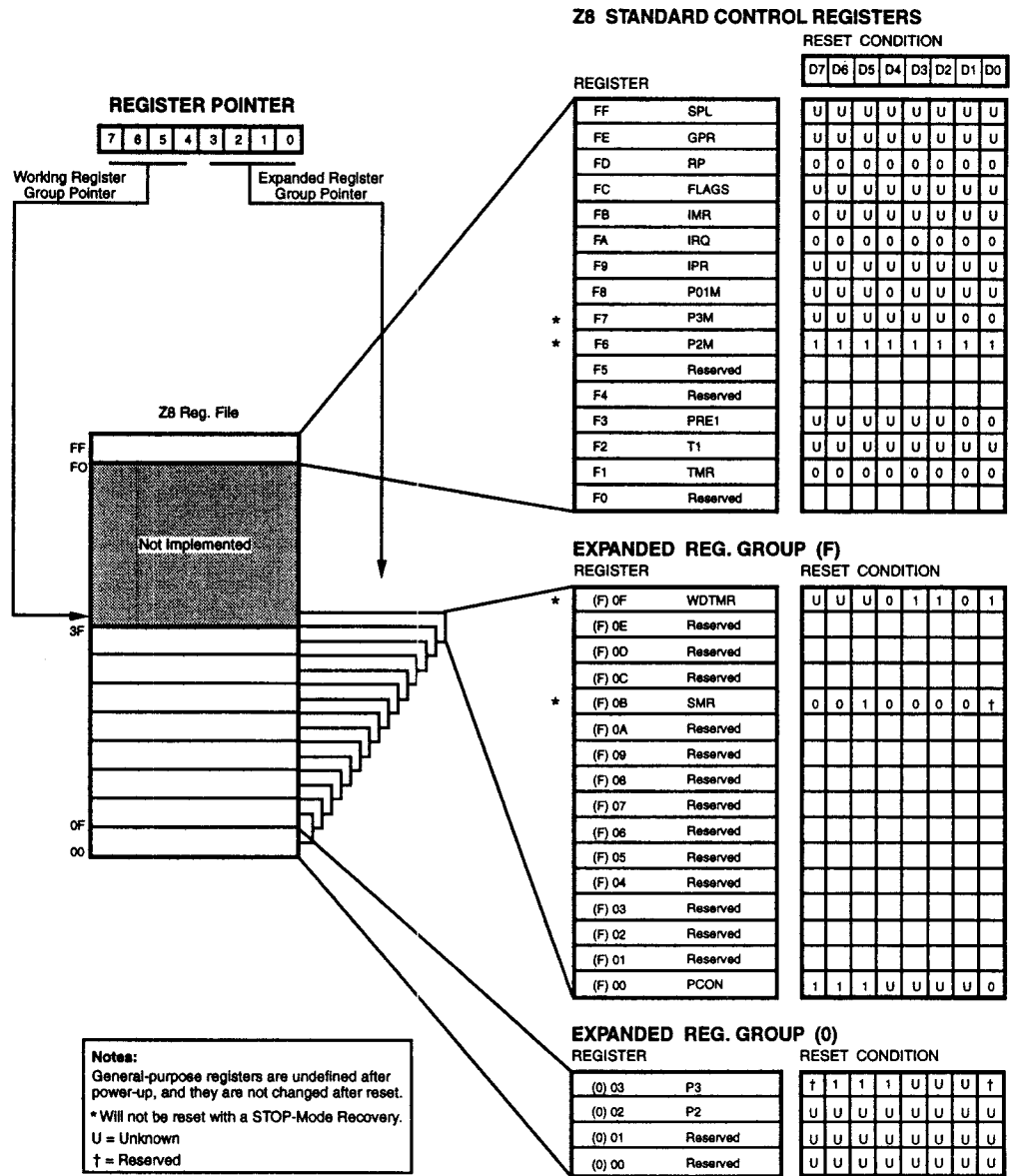
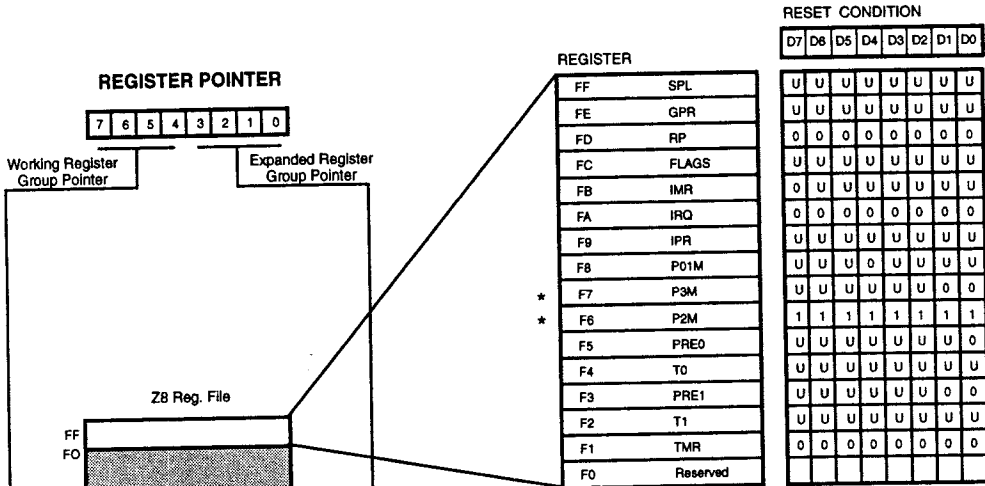


Figure 7a. Expanded Register File Architecture (Z86E03)

Z8 STANDARD CONTROL REGISTERS



REGISTER	
FF	SPL
FE	GPR
FD	RP
FC	FLAGS
FB	IMR
FA	IRQ
F9	IPR
F8	P01M
F7	P3M
* F6	P2M
F5	PRE0
F4	T0
F3	PRE1
F2	T1
F1	TMR
F0	Reserved

RESET CONDITION							
D7	D6	D5	D4	D3	D2	D1	D0
U	U	U	U	U	U	U	U
U	U	U	U	U	U	U	U
0	0	0	0	0	0	0	0
U	U	U	U	U	U	U	U
0	U	U	U	U	U	U	U
0	0	0	0	0	0	0	0
U	U	U	U	U	U	U	U
U	U	U	0	U	U	U	U
U	U	U	U	U	U	0	0
1	1	1	1	1	1	1	1
U	U	U	U	U	U	U	0
U	U	U	U	U	U	U	U
U	U	U	U	U	U	0	0
U	U	U	U	U	U	U	U
0	0	0	0	0	0	0	0

EXPANDED REG. GROUP (F)

REGISTER	
* (F) 0F	WDTMR
(F) 0E	Reserved
(F) 0D	Reserved
(F) 0C	Reserved
** (F) 0B	SMR
(F) 0A	Reserved
(F) 09	Reserved
(F) 08	Reserved
(F) 07	Reserved
(F) 06	Reserved
(F) 05	Reserved
(F) 04	Reserved
(F) 03	Reserved
(F) 02	Reserved
(F) 01	Reserved
(F) 00	PCON

RESET CONDITION							
D7	D6	D5	D4	D3	D2	D1	D0
U	U	U	0	1	1	0	1
0	0	1	0	0	0	0	0
1	1	1	U	U	U	U	0

EXPANDED REG. GROUP (C)

REGISTER	
(C) 02	SCON
(C) 01	RxBUF
(C) 00	SCOMP

RESET CONDITION							
D7	D6	D5	D4	D3	D2	D1	D0
U	U	U	U	0	0	0	0
U	U	U	U	U	U	U	U
0	0	0	0	0	0	0	0

EXPANDED REG. GROUP (0)

REGISTER	
(0) 03	P3
(0) 02	P2
(0) 01	Reserved
(0) 00	Reserved

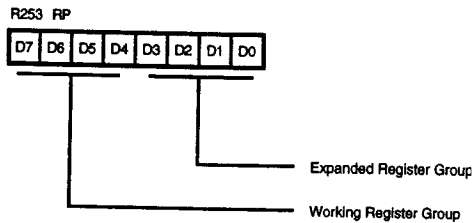
RESET CONDITION							
D7	D6	D5	D4	D3	D2	D1	D0
†	1	1	1	U	U	U	†
U	U	U	U	U	U	U	U
U	U	U	U	U	U	U	U
U	U	U	U	U	U	U	U

Notes:
 General-purpose registers are undefined after power-up, and they are not changed after reset.
 * Will not be reset with a STOP-Mode Recovery
 ** Will not be reset with a STOP-Mode Recovery, except Bit D0.
 U = Unknown
 † = Reserved

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Figure 7b. Expanded Register File Architecture (Z86E06)

FUNCTIONAL DESCRIPTION (Continued)



Note: Default Setting After Reset = 00000000

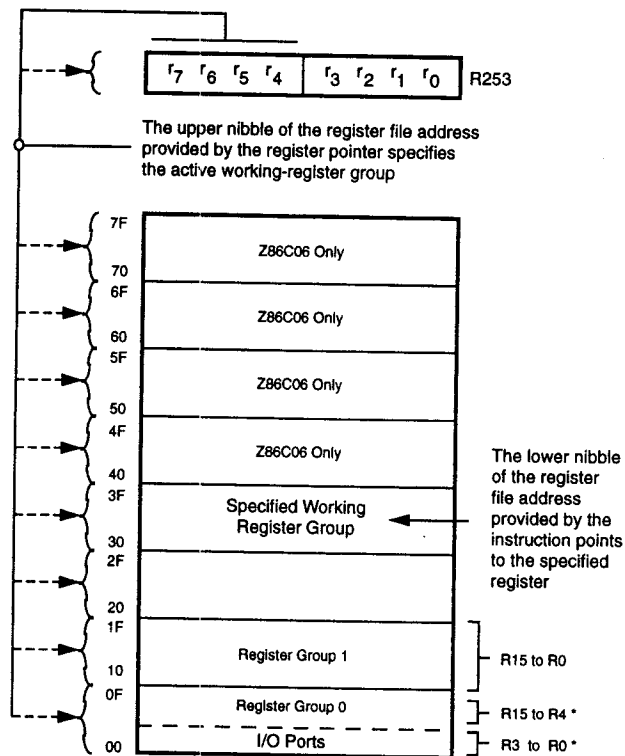
Figure 8. Register Pointer Register

Register File. The Register File consists of two I/O port registers, 60/124 general-purpose registers, and 13/15 control and status registers. The Z86E03 General-Purpose Register file ranges from address 00 to 3F while the Z86E06 General-Purpose Register file ranges from ad-

dress 00 to 7F (see Figure 9). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 9). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

Stack. An 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60/124 general-purpose registers.



* Expanded Register Group (0) is selected in this figure by handling bits D3 to D0 as "0" in Register R253 (RP).

Figure 9. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler (Z86E03 only has T1). The T1

prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 10).

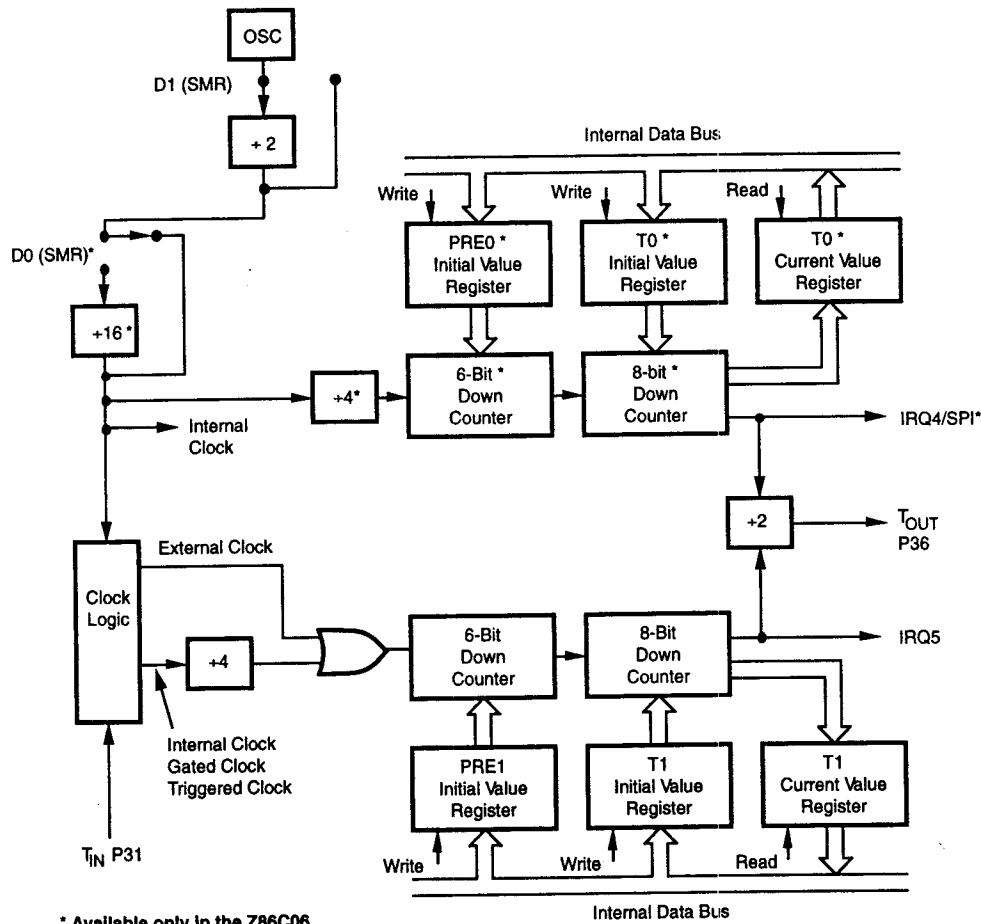


Figure 10. Counter/Timer Block Diagram

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FUNCTIONAL DESCRIPTION (Continued)

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated. Note that IRQ4 is software-generated in the Z86E03.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an exter-

nal signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 serves as a timer output (T_{out}) through which T0 (E06 only), T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1 (E06 only). The T_{in} mode is enabled by setting PRE1 bit D1 (R243) to 0.

Interrupts. The Z86E03/E06 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 11). The six sources are divided as follows; three sources are claimed by Port 3 lines P31-P33, two sources in the counter/timers, and one source for the SPI. The Interrupt Mask Register globally or singularly enables or disables the six interrupt requests (Table 2).

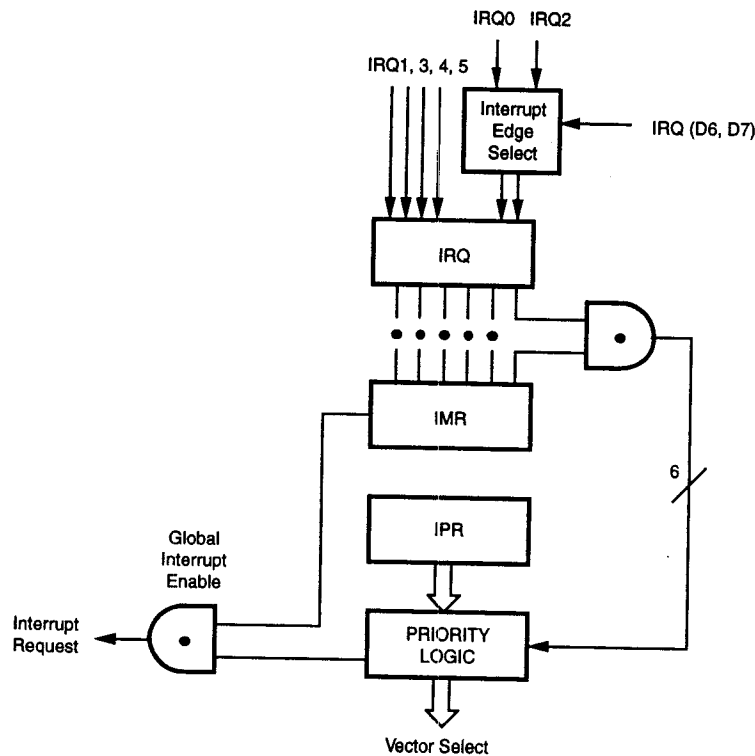


Figure 11. Interrupt Block Diagram

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	IRQ 0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ 1	IRQ 1	2, 3	External (P33), Falling Edge Triggered
IRQ 2	IRQ 2, T _{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ 3	IRQ 3	6, 7	Software Generated, SPI Receive
IRQ 4	TO/IRQ 4	8, 9	Internal for E06 and Software Generated for E03
IRQ 5	TI	10, 11	Internal

Note:

When enabled, the SPI receive interrupt is mapped to IRQ3 in the Z86E06.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E03/E06 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service. In the Z86E06, when the SPI is disabled, IRQ3 has no hardware source but can be invoked by software (write to IRQ3 Register). When the SPI is enabled, an interrupt will be mapped to IRQ3 after a byte of data has been received by the SPI Shift Register.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

The programming bits for the INTERRUPT EDGE SELECT are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

Table 3. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:

 F = Falling Edge
 R = Rising Edge

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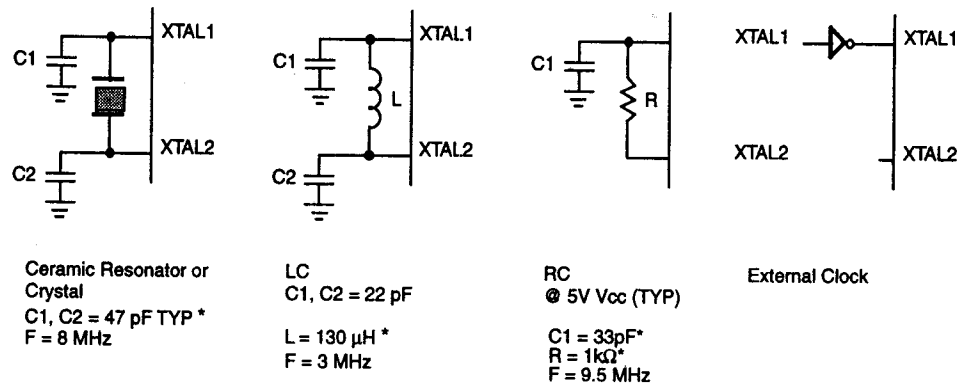
FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86E03/E06 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 8 MHz/12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values (capacitance between 10 pF to 300 pF) from each pin directly to the device ground (pin 14). The layout is important to reduce ground noise injection.

The RC oscillator option is EPROM-programmable, to be selected by the customer at the time the Z8 is EPROM programmed. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 12).

In addition, a special feature has been incorporated into the Z86E03/E06; in low EMI noise mode (bit 7 of PCON register=0) with the RC option selected, the oscillator is targeted to consume considerably less I_{cc} current at frequencies of 10 kHz or less.



* Preliminary Value Including Pin Parasitics

Figure 12. Oscillator Configuration

Power-On Reset. A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{cc} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the three conditions:

- Power-Fail to Power-OK Status
- STOP-Mode Recovery (If D5 of SMR=1)
- WDT Time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after STOP mode recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. Will turn off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device may be recovered by interrupts either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP mode is terminated by a RESET only, either by WDT time-out, POR, SPI compare; or SMR recovery. This causes the processor to restart the application program at address 000C (HEX). Note, the crystal remains active in STOP mode if bits 3 and 4 of the WDTMR are enabled. In this mode, only the Watch-Dog Timer runs in STOP mode.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, i.e.:

- FF NOP ; clear the pipeline
- 6F STOP ; enter STOP mode
- or
- FF NOP ; clear the pipeline
- 7F HALT ; enter HALT mode

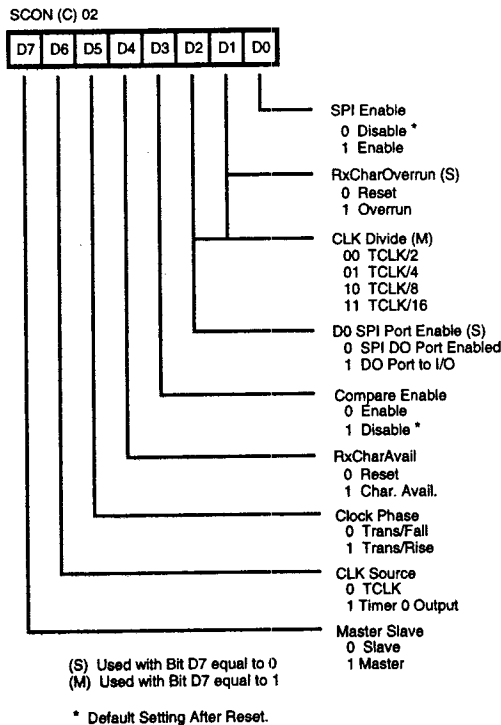
Serial Peripheral Interface (SPI)—Z86E06 Only. The Z86E06 incorporates a serial peripheral interface for communication with other microcontrollers and peripherals. **The SPI does not exist on the Z86E03.** The SPI includes features such as STOP-Mode Recovery, Master/Slave selection, and Compare mode. Table 4 contains the pin configuration for the SPI feature when it is enabled. The SPI consists of four registers: SPI Control Register (SCON), SPI Compare Register (SCOMP), SPI Receive/Buffer Register (RxBUF), and SPI Shift Register. SCON is located in bank (C) of the Expanded Register Group at address 02.

Table 4. SPI Pin Configuration

Name	Function	Pin Location
DI	Data-In	P20
DO	Data-Out	P27
SS	Slave Select	P35
SK	SPI Clock	P34

The SPI Control Register (SCON) (Figure 13) is a read/write register that controls; Master/Slave selection, interrupts, clock source and phase selection, and error flag. Bit 0 enables/disables the SPI with the default being SPI disabled. A 1 in this location will enable the SPI, and a 0 will disable the SPI. Bits 1 and 2 of the SCON register in Master mode select the clock rate. The user may choose whether internal clock is divide-by-2, -4, -8, or -16. In slave mode, Bit 1 of this register flags the user if an overrun of the RxBUF Register has occurred. The RxCharOverrun flag is only reset by writing a 0 to this bit. In slave mode, bit 2 of the

Control Register disables the data-out I/O function. If a 1 is written to this bit, the data-out pin is released to its original port configuration. If a 0 is written to this bit, the SPI shifts out one bit for each bit received. Bit 3 of the SCON Register enables the compare feature of the SPI, with the default being disabled. When the compare feature is enabled, a comparison of the value in the SCOMP Register is made with the value in the RxBUF Register. Bit 4 signals that a receive character is available in the RxBUF Register.



**Figure 13. SPI Control Register (SCON)
(Z86E06 Only)**

If the associated IRQ3 is enabled, an interrupt is generated. Bit 5 controls the clock phase of the SPI. A 1 in Bit 5 allows for receiving data on the clock's falling edge and transmitting data on the clock's rising edge. A 0 allows receiving data on the clock's rising edge and transmitting on the clock's falling edge. The SPI clock source is defined in bit 6. A 1 uses Timer0 output for the SPI clock, and a 0 uses TCLK for clocking the SPI. Finally, bit 7 determines whether the SPI is used as a Master or a Slave. A 1 puts the SPI into Master mode and a 0 puts the SPI into Slave mode.

2

FUNCTIONAL DESCRIPTION (Continued)

SPI Operation (Z86E06 only). The SPI is used in one of two modes: either as system slave, or as system master. Several of the possible system configurations are shown in Figure 14. In the slave mode, data transfer starts when the slave select (SS) pin goes active. Data is transferred into the slave's SPI Shift Register through the DI pin, which has the same address as the RxBUF Register. After a byte of data has been received by the SPI Shift Register, a Receive Character Available (RCA/IRQ3) flag and interrupt is generated. The next byte of data will be received at this time. The RxBUF Register must be cleared, or a Receive Character Overrun (RxCharOverrun) flag will be set in the SCON Register, and the data in the RxBUF Register will be overwritten. When the communication between the master and slave is complete, the SS goes inactive.

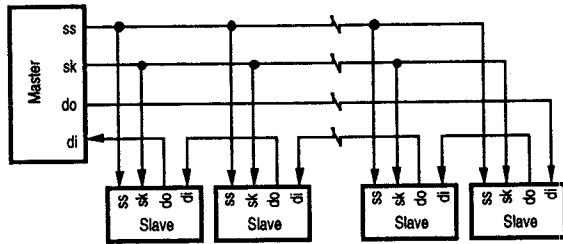
Unless disconnected, for every bit that is transferred into the slave through the DI pin, a bit is transferred out through the DO pin on the opposite clock edge. During slave operation, the SPI clock pin (SK) is an input. In master mode, the CPU must first activate a SS through one of its I/O ports. Next, data is transferred through the master's DO pin one bit per master clock cycle. Loading data into the shift register initiates the transfer. In master mode, the master's clock will drive the slave's clock. At the conclusion of a transfer, a Receive Character Available (RCA/IRQ3) flag and interrupt is generated. Before data is transferred via the DO pin, the SPI Enable bit in the SCON Register must be enabled.

SPI Compare (Z86E06 only). When the SPI Compare Enable bit, D3 of the SCON Register is set to 1, the SPI Compare feature is enabled. The compare feature is only valid for slave mode. A compare transaction begins when the (SS) line goes active. Data is received as if it were a normal transaction, but there is no data transmitted to avoid bus contention with other slave devices. When the compare byte is received, IRQ3 is not generated. Instead, the data is compared with the contents of the SCOMP Register. If the data does not match, DO remains inactive and the slave ignores all data until the (SS) signal is reset. If the data received matches the data in the SCOMP register, then a SMR signal is generated. DO is activated if it is not tri-stated by D2 in the SCON Register, and data is received the same as any other SPI slave transaction.

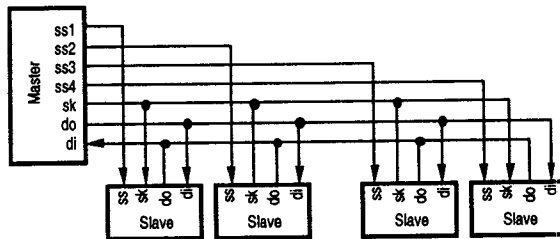
When the SPI is activated as a slave, it operates in all system modes; STOP, HALT, and RUN. Slaves' not comparing remain in their current mode, whereas slaves' comparing wake from a STOP or HALT mode by means of an SMR.

SPI Clock (Z86E06 only). The SPI clock maybe driven by three sources: Timer0, a division of the internal system clock, or the external master when in slave mode. Bit D6 of the SCON Register controls what source drives the SPI clock. A 0 in bit D6 of the SCON Register determines the division of the internal system clock if this is used as the SPI clock source. Divide by 2, 4, 8, or 16 is chosen as the scaler.

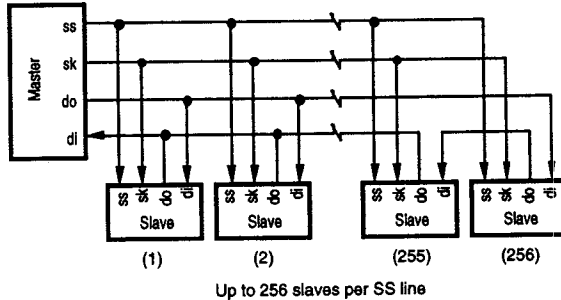
Standard Serial Setup



Standard Parallel Setup



Setup For Compare



Three Wire Compare Setup

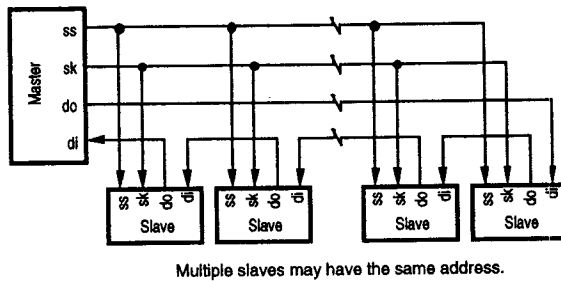


Figure 14. SPI System Configuration (Z86E06 Only)

2

FUNCTIONAL DESCRIPTION (Continued)

Receive Character Available and Overrun (Z86E06 Only). When a complete data stream is received, an interrupt is generated and the RxCharAvail bit in the SCON Register is set. Bit 4 in the SCON Register is for enabling or disabling the RxCharAvail interrupt. The RxCharAvail bit is available for interrupt polling purposes and is reset when the RxBUF Register is read. RxCharAvail is generated in both master and slave modes. While in slave mode, if the RxBUF is not read before the next data stream is received and loaded into the RxBUF Register, Receive Character Overrun (RxCharOverrun) occurs. Since there is no need

for clock control in slave mode, bit D1 in the SPI Control Register is used to log any RxCharOverrun (Figure 15 and Figure 16).

No	Parameter	Min	Units
1	DI to SK Setup	10	ns
2	SK to D0 Valid	15	ns
3	SS to SK Setup	.5 Tsk	ns
4	SS to D0 Valid	15	ns
5	SK to DI Hold Time	10	ns

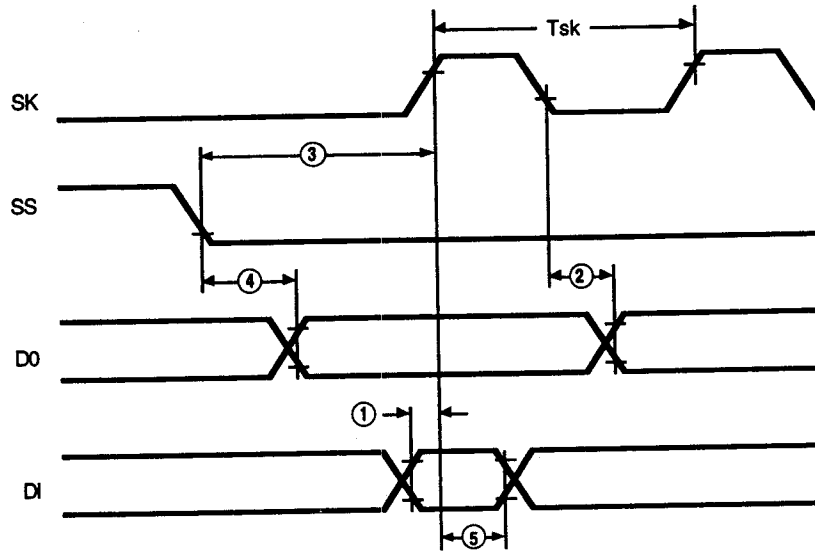


Figure 15. SPI Timing (Z86E06 Only)

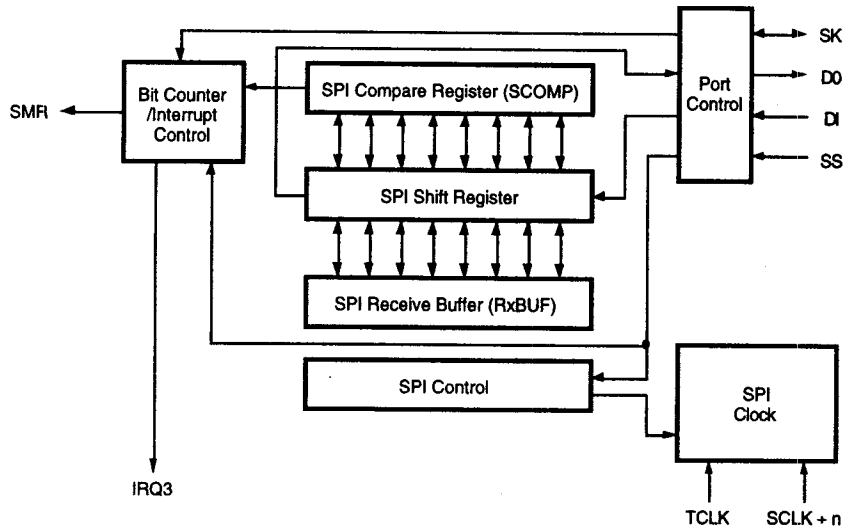


Figure 16. SPI Logic (Z86E06 Only)

PORT Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 17).

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34, and P35 and a 0 releases the Port to its standard I/O configuration.

Bits D4-D1. These bits are reserved and must be 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting D5=1. The default value is 1.

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting D6=1. The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive, it does not affect the relationship of SCLK and XTAL.

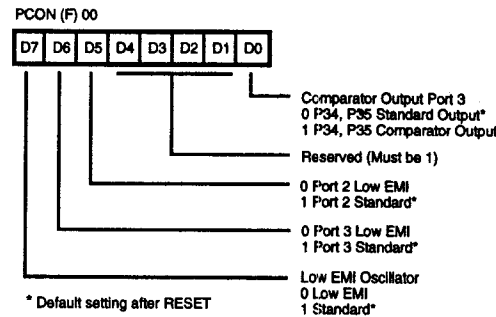


Figure 17. Port Configuration Register (PCON) (Write Only)

2

FUNCTIONAL DESCRIPTION (Continued)

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP-Mode Recovery (Figure 18). All bits are Write Only except bit 7, which is Read Only. Bit 7 is a flag bit that is hardware set on the condition of a STOP recovery and reset on a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. The recovery level must be active Low to work with SPI. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR specify the source of the STOP-Mode Recovery signal. Bit 1 determines whether the XTAL is divided by 1 or 2. A 0 in this location uses XTAL divide-by-two, and a 1 uses XTAL. The default for this bit is XTAL divide-by-two. Bit 0 controls the divide-by-16 prescaler of SCLK/TCLK. The SMR is located in bank F of the Expanded Register Group at address 0BH.

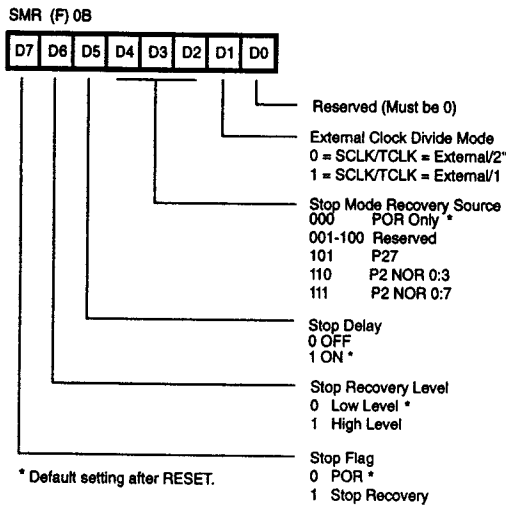


Figure 18a. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only.) (Z86E03)

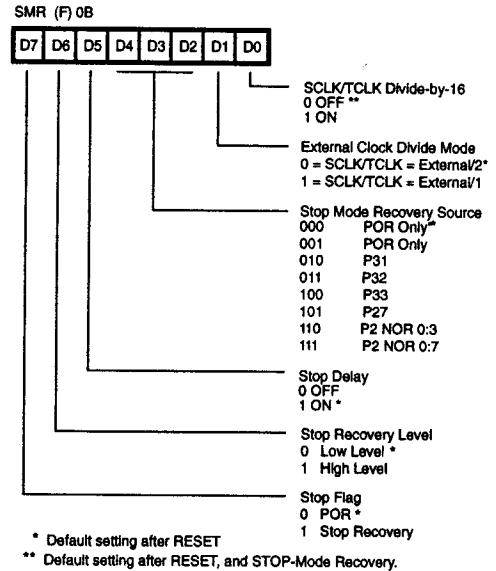


Figure 18b. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only.) (Z86E06)

SCLK/TCLK Divide-by-16 Select (D0)—Z86E06 Only. D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources the counter/timers and interrupt logic).

External Clock Divide Mode (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit, together with D7 of PCON, helps further lower EMI [i.e., D7 (PCON)=0, D1 (SMR)=1]. The default setting is 0.

STOP-Mode Recovery Source (D2,D3,D4). These three bits of the SMR specify the wake-up source of the STOP-Mode Recovery (Figure 19 and Table 5).

Table 5. STOP-Mode Recovery Source

SMR			Operation Description of Action
D4	D3	D2	
0	0	0	POR recovery only
0	0	1	POR recovery only (E03 = Reserved)
0	1	0	P31 transition (E03 = Reserved)
0	1	1	P32 transition (E03 = Reserved)
1	0	0	P33 transition (E03 = Reserved)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0:3
1	1	1	Logical NOR of Port 2 bits 0:7

P31-P33 cannot wake up from STOP Mode if the input lines are configured as analog inputs. In the Z86E06, when the SPI is enabled and the Compare feature is active, a SMR is generated upon a comparison in the SPI Shift Register and SCOMP Register, regardless of the above SMR Reg-

ister settings. If SPI Compare is used to wake up the part from STOP Mode, it is still possible to have one of the other STOP-Mode Recovery sources active. **Note:** These other STOP-Mode Recovery sources must be active level Low (bit D6 in SMR set to 0 if P31, P32, P33, and P27 selected, or bit D6 in SMR set to 1 if logical NOR of Port 2 is selected).

STOP-Mode Recovery Delay Select (D5). This bit disables the 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the "fast" wake up is selected, the STOP-Mode Recovery source needs to be kept active for at least 5 T_{PC}.

STOP-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 19).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. It is active High, and is 0 (cold) on POR/WDT RESET. This bit is Read Only. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

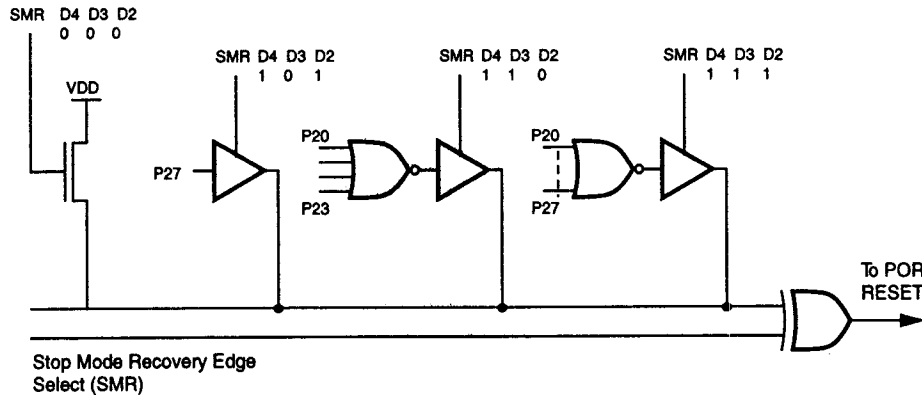
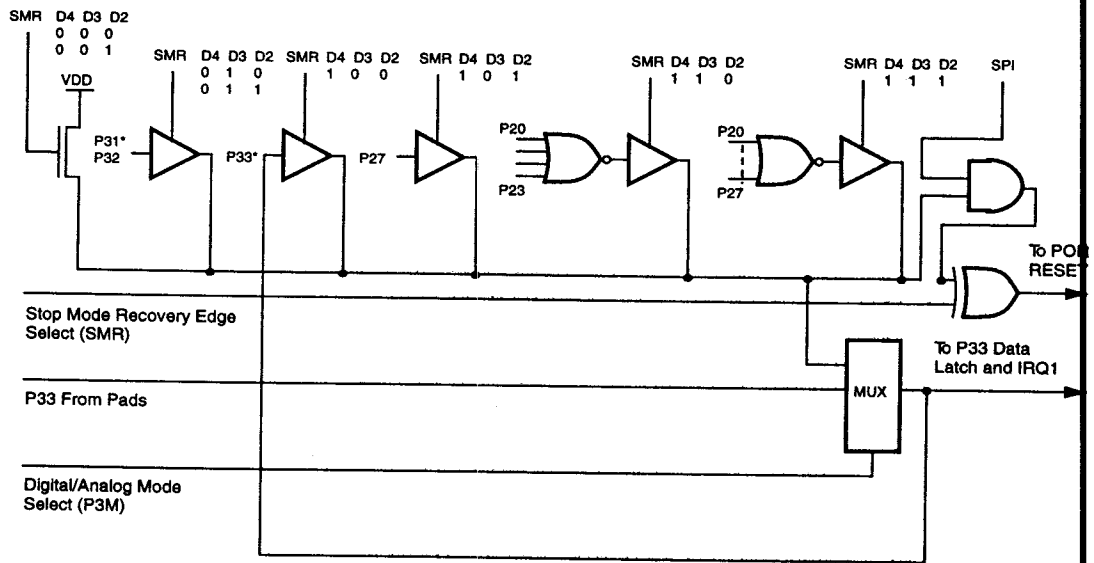


Figure 19a. STOP Mode Recovery Source (Z86E03)

2

FUNCTIONAL DESCRIPTION (Continued)



*Note: P31, P32 and P33 are not in Analog Mode.

Figure 19b. STOP-Mode Recovery Source (Z86E06)

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled after it has been initially enabled. The WDT circuit is driven by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDTMR register.

Note: Execution of the WDT instruction affects the Z (zero), S (sign), and V (overflow) flags.

Bits 0 and 1 control a tap circuit that determines the timeout period (on Z86E06 only). Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to 1, the WDT is only driven by the external clock during STOP mode. This feature makes it possible to wake up from STOP mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 20). **This register is accessible only during the first 64 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Reset or a STOP Mode Recovery (Figure 21). After this point, the regis-**

ter cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH.

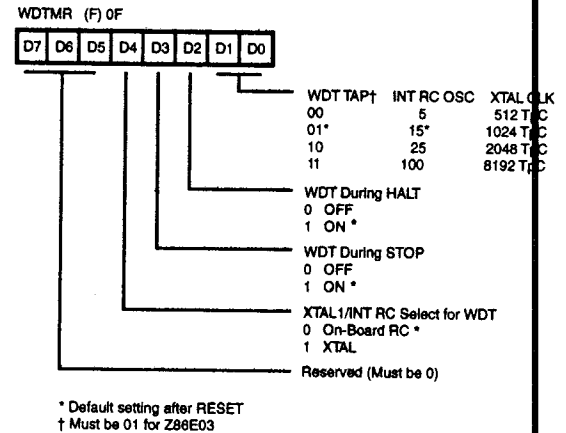
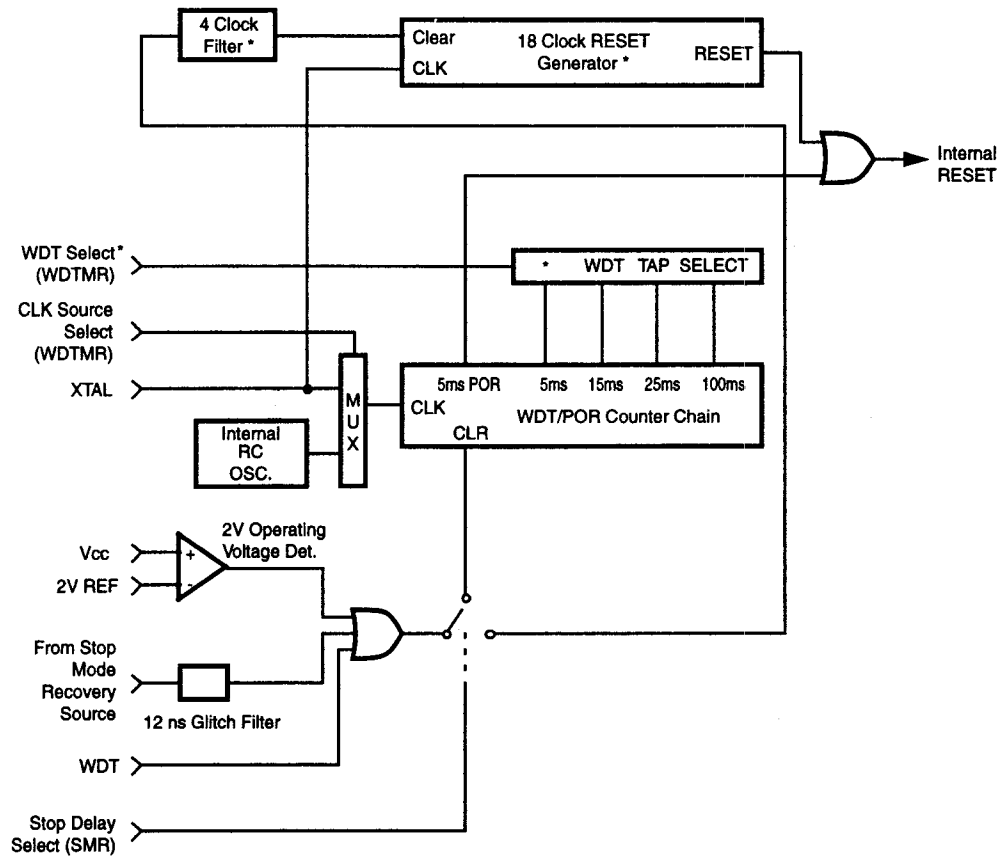


Figure 20. Watch-Dog Timer Mode Register (Write Only)



* Not available on the Z86E03, WDT fixed at 15 ms/1024T_{pC} in the Z86E03.

Figure 21. Resets and WDT

2