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CMOS Z8 16K/32K EPROM MCUs

Z86E61/Z86E63 Microcontrollers

Product Specification

PS014404-0212

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Revision History

Each instance in the following revision history table reflects a change to this document from its previous version. For more details, refer to the corresponding pages or appropriate links provided in the table.

Date	Revision Level	Description	Page
Feb 2012	04	Globally updated for style and content.	All
Oct 2008	03	Updated pin descriptions.	11
May 2008	02	Added LQFP pin diagram (Standard and Programming modes); replaced 44-pin QFP with 44-pin LQFP for CR #10886.	7, 8
Nov 2001	01	Original issue.	All

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Overview

The Z86E61/Z86E63 microcontrollers are members of the Z8® single-chip microcontroller family with 16K/32KB of EPROM and 236 bytes of general-purpose RAM. Offered in 40-pin DIP, 44-pin PLCC or 44-pin LQFP package styles, these devices are pin-compatible EPROM versions of the Z86C61/ 63. The ROMless pin option is available on the 44-pin versions only.

With 16KB/32KB of ROM and 236 bytes of general-purpose RAM, the Z86E61/Z86E63 MCU offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

For applications demanding powerful I/O capabilities, the Z86E61/Z86E63 MCU offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

The Z86E61/Z86E63 MCU can address both external memory and preprogrammed ROM, making it well suited for high-volume applications or where code flexibility is required. There are three basic address spaces available to support this configuration:

- Program memory
- Data memory
- 236 General-purpose registers

Features

The Z86E61 and Z86E63 MCUs offer the following features:

- 8-Bit CMOS microcontroller
- 40-pin DIP, 44-pin PLCC and 44-pin LQFP packages
- 4.5V to 5.5V operating range
- Clock speeds: 16MHz and 20MHz
- Low power consumption: 275 mW (max)
- Two Standby modes: STOP and HALT
- 32 Input/Output lines
- Full-duplex UART
- All digital inputs are TTL levels

- Auto Latches
- High-voltage protection on high-voltage inputs
- RAM and EPROM Protect
- EPROM:
  - 16 KB Z86E61
  - 32 KB Z86E63

- 256-byte Register File:
  - 236 bytes of General-Purpose RAM
  - 16 bytes of Control and Status registers
  - 4 bytes for ports

- Two programmable 8-bit Counter/Timers, each with 6-bit programmable prescaler
- Six vectored priority interrupts from eight different sources
- On-chip oscillator that accepts a crystal ceramic resonator, LC or external clock drive

To unburden the system from coping with real-time tasks such as counting/timing and serial data communication, the Z86E61/Z86E63 MCU offers two on-chip counter/timers with a large number of user selectable modes. See the block diagram in Figure 1.

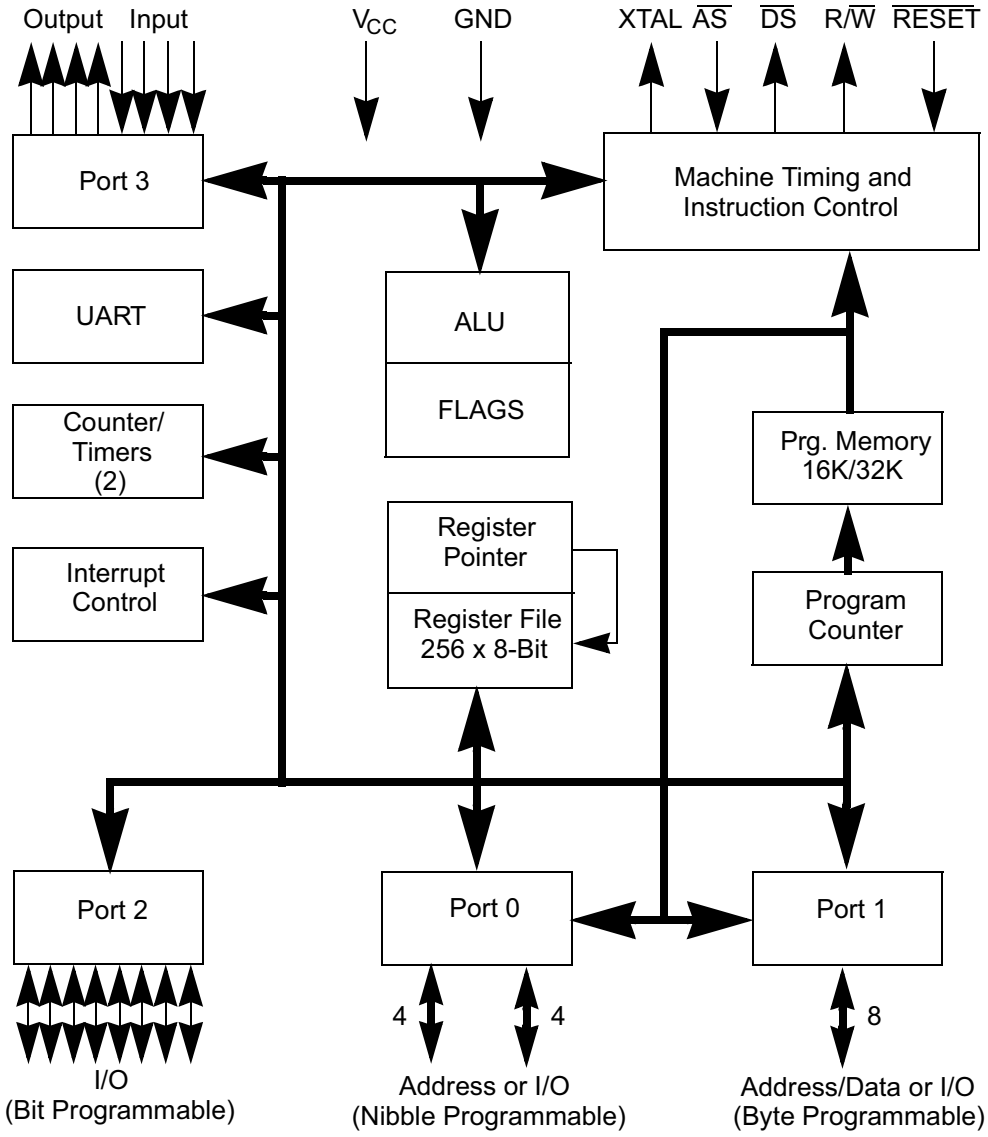

Figure 1. Z86E61/Z86E63 MCU Functional Block Diagram

Power connections follow the conventional descriptions listed in Table 24.

Table 24. Power Connection Conventions

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Pin Functions

The Z86E61/Z86E63 MCU is available in variety of package styles, programming modes and pin configurations. This section describes the pin signals and configurations for each of the 40-pin PDIP, 44-pin PLCC and 44-pin LQFP packages in both Standard and EPROM Programming modes.

Pin Signals

Figure 2 shows the pin-outs for the 40-pin PDIP Standard Mode package; Table 25 describes each pin.

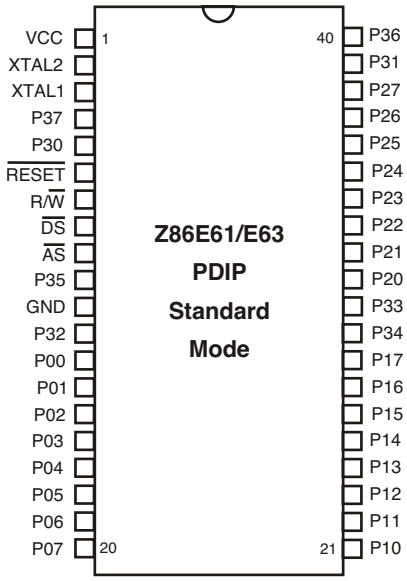

Figure 2. Z86E61/Z86E63 PDIP Pin Diagram, Standard Mode

Table 25. Z86E61/Z86E63 PDIP Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output

Table 25. Z86E61/Z86E63 PDIP Pin Description, Standard Mode (Continued)

Pin Signal	Description	I/O
$\overline{DS}$	Data Strobe	Output
$\overline{AS}$	Address Strobe	Output
P00–P07 Port 0	8-bit General I/O	Input/Output
P10–P17 Port 1	8-bit General I/O	Input/Output
P20–P27 Port 2	8-bit General I/O	Input/Output
P30–P33 Port 3	4-bit Input	Input
P34–P37 Port 3	4-bit Output	Output
R/$\overline{RL}$	ROM/ROMless Control	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 3 shows the pin-outs for the 40-pin PDIP EPROM Programming Mode package; Table 26 describes each pin.

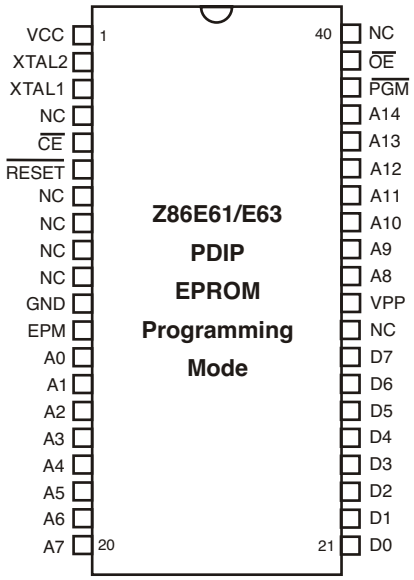

Figure 3. Z86E61/Z86E63 PDIP Pin Diagram, EPROM Programming Mode

Table 26. Z86E61/Z86E63 PDIP Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 4 shows the pin-outs for the 44-pin LQFP Standard Mode package; Table 27 describes each pin.

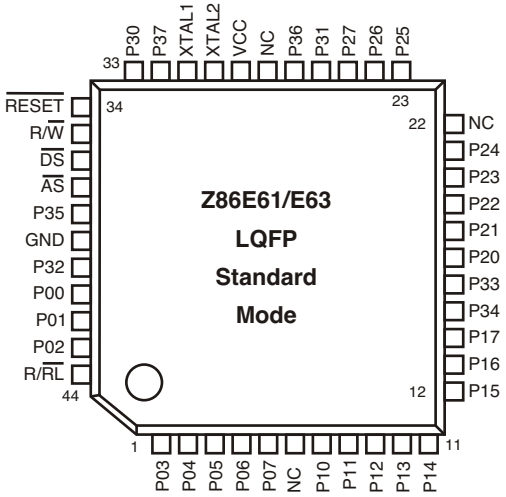

Figure 4. Z86E61/Z86E63 LQFP Pin Diagram, Standard Mode

Table 27. Z86E61/Z86E63 LQFP Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00–P07 Port 0	8-bit General I/O	Input/Output
P10–P17 Port 1	8-bit General I/O	Input/Output
P20–P27 Port 2	8-bit General I/O	Input/Output
P30–P33 Port 3	4-bit Input	Input
P34–P37 Port 3	4-bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Control	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 5 shows the pin-outs for the 44-pin LQFP EPROM Programming Mode package; Table 28 describes each pin.

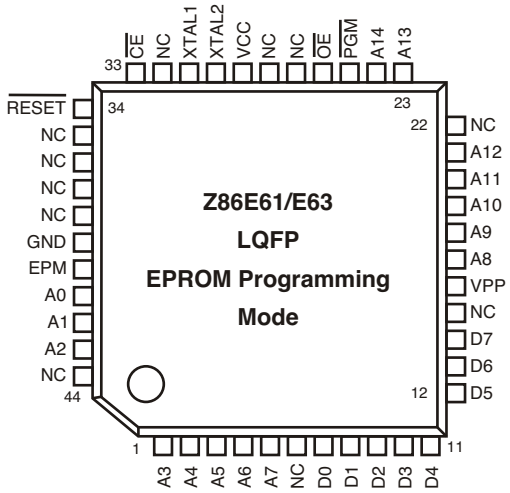

Figure 5. Z86E61/Z86E63 LQFP Pin Diagram, EPROM Programming Mode

Table 28. Z86E61/Z86E63 LQFP Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 6 shows the pin-outs for the 44-pin PLCC Standard Mode package; Table 29 describes each pin.

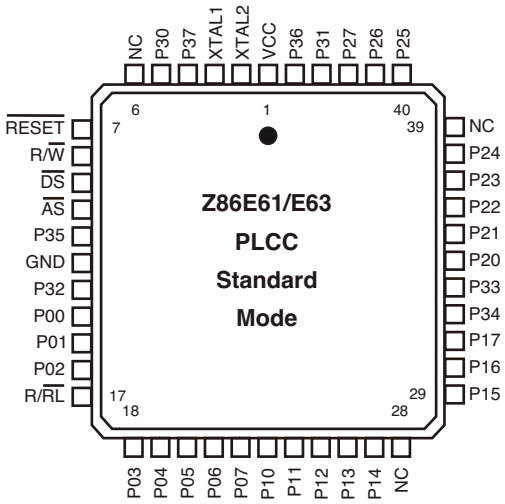

Figure 6. Z86E61/Z86E63 PLCC Pin Diagram, Standard Mode

Table 29. Z86E61/Z86E63 PLCC Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00–P07 Port 0	8-bit General I/O	Input/Output
P10–P17 Port 1	8-bit General I/O	Input/Output
P20–P27 Port 2	8-bit General I/O	Input/Output
P30–P33 Port 3	4-bit Input	Input
P34–P37 Port 3	4-bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Control	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 7 shows the pin-outs for the 44-pin PLCC EPROM Programming Mode package; Table 30 describes each pin.

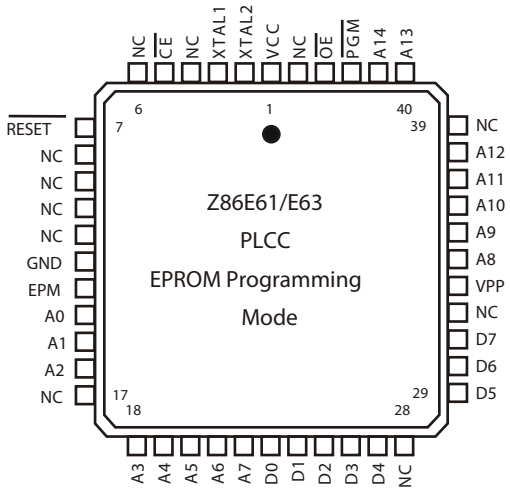

Figure 7. Z86E61/Z86E63 PLCC Pin Diagram, EPROM Programming Mode

Table 30. Z86E61/Z86E63 PLCC Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Pin Descriptions

This section describes the major Z86E61/Z86E63 MCU pin signals and ports.

ROMless (Input, Active Low)

Connecting this pin to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8 (see the Z86C91 product specification for more information). When pulled High to V_{CC}, the device functions as a normal Z86E61/Z86E63 EPROM version. This pin is only available on the 44-pin versions of the Z86E61/Z86E63 MCU.

DS (Output, Active Low)

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of DS. For WRITE operations, the falling edge of DS indicates that output data is valid.

AS (Output, Active Low)

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of AS. Under program control, AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL2, XTAL1

Crystal 2, Crystal 1 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W (Output, Write Low)

The Read/Write signal is Low when the MCU is writing to the external program or data memory.

RESET (Input, Active Low)

To avoid asynchronous and noisy reset problems, the Z86E61/Z86E63 MCU is equipped with a reset filter of four external clocks (4TpC). If the external RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external RESET, whichever is longer. During the reset cycle, DS is held active Low while AS cycles at a rate of TpC/2. When RESET is deactivated, program execution begins at location `000Ch`. Power-up reset time must be held low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P07–P00)

Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07–P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode Register.

In ROMless Mode, after a hardware reset, the Port 0 lines are defined as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode; see Figure 8.

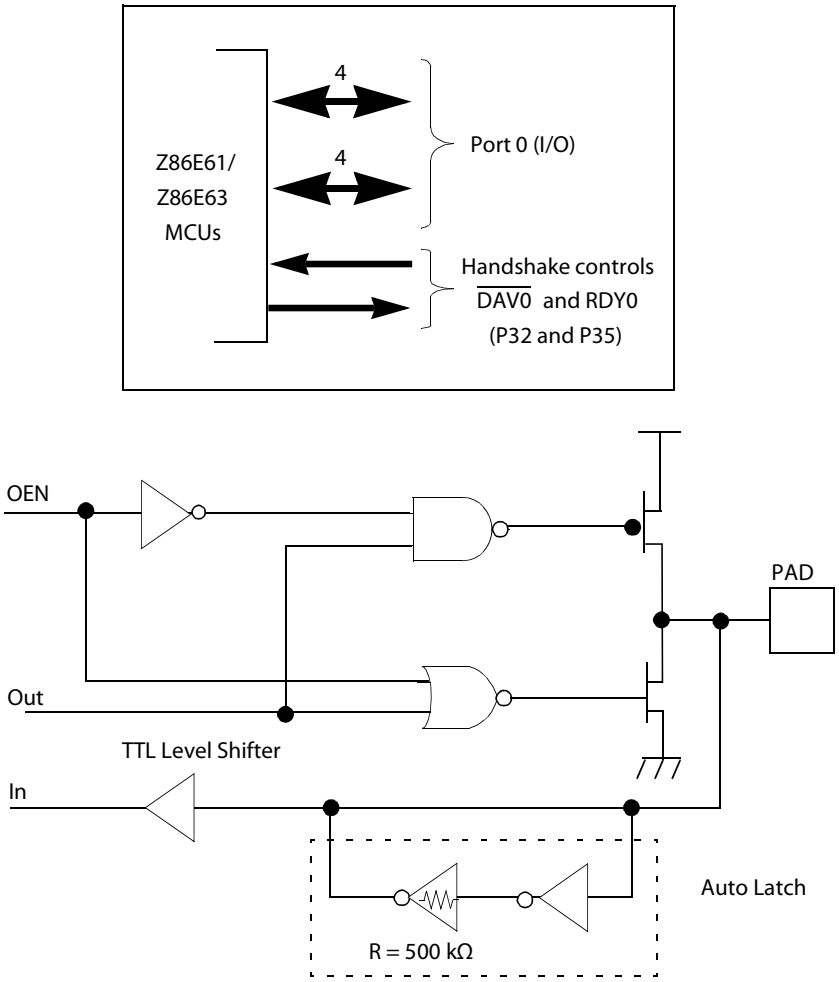

Figure 8. Port 0 Configuration

Port 1 (P17–P10)

Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7–A0) and Data (D7–D0) ports. For the Z86E61/Z86E63 MCU, these eight I/O lines can be programmed as input or output lines or are configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 lines, P33 and P34, are used as the handshake controls RDY1 and DAV1.

Memory locations greater than 16384 (Z86E61) or 32768 (Z86E63) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multi-

plexed Address/ Data Mode. If more than 256 external locations are required, Port 0 must output the additional address lines.

Port 1 can be placed in high-impedance state along with Port 0, AS, DS, and R/W, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus Request output; see Figure 9.

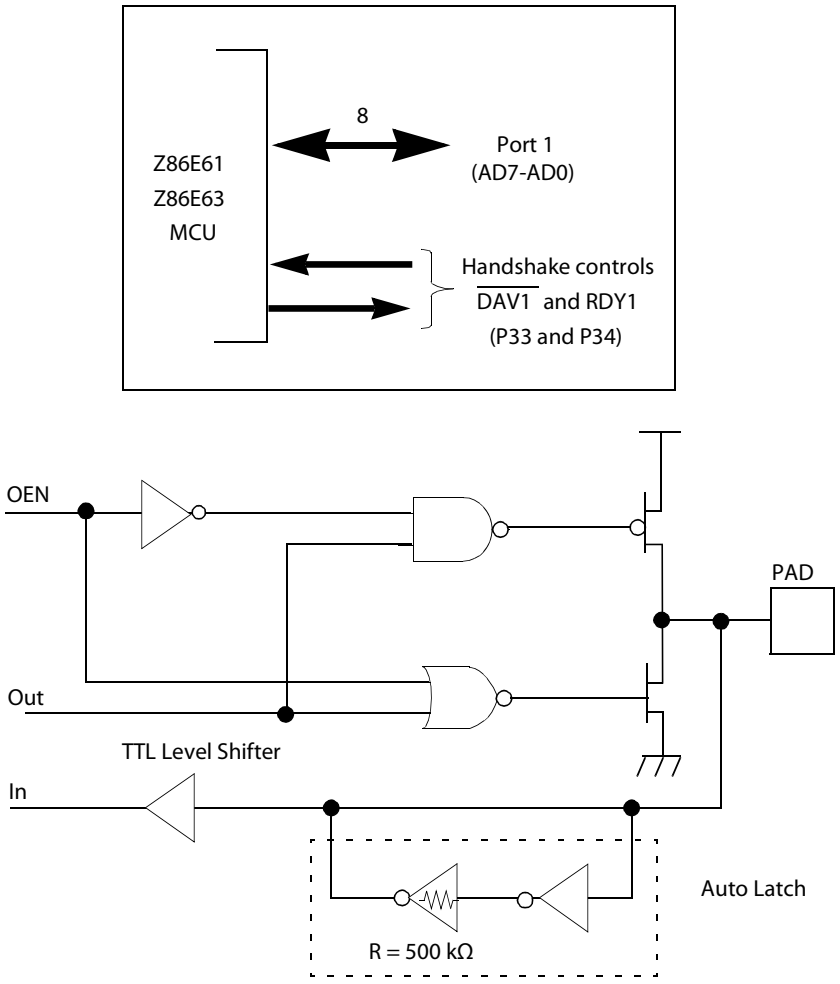

Figure 9. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bit programmable, bi-directional, CM0S compatible port. Each of these eight I/0 lines can be independently programmed as an input or output, or globally as an

open-drain output. Port 2 is always available for I/ 0 operation. When used as an I/0 port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27; see Figure 10 and Table 31 on page 16).

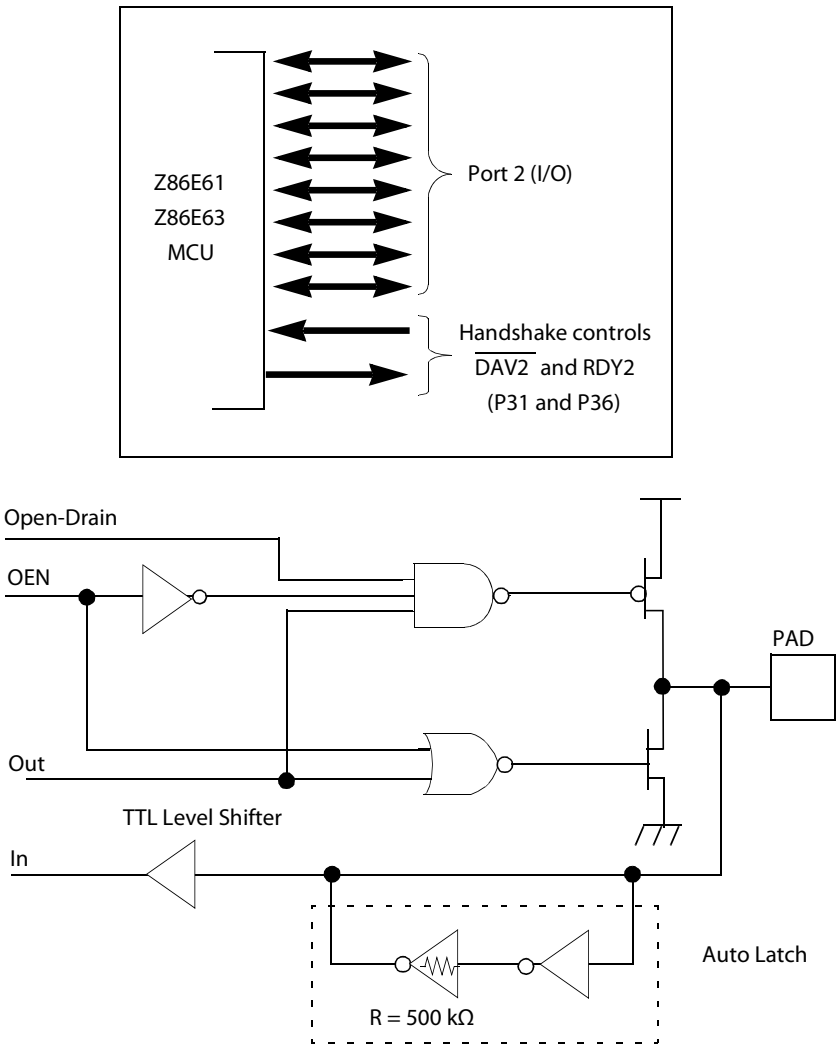

Figure 10. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33–P30) input and four-fixed (P37–P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively; see Figure 11.

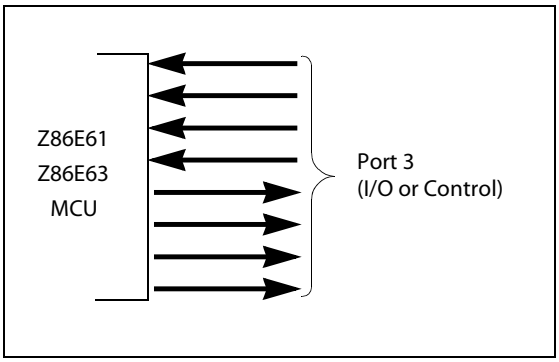

Figure 11. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (DAV and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals (T_{IN} and T_{OUT}) Data Memory Select ($\overline{DM}$) and EPROM control signals (P30 = $\overline{CE}$, P31 = $\overline{OE}$, P32 = EPM and P33 = V_{PP}).

Table 31 lists the pin assignments for Port 3.

Table 31. Port 3 Pin Assignments*

Pin	I/O	CTCI	Interrupt	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	In	T_{IN}	IRQ3				Serial In		$\overline{CE}$
P31	In	T_{IN}	IRQ2			D/R			$\overline{OE}$
P32	In	T_{IN}	IRQ0	D/R					EPM
P33	In	T_{IN}	IRQ1		D/R				V_{PP}
P34	Out	T_{OUT}			R/D			$\overline{DM}$	
P35	Out	T_{OUT}		R/D					
P36	Out	T_{OUT}				R/D			
P37	Out	T_{OUT}					Serial Out		
T0			IRQ4						
T1			IRQ5						

Note: *HS = Handshake Signals; D = Data Available; R = Ready.

UART Operation. Port 3 lines, P37 and P30, are programmed as serial I/0 lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/ Timer0.

The Z86E61/Z86E63 MCU automatically adds a start bit and two stop bits to transmitted data; see Figure 12. Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

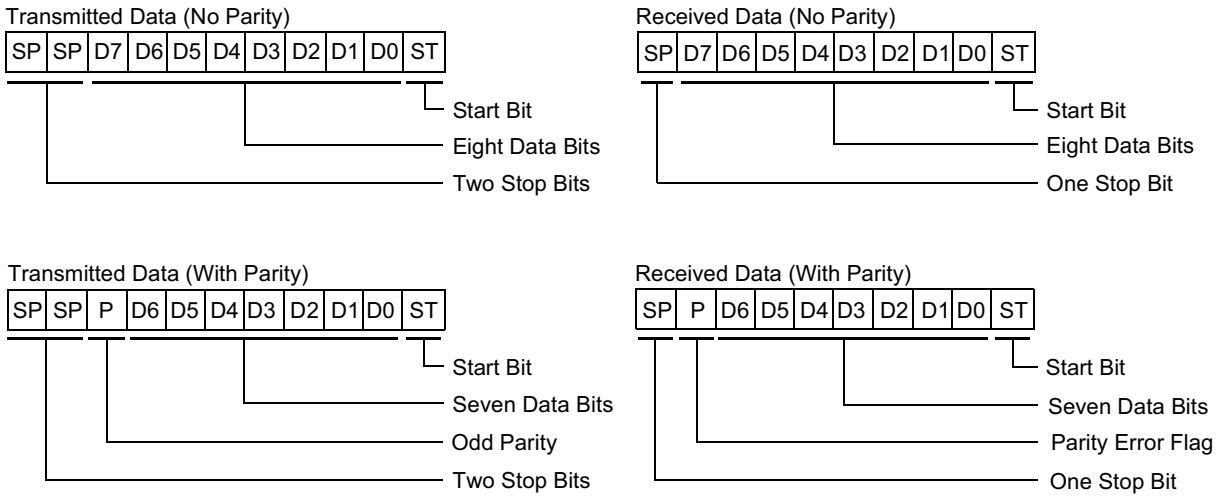

Figure 12. Serial Data Formats

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P33–P30 inputs differ from the Z86C61/C63 in that there is no clamping diode to V_{CC} because of the EPROM high voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM Mode.