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Z86E61/Z86E63

CMOS Z8 16K/32K EPROM Microcontroller

Product Specification

PS014401-1001

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- 40-Pin DIP, 44-Pin PLCC, 44-Pin LQFP Style Packages
- 4.5V to 5.5V Operating Range
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- Low Power Consumption: 275 mW (max)
- Fast Instruction Pointer: 1.0 ms 0 12 MHz
- Two Standby Modes: STOP and HALT
- 32 Input/Output Lines
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- High Voltage Protection on High Voltage Inputs
- RAM and EPROM Protect
- EPROM:
  - 16 Kbytes Z86E61
  - 32 Kbytes Z86E63
- 256 Bytes Register File
  - 236 Bytes of General-Purpose RAM
  - 16 Bytes of Control and Status Registers
  - 4 Bytes for Ports
- Two Programmable 8-Bit Counter/Timers. Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive

GENERAL DESCRIPTION

The Z86E61/E63 microcontrollers are members of the Z8® single-chip microcontroller family with 16K/32 Kbytes of EPROM and 236 bytes of general-purpose RAM. Offered in 40-pin DIP, 44-pin PLCC or 44-Pin LQFP package styles, these devices are pin-compatible EPROM versions of the Z86C61/ 63. The ROMless pin option is available on the 44-pin versions only.

With 4 Kbytes of ROM and 236 bytes of general-purpose RAM, the Z86E61/E63 offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

For applications demanding powerful I/O capabilities, the Z86E61/E63 offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

The Z86E61/E63 can address both external memory and preprogrammed ROM, making it well suited for high-volume applications or where code flexibility is required. There are three basic address spaces available to support this configuration: Program Memory, Data Memory, and 236 general-purpose registers.

To unburden the system from coping with real-time tasks such as counting/timing and serial data communication, the Z86E61/E63 offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

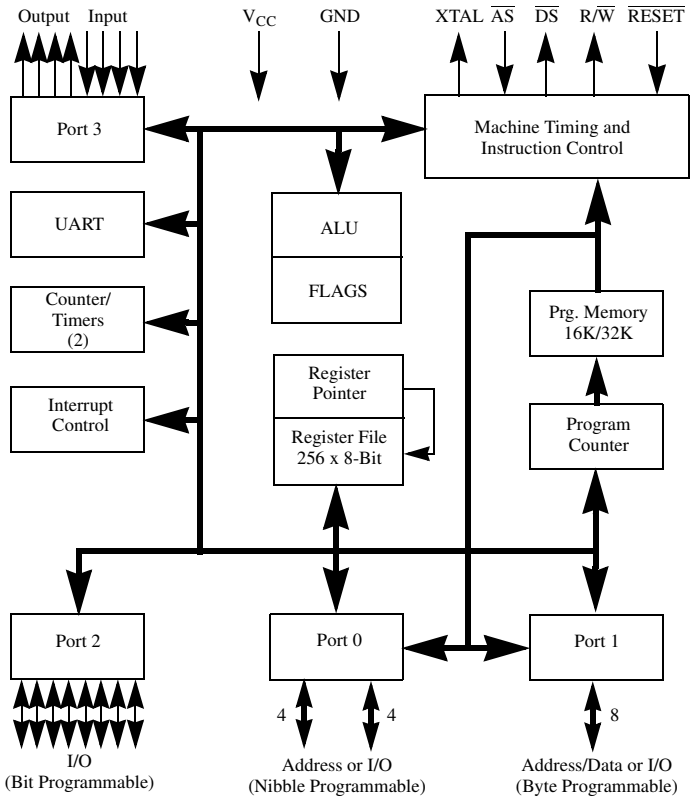
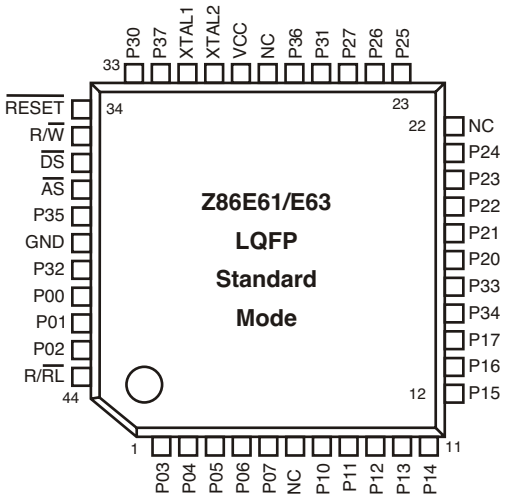
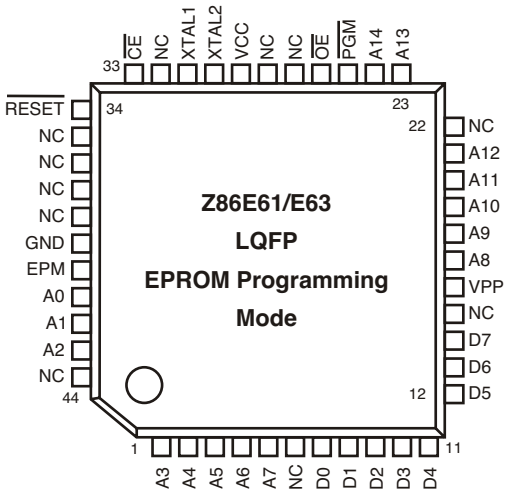


Figure 1. Z86E61/E63 Functional Block Diagram



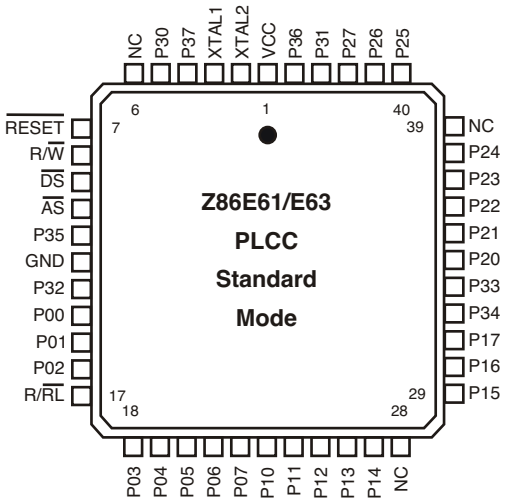
Pin Description - Standard Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00-P07 Port 0	8 bit Genaral IO	Input/Output
P10-P17 Port 1	8 bit Genaral IO	Input/Output
P20-P27 Port 2	8 bit Genaral IO	Input/Output
P30-P33 Port 3	4 bit Input	Input
P34-P37 Port 3	4 bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Ctrl	Input
GND	Ground	Input
VCC	Power Supply	Input



Pin Description - EPROM Programming Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{CE}}$	Chip Enable	Input
$\overline{\text{RESET}}$	Reset	Input
EPM	EPROM Prog Mode	Input
A0-A14	15-bit Address bus	Input
D7-D0	8-bit Data bus	Input/Output
VPP	Prog Voltage	Input
$\overline{\text{PGM}}$	Prog Mode	Input
$\overline{\text{OE}}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
VCC	Power Supply	Input



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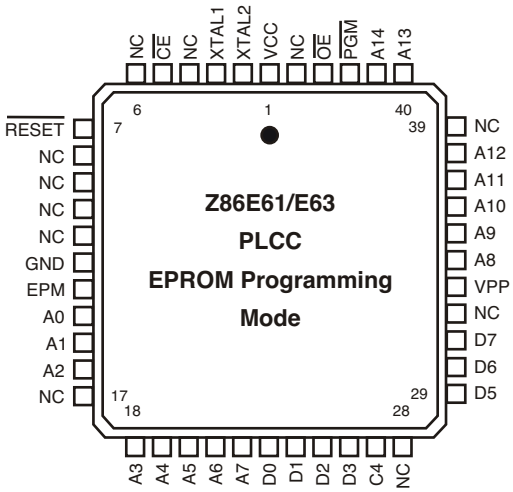
P30-P33 Port 3	4 bit Input	Input
P34-P37 Port 3	4 bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Ctrl	Input
GND	Ground	Input
VCC	Power Supply	Input



Pin Description - EPROM Programming Mode

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XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{CE}}$	Chip Enable	Input
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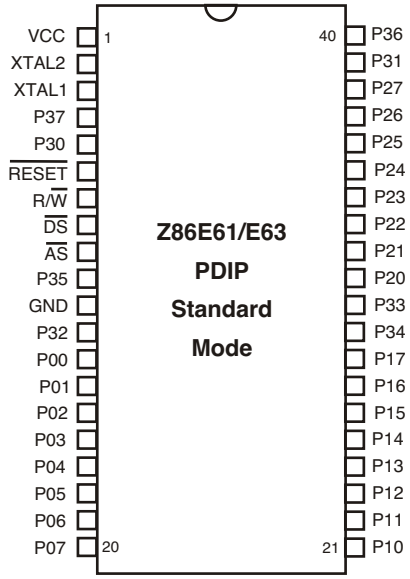

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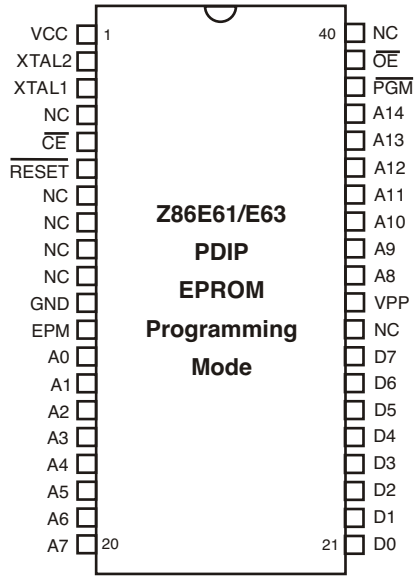
P10-P17 Port 1	8 bit Genaral IO	Input/Output
P20-P27 Port 2	8 bit Genaral IO	Input/Output
P30-P33 Port 3	4 bit Input	Input
P34-P37 Port 3	4 bit Output	Output
GND	Ground	Input
VCC	Power Supply	Input



Pin Description - EPROM Programming Mode

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VPP	Prog Voltage	Input
PGM	Prog Mode	Input
$\overline{OE}$	Output Enable	Input
$\overline{NC}$	Not Connected	Input
GND	Ground	Input
VCC	Power Supply	Input

PIN FUNCTIONS

ROMless (Input, Active Low).

Connecting this pin to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8 (see the Z86C91 product specification for more information). When pulled High to V_{CC}, the device functions as a normal Z86E61/E63 EPROM version.

Note: This pin is only available on the 44-pin versions of the Z86E61/E63.

$\overline{DS}$ (Output, Active Low).

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{DS}$. For WRITE operations, the falling edge of $\overline{DS}$ indicates that output data is valid.

$\overline{AS}$ (Output, Active Low).

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{AS}$. Under program control, $\overline{AS}$ can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL2, XTAL1

Crystal 2, Crystal 1 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/$\overline{W}$ (Output, Write Low).

The Read/Write signal is Low when the MCU is writing to the external program or data memory.

$\overline{RESET}$ (Input, Active Low).

To avoid asynchronous and noisy reset problems, the Z86E61/E63 is equipped with a reset filter of four external clocks (4TpC). If the external $\overline{RESET}$ signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external RESET, whichever is longer. During the reset cycle, DS is held active Low while AS cycles at a rate of TpC/2. When RESET is deactivated, program execution begins at location 000C (HEX). Power-up reset time must be held low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P07-P00)

Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode (Figure 8).

Port 1 (P17-P10)

Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86E61/E63, these eight I/O lines can be programmed as input or output lines or are configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 lines, P33 and P34, are used as the handshake controls RDY1 and DAV1.

Memory locations greater than 16384 (E61) or 32768 (E63) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/ Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus Request output (Figure 7).

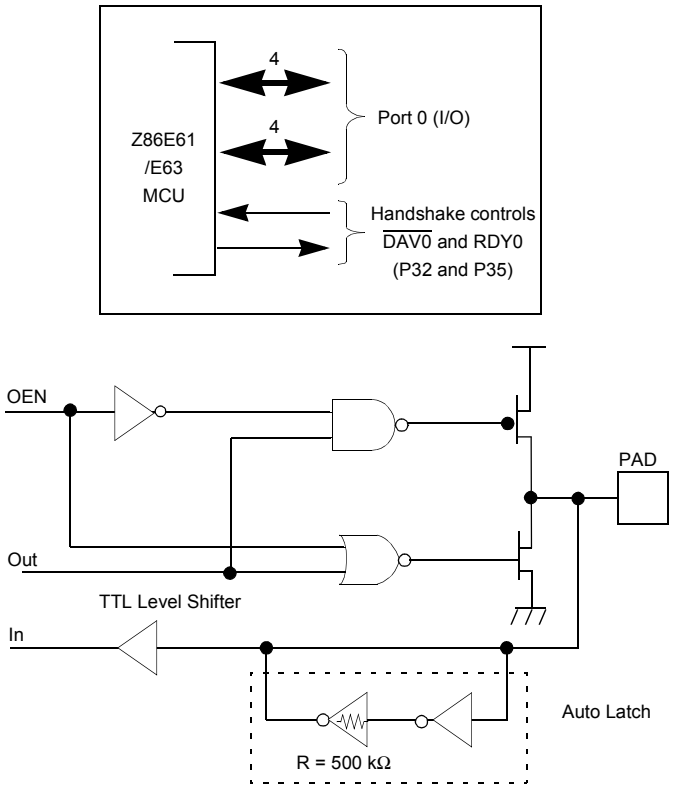

Figure 6. Port 0 Configuration

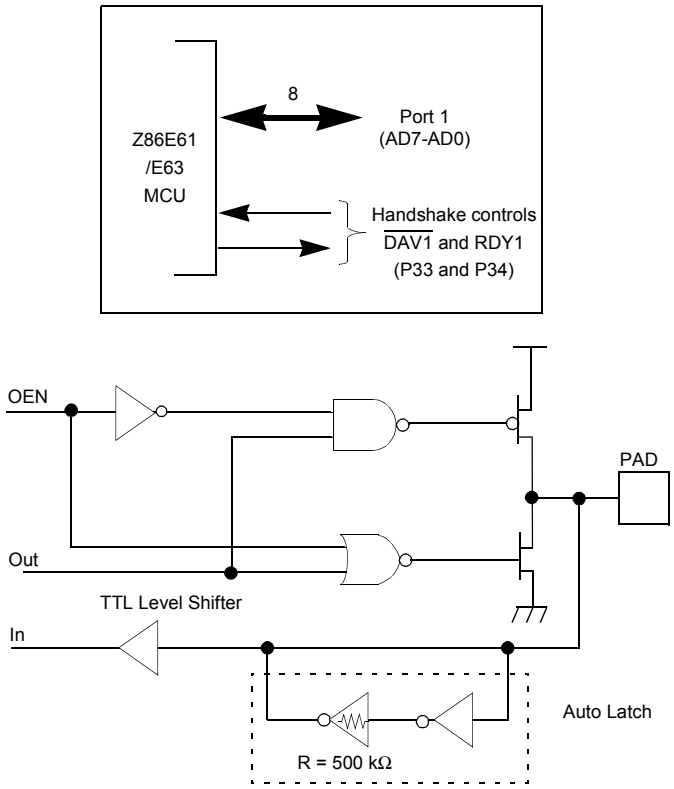

Figure 7. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CM0S compatible port. Each of these eight I/0 lines can be independently programmed as an input or output, or globally as an open-drain output. Port 2 is always available for I/0 operation. When used as an I/0 port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27 (Figure 8 and Table 21 on page 16).

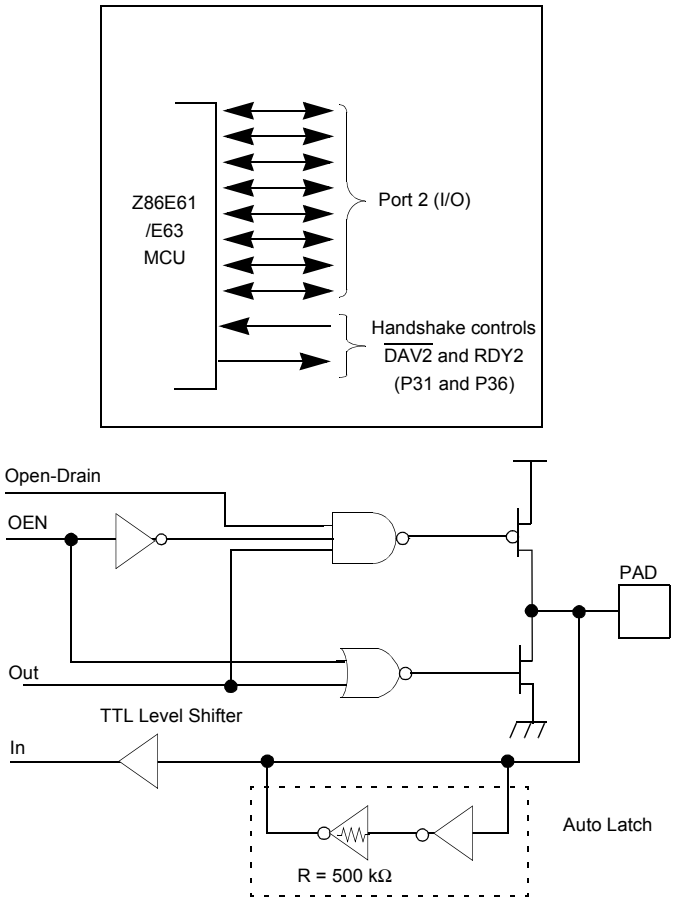

Figure 8. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively (Figure 9).

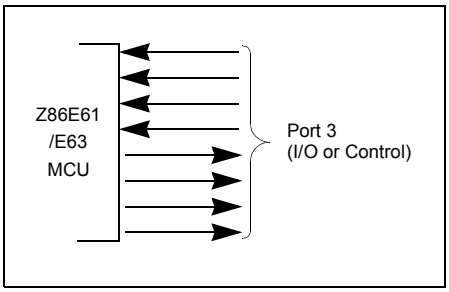

Figure 9. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (TIN and TOUT) Data Memory Select (/DM) and EPROM control signals (P30 = $\overline{CE}$, P31 = $\overline{OE}$, P32 = EPM and P33 = VPP).

Table 21. Port 3 Pin Assignments

Pin	I/O	CTCI	Int.	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	IN	T_{IN}	IRQ3				Serial In		$\overline{CE}$
P31	IN	T_{IN}	IRQ2			D/R			$\overline{OE}$
P32	IN	T_{IN}	IRQ0	D/R					EPM
P33	IN	T_{IN}	IRQ1		D/R				V_{PP}
P34	OUT	T_{OUT}			R/D			DM	
P35	OUT	T_{OUT}		R/D					
P36	OUT	T_{OUT}				R/D			
P37	OUT	T_{OUT}					Serial Out		
T0			IRQ4						
T1			IRQ5						

1. HS = Handshake Signals D = Data Available R = Ready

UART OPERATION

Port 3 lines, P37 and P30, are programmed as serial I/0 lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/ Timer0.

The Z86E61/E63 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

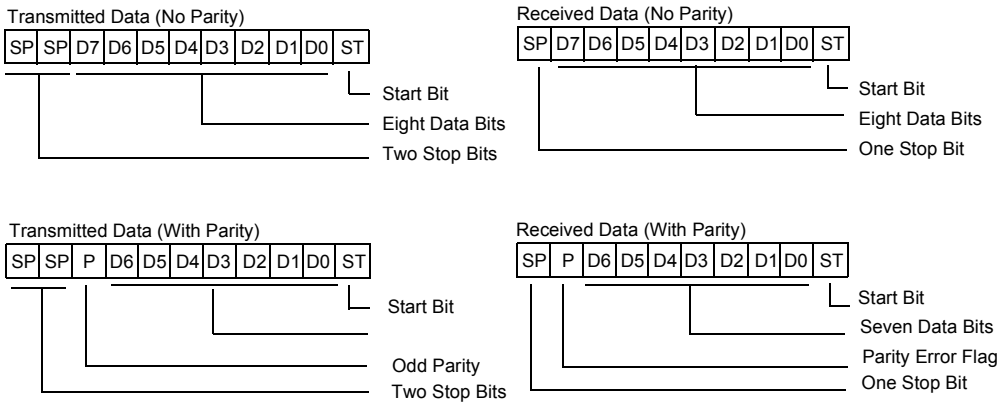

Figure 10. Serial Data Formats

Auto Latch

The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P33-P30 inputs differ from the Z86C61/C63 in that there is no clamping diode to V_{CC} because of the EPROM high voltage detection circuits. Exceeding the VIH maximum specification during standard operating mode may cause the device to enter EPROM mode.

ADDRESS SPACE

Program Memory. The Z86E61/E63 can address 48 Kbytes (E61) or 32 Kbytes (E63) of external program memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 13 to byte 16383 (E61) or 32767 (E63) consists of on-chip EPROM. At addresses 16384 (E61) or 32768 (E63) and above, the Z86E61/E63 executes external program memory fetches. In ROMless mode, the Z86E61/E63 can address up to 64 Kbytes of program memory. Program execution begins at external location 000C (HEX) after a reset.

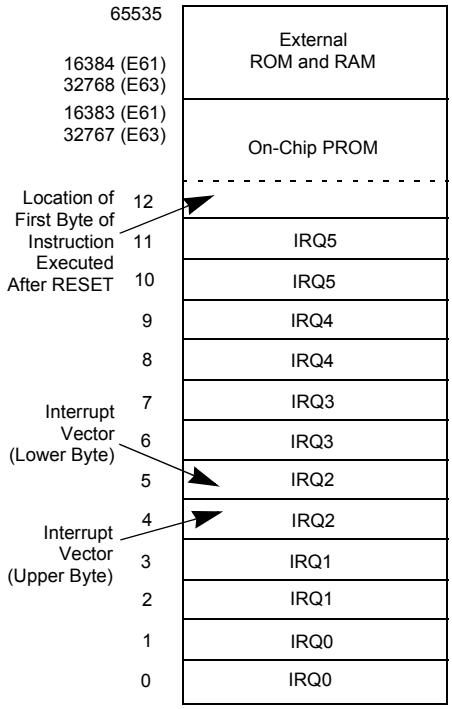

Figure 11. Program Memory Configuration

Data Memory ($\overline{DM}$)

The EPROM version can address up to 48 Kbytes (E61) or 32 Kbytes (E63) of external data memory space beginning at location 16384 (E61) or 32768 (E63). The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory

space (Figure 12). The state of the $\overline{DM}$ signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references DATA ($\overline{DM}$ active Low) memory.

Register File

The register file consists of four I/0 port registers, 236 general-purpose registers, and 16 control and status registers (Figure 13). The instructions can access registers directly or indirectly through an 8-bit address field. The Z86E61/E63 also allows short 4-bit register addressing using the Register Pointer (Figure 14). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Stack

The Z86E61/E63 has a 16-bit Stack Pointer (R255-R254) used for external stacks that reside anywhere in the data memory for the ROMless mode, but only from 16384 (E61) or 32768 (E63) to 65535 in the EPROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). The high byte of the Stack Pointer (SPH Bits 15-8) can be use as a general purpose register when using internal stack only.

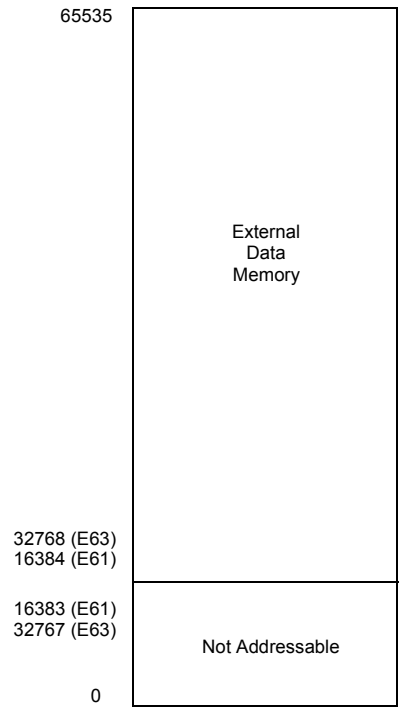

Figure 12. Data Memory Configuration

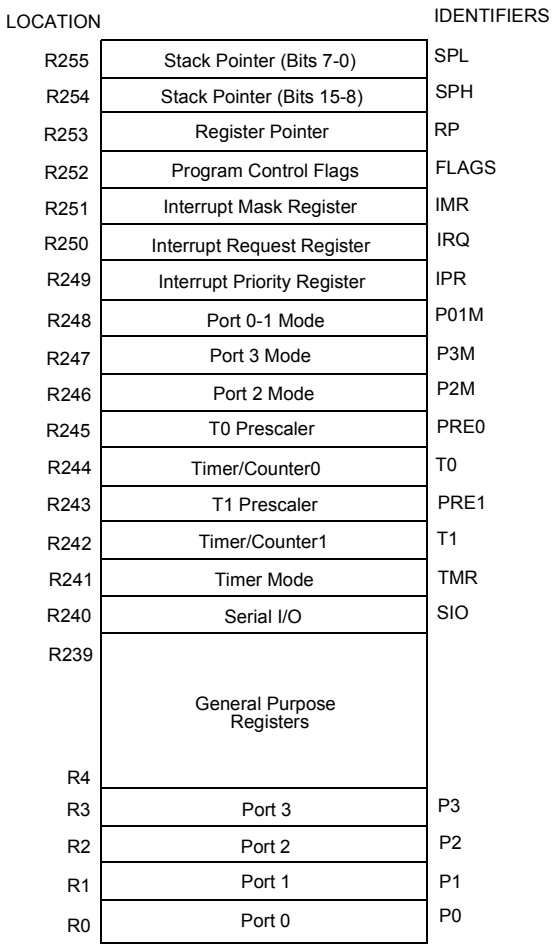

Figure 13. Register File