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Z86E72/73

OTP Microcontroller

Product Specification

PS008704-0507

www.zilog.com

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Document Disclaimer

Table of Contents

Features

Table 1 lists some of the features of the Z86E72/73 microcontrollers.

Table 1. Z86E72/73 Features

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86E73	32	236	31	3.0 V to 5.5 V
Z86E72	16	748	31	3.0 V to 5.5 V

Note: *General-purpose

- Low power consumption—60 mW (typical)
- Two standby modes (typical)
  - STOP—2 μA
  - HALT—0.8 mA
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers
  - One programmable 16-bit counter/timer with one capture register
  - Programmable input glitch filter for pulse reception
- Five priority interrupts
  - Three external
  - Two assigned to counter/timers
- Two independent comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, RC (mask option), or external clock drive
- Software-selectable 200±50% KΩ resistive transistor pull-ups on Port 0 and Port 2
  - Port 2 pull-ups are bit selectable
  - Pull-ups automatically disabled as outputs
- Software mouse/trackball interface on P00 through P03

General Description

The Z86E7X family are OTP-based members of the Z8® MCU single-chip family with 236 or 748 bytes of general-purpose RAM. The only differentiating factor between the E72/73 versions is the availability of RAM and ROM. This EPROM microcontroller family of OTP controllers also offers the use of external memory, which enables this Z8 microcontroller to be used where code flexibility is required. ZiLOG's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with cost-effective and low power consumption.

The Z86E7X architecture is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

Z8 applications demand powerful I/O capabilities. The Z86E7X family fulfills this with three package options in which the E72/73 versions provide 31 pins of dedicated input and output. These lines are grouped into four ports. Each port consists of eight lines (Port 3 has seven lines of I/O and one Pref comparator input) and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are five basic address spaces available to support a wide range of configurations: program memory, register file, Expanded Register File, Extended Data RAM, and external memory. The register file is composed of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and the rest are general-purpose registers. The Extended Data RAM adds 512 (E72) of usable general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86E7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (Figure 19 on page 34).

Note: All signals with a preceding front slash, “/”, are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

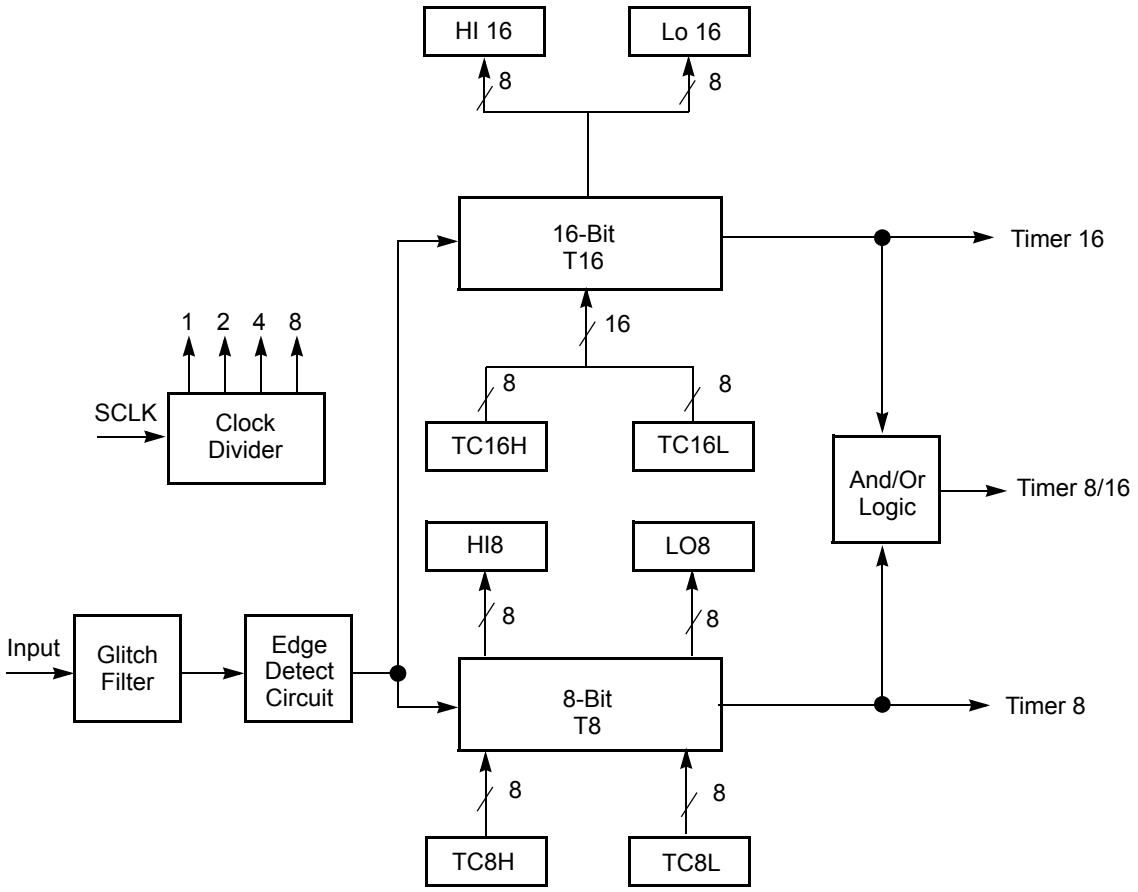

Figure 1. Z86E7X Counter/Timer Block Diagram

Power connections follow the conventions listed in Table 2.

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Figure 2 displays the functional block diagram.

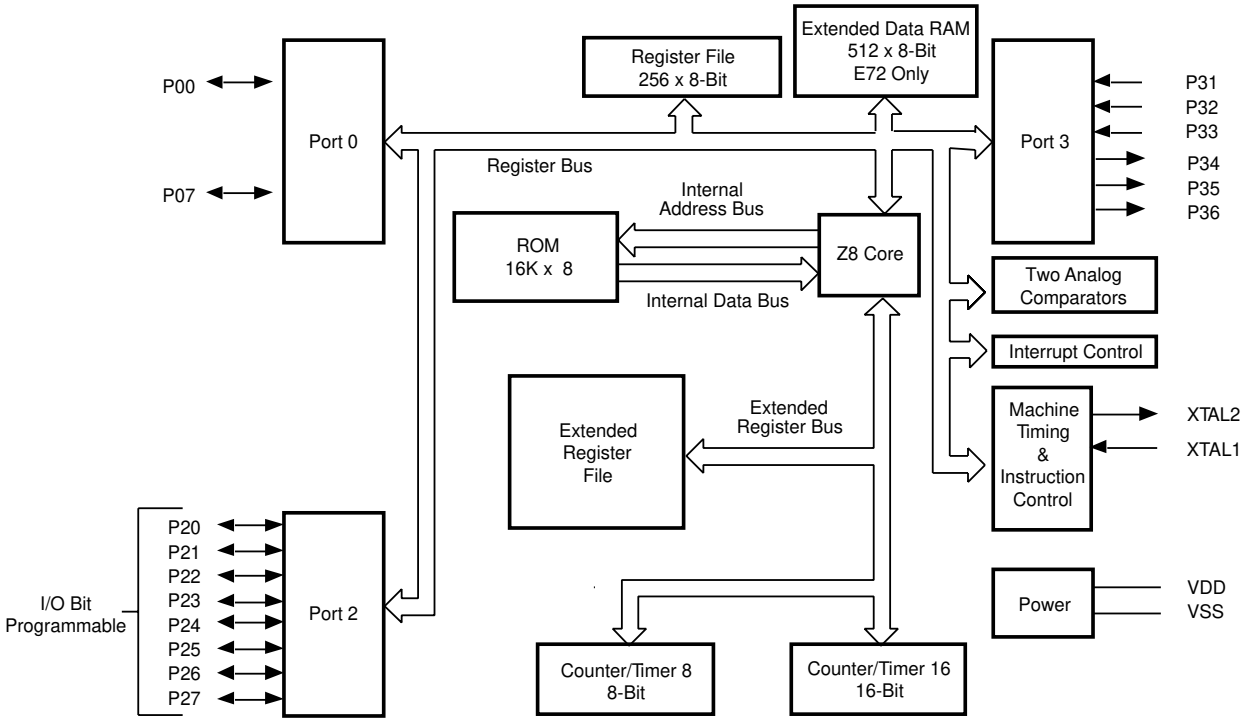

Figure 2. Z86E7X Functional Block Diagram

Pin Description

Figure 3 shows the pin assignments for the standard mode of the 40-pin dual in-line package (DIP). Figure 4 on page 6 shows the pin assignments for the electronically programmable read-only memory (EPROM) mode of the 40-pin DIP.

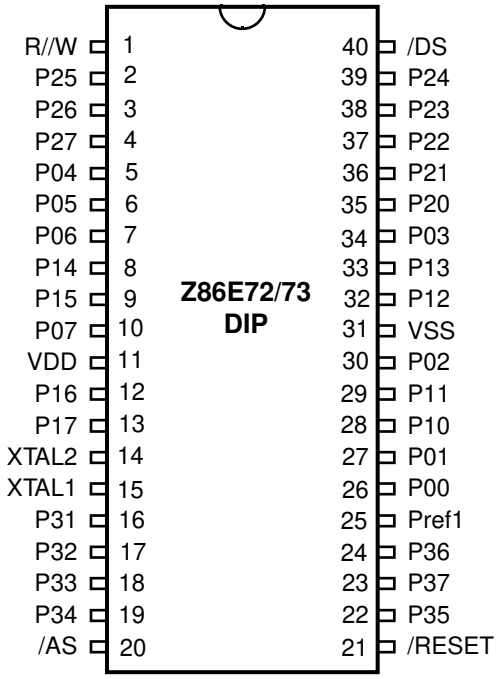

Figure 3. 40-Pin DIP Pin Assignments (Standard Mode)

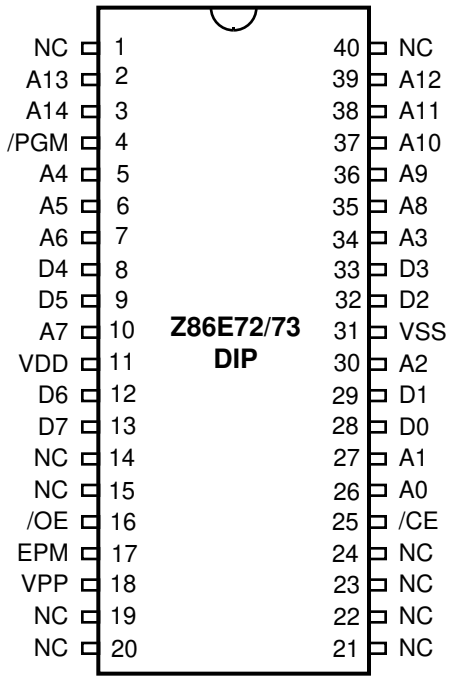

Figure 4. 40-Pin DIP Pin Assignments (EPROM Mode)

Figure 5 on page 7 shows the pin assignments for the standard mode of the 44-pin plastic leaded chip carrier (PLCC). Figure 6 on page 7 displays the pin assignments for the EPROM mode of the 44-pin PLCC.

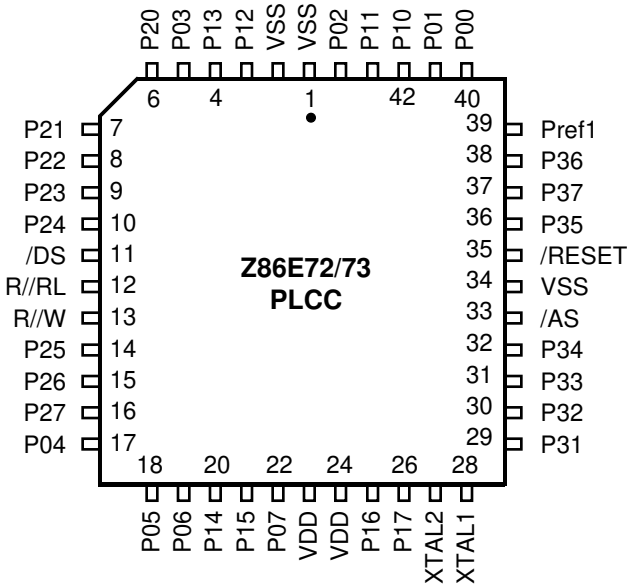

Figure 5. 44-Pin PLCC Pin Assignments (Standard Mode)

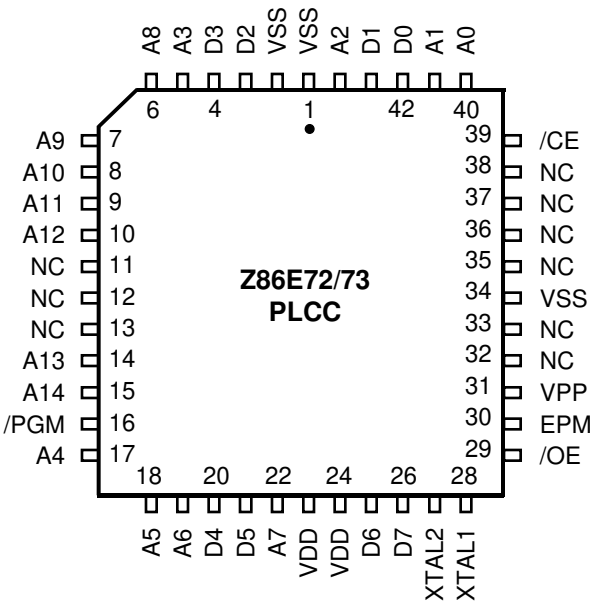

Figure 6. 44-Pin PLCC Pin Assignments (EPROM Mode)

Figure 7 displays the pin assignments for the standard mode of the 44-pin low-profile quad flat pack (LQFP). Figure 8 on page 9 shows the pin assignments for the EPROM mode of the 44-pin LQFP.

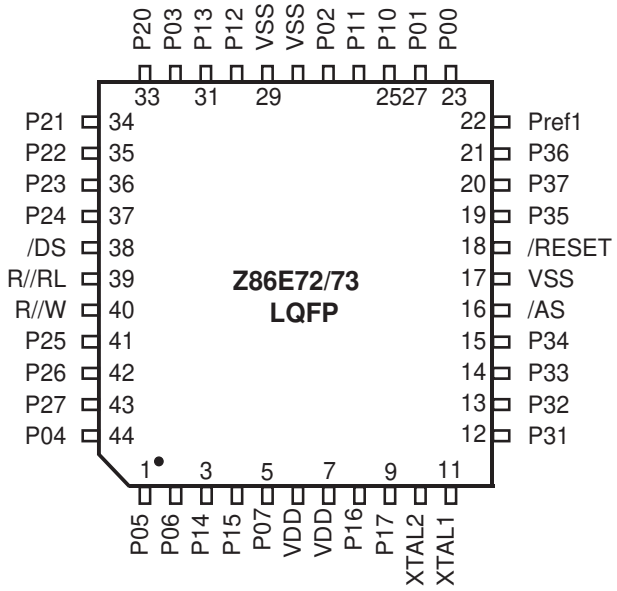

Figure 7. 44-Pin LQFP Pin Assignments (Standard Mode)

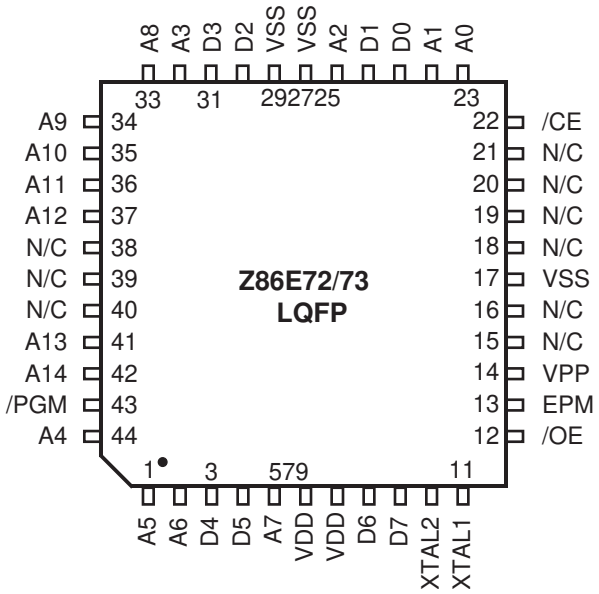

Figure 8. 44-Pin LQFP Pin Assignments (EPROM Mode)

Table 3 identifies the pins in packages in standard mode. Table 4 on page 11 identifies the pins in the 40-pin DIP in EPROM mode. Table 5 on page 12 identifies the pins in the 44-pin LQFP and PLCC.

Table 3. Pin Identification (Standard Mode)

40-Pin DIP #	44-Pin PLCC #	44-Pin LQFP #	Symbol	Direction	Description
26	40	23	P00	Input/Output	Port 0 is Nibble Programmable.
27	41	24	P01	Input/Output	Port 0 can be configured as A15–A8 external program
30	44	27	P02	Input/Output	
34	5	32	P03	Input/Output	ROM Address Bus.
5	17	44	P04	Input/Output	Port 0 can be configured as a
6	18	1	P05	Input/Output	mouse/trackball input.
7	19	2	P06	Input/Output	
10	22	5	P07	Input/Output	
28	42	25	P10	Input/Output	Port 1 is byte programmable.

Table 3. Pin Identification (Standard Mode) (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin LQFP #	Symbol	Direction	Description
29	43	26	P11	Input/Output	Port 1 can be configured as multiplexed A7–A0/D7–D0 external program ROM Address/Data Bus
32	3	30	P12	Input/Output	
33	4	31	P13	Input/Output	
8	20	3	P14	Input/Output	.
9	21	4	P15	Input/Output	
12	25	8	P16	Input/Output	
13	26	9	P17	Input/Output	
35	6	33	P20	Input/Output	Port 2 pins are individually configurable as input or output
36	7	34	P21	Input/Output	
37	8	35	P22	Input/Output	
38	9	36	P23	Input/Output	
39	10	37	P24	Input/Output	
2	14	41	P25	Input/Output	
3	15	42	P26	Input/Output	
4	16	43	P27	Input/Output	
16	29	12	P31	Input	IRQ2/Modulator input
17	30	13	P32	Input	IRQ0
18	31	14	P33	Input	IRQ1
19	32	15	P34	Output	T8 output
22	36	19	P35	Output	T16 output
24	38	21	P36	Output	T8/T16 output
23	37	20	P37	Output	
20	33	16	/AS	Output	Address Strobe
40	11	38	/DS	Output	Data Strobe
1	13	40	R//W	Output	Read/Write
21	35	18	/RESET	Input	Reset
15	28	11	XTAL1	Input	Crystal, Oscillator Clock

Table 3. Pin Identification (Standard Mode) (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin LQFP #	Symbol	Direction	Description
14	27	10	XTAL2	Output	Crystal, Oscillator Clock
11	23, 24	6, 7	V_{DD}		Power Supply
31	1, 2, 34	17, 28, 29	V_{SS}		Ground
25	39	22	Pref1	Input	Comparator 1 Reference
NC	12	39	R//RL	Input	ROM//ROMless

Table 4. Z86E72/73 40-Pin DIP Identification—EPROM Mode

40-Pin #	Symbol	Function	Direction
1	N/C	Not Connected	
2–3	A13–14	Address 13, 14	Input
4	/PGM	Program Mode	Input
5–7	A4–A6	Address 4, 5, 6	Input
8–9	D4–D5	Data 4, 5	Input/Output
10	A7	Address 7	Input
11	V_{DD}	Power Supply	
12–13	D6–D7	Data 6, 7	Input/Output
14–15	N/C	Not Connected	
16	/OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19–24	N/C	Not Connected	
25	/CE	Chip Enable	Input
26–27	A0–A1	Address 0, 1	Input
28–29	D0–D1	Data 0, 1	Input/Output
30	A2	Address 2	Input
31	V_{SS}	Ground	
32–33	D2–D3	Data 2, 3	Input/Output

Table 4. Z86E72/73 40-Pin DIP Identification—EPROM Mode (Continued)

40-Pin #	Symbol	Function	Direction
34	A3	Address 3	Input
35–39	A8–A12	Address 8, 9, 10, 11, 12	Input
40	N/C	Not Connected	

Table 5. Z86E72/73 44-Pin LQFP/PLCC Pin Identification—EPROM Mode

44-Pin LQFP	44-Pin PLCC	Symbol	Function	Direction
1–2	18–19	A5–A6	Address 5, 6	Input
3–4	20–21	D4–D5	Data 4, 5	Input/Output
5	22	A7	Address 7	Input
6–7	23–24	V_{DD}	Power Supply	
8–9	25–26	D6–D7	Data 6, 7	Input/Output
10	27	XTAL2	Crystal Oscillator Clock	
11	28	XTAL1	Crystal Oscillator Clock	
12	29	/OE	Output Enable	Input
13	30	EPM	EPROM Prog. Mode	Input
14	31	V_{PP}	Prog. Voltage	Input
15–16	32–33	N/C	Not Connected	
17	34	V_{SS}	Ground	
18–21	35–38	N/C	Not Connected	
22	39	/CE	Chip Select	Input
23–24	40–41	A0–A1	Address 0, 1	Input
25–26	42–43	D0–D1	Data 0, 1	Input/Output
27	44	A2	Address 2	Input
28–29	1–2	V_{SS}	Ground	
30–31	3–4	D2–D3	Data 2, 3	Input/Output
32	5	A3	Address 3	Input
33–37	6–10	A8–A12	Address 8, 9, 10, 11, 12	Input
38–40	11–13	N/C	Not Connected	

Table 5. Z86E72/73 44-Pin LQFP/PLCC Pin Identification—EPROM Mode

44-Pin LQFP	44-Pin PLCC	Symbol	Function	Direction
41–42	14–15	A13–A14	Address 13, 14	Input
43	16	/PGM	Prog. Mode	Input
44	17	A4	Address 4	Input

Absolute Maximum Ratings

Table 6 lists the absolute maximum ratings for the Z86E72/73 microcontrollers.

Table 6. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{MAX}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65°	+150°	C
T_A	Oper. Ambient Temperature		†	C

Notes:
* Voltage on all pins with respect to GND.
† See “Ordering Information” on page 97.

Stresses greater than those listed under Absolute Maximum Ratings might cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 9).

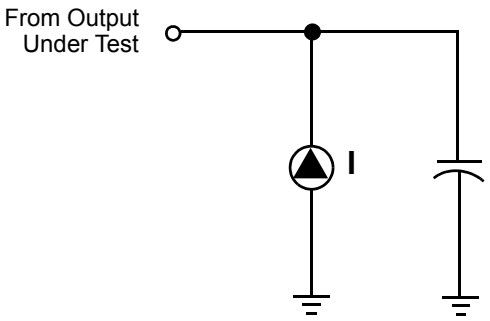

Figure 9. Test Load Diagram

Capacitance

Table 7 lists the capacitances for the Z86E72/73 microcontrollers.

Table 7. Capacitance

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

Note: T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND.

DC Characteristics

Table 8 lists the direct current (DC) characteristics.

Table 8. DC Characteristics

			T_A = 0 °C to +70 °C		Typical		
Sym.	**Parameter**	**V_{CC}**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**
	Max Input Voltage	3.0 V 5.5 V		7 7		V V	I_{IN} 250 µA I_{IN} 250 µA
V_{CH}	Clock Input High Voltage	3.0 V 5.5 V	0.9 V_{CC} 0.9 V_{CC}	V_{CC} + 0.3 V_{CC} + 0.3		V V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	3.0 V 5.5 V	V_{SS} –0.3 V_{SS} –0.3	0.2 V_{CC} 0.2 V_{CC}		V V	Driven by External Clock Generator
V_{IH}	Input High Voltage	3.0 V 5.5 V	0.7 V_{CC} 0.7 V_{CC}	V_{CC} + 0.3 V_{CC} + 0.3	0.5 V_{CC} 0.5 V_{CC}	V V	
V_{IL}	Input Low Voltage	3.0 V 5.5 V	V_{SS} –0.3 V_{SS} –0.3	0.2 V_{CC} 0.2 V_{CC}	0.5 V_{CC} 0.5 V_{CC}	V V	
V_{OH1}	Output High Voltage	3.0 V 5.5 V	V_{CC} –0.4 V_{CC} –0.4		2.9 5.4	V V	I_{OH} = –0.5 mA I_{OH} = –0.5 mA
V_{OH2}	Output High Voltage (P00, P01, P36, P37)	3.0 V 5.5 V	V_{CC} 0.7 V_{CC} 0.7			V V	I_{OH} = –7 mA I_{OH} = –7 mA
V_{OL1}	Output Low Voltage	3.0 V 5.5V		0.4 0.4	0.1 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 4.0 mA
V_{OL2*}	Output Low Voltage	3.0 V 5.5 V		0.8 0.8	0.5 0.3	V V	I_{OL} = 5.0 mA I_{OL} = 7.0 mA
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	3.0 V 5.5 V		0.8 0.8	0.3 0.2	V V	I_{OL} = 10 mA I_{OL} = 10 mA
V_{RH}	Reset Input High Voltage	3.0 V 5.5 V	0.8 V_{CC} 0.8 V_{CC}	V_{CC} V_{CC}	1.5 2.5	V V	
V_{RI}	Reset Input Low Voltage	3.0 V 5.5 V	V_{SS} –0.3 V_{SS} –0.3	0.2 V_{CC} 0.2 V_{CC}	0.9 1.8		
V_{OFFSET}	Comparator Input Offset Voltage	3.0 V 5.5 V		25 25	10 10	mV mV	
I_{IL}	Input Leakage	3.0 V 5.5 V	–1 –1	1 1	< 1 < 1	µA µA	V_{IN} = 0 V, V_{CC} V_{IN} = 0 V, V_{CC}
I_{OL}	Output Leakage	3.0 V 5.5 V	–1 –1	1 1	< 1 < 1	µA µA	V_{IN} = 0 V, V_{CC} V_{IN} = 0 V, V_{CC}

Table 8. DC Characteristics (Continued)

			T_A = 0 °C to +70 °C		Typical		
Sym.	**Parameter**	**V_{CC}**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**
I_{IR}	Reset Input Current	3.0 V		–230	–50	µA	
		5.5 V		–400	–80	µA	
I_{CC}	Supply Current (WDT off)	3.0 V		10	4	mA	@ 8.0 MHz
		5.5 V		15	10	mA	@ 8.0 MHz
I_{CC1}	Standby Current (WDT Off)	3.0 V		3	1	mA	HALT Mode V_{IN} = 0 V, V_{CC} at 8.0 MHz, Notes 1, 2
		5.5 V		5	4	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 8.0 MHz, Notes 1, 2
		3.0 V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz Notes 1, 2
		5.5 V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz Notes 1, 2
I_{CC2}	Standby Current	3.0 V		8	2	µA	STOP Mode V_{IN} = 0 V, V_{CC} WDT is not Running Notes 3, 5, 9
		5.5 V		10	3	µA	STOP Mode V_{IN} = 0 V, V_{CC} WDT is not Running Notes 3, 5, 9
		3.0 V		500	310	µA	STOP Mode Notes 3, 5
		5.5 V		800	600	µA	V_{IN} = 0 V, V_{CC} WDT is Running
V_{ICR}	Input Common Mode Voltage Range	3.0 V	0	V_{CC}–1.0 V	V		Note 8
		5.5 V	0	V_{CC}–1.0 V	V		
V_{LV}	VCC Low-Voltage Detection			2.9 V	2.55 V		Note 6
T_{POR}	Power-On Reset	3.0 V	12	75	18	ms	
		5.5 V	5	20	7	ms	

Table 8. DC Characteristics (Continued)

Sym.	Parameter	V_{CC}	T_A = 0 °C to +70 °C Min	Max	Typical @ 25°C	Units	Conditions
V_{RAM}	Static RAM Data Retention Voltage	Vram			0.5	V	Worst case 0.8 V guaranteed by design only Note 6

Notes:	ICC1	Typ	Max	Unit	Frequency
	Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
	External Clock Drive	0.3 mA	5	mA	8.0 MHz

1. All outputs unloaded, inputs at rail
2. CL1 = CL2 = 100 pF
3. Same as note [4] except inputs at V_{CC}
4. The V_{LV} increases as the temperature decreases.
5. Oscillator stopped
6. Oscillator does not stop when V_{CC} falls below V_{LV} threshold.
7. 32 kHz clock driver input
8. For analog comparator, inputs when analog comparators are enabled
9. WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.

* All outputs excluding P00, P01, P36, and P37

AC Characteristics

Figure 10 shows the external input/output (I/O) or memory read and write timing. Table 9 describes the I/O or memory read and write timing.

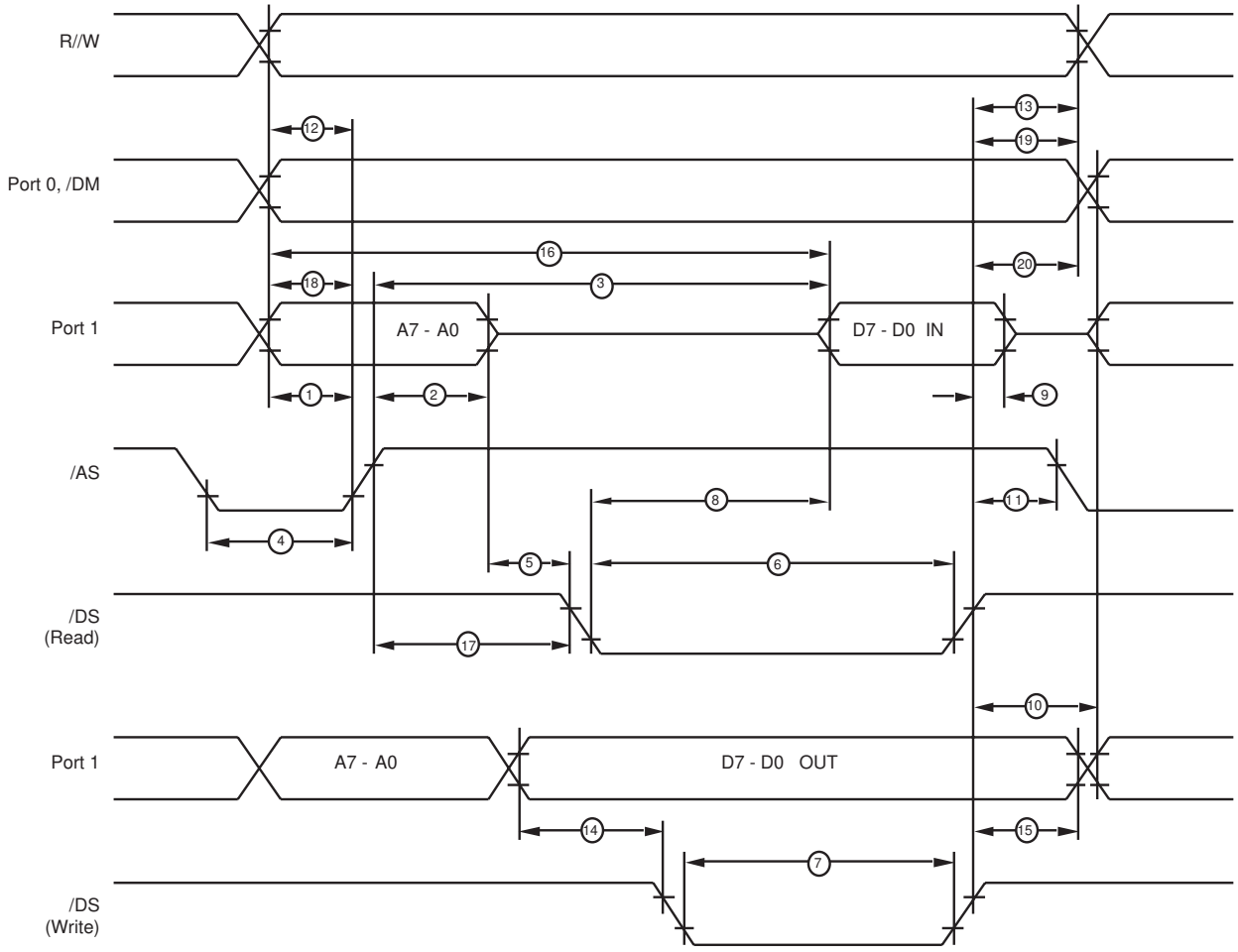

Figure 10. External I/O or Memory Read/Write Timing

Table 9. External I/O or Memory Read and Write Timing

				T_A = 0 °C to +70 °C 16 MHz			
No.	**Symbol**	**Parameter**	**V_{CC}**	**Min.**	**Max.**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS Rising Delay	3.0 V 5.5 V	55 55		ns ns	2
2	TdAS(A)	/AS Rising to Address Float Delay	3.0 V 5.5 V	70 70		ns ns	2
3	TdAS(DR)	/AS Rising to Read Data Required Valid	3.0 V 5.5 V		400 400	ns ns	1, 2 1, 2
4	TwAS	/AS Low Width	3.0 V 5.5 V	80 80		ns ns	2 2
5	Td	Address Float to /DS Falling	3.0 V 5.5 V	0 0		ns ns	
6	TwDSR	/DS (Read) Low Width	3.0 V 5.5 V	300 300		ns ns	1, 2
7	TwDSW	/DS (Write) Low Width	3.0 V 5.5 V	165 165		ns ns	1, 2
8	TdDSR(DR)	/DS Falling to Read Data Required Valid	3.0 V 5.5 V		260 260	ns ns	1, 2
9	ThDR(DS)	Read Data to /DS Rising Hold Time	3.0 V 5.5 V	0 0		ns ns	
10	TdDS(A)	/DS Rising to Address Active Delay	3.0 V 5.5 V	85 95		ns ns	2
11	TdDS(AS)	/DS Rising to /AS Falling Delay	3.0 V 5.5 V	60 70		ns ns	2
12	TdR/W(AS)	R//W Valid to /AS Rising Delay	3.0 V 5.5 V	70 70		ns ns	2
13	TdDS(R/W)	/DS Rising to R//W Not Valid	3.0 V 5.5 V	70 70		ns ns	2
14	TdDW(DSW)	Write Data Valid to /DS Falling (Write) Delay	3.0 V 5.5 V	80 80		ns ns	2
15	TdDS(DW)	/DS Rising to Write Data Not Valid Delay	3.0 V 5.5 V	70 80		ns ns	2
16	TdA(DR)	Address Valid to Read Data Required Valid	3.0 V 5.5 V		475 475	ns ns	1, 2

Table 9. External I/O or Memory Read and Write Timing (Continued)

				T_A = 0 °C to +70 °C 16 MHz			
No.	**Symbol**	**Parameter**	**V_{CC}**	**Min.**	**Max.**	**Units**	**Notes**
17	TdAS(DS)	/AS Rising to /DS Falling Delay	3.0 V 5.5 V	100 100		ns ns	2 2
18	TdDM(AS)	/DM Valid to /AS Falling Delay	3.0 V 5.5 V	55 55		ns ns	2
19	TdDS(DM)	/DS Rise to /DM Valid Delay	3.0 V 5.5 V	70 70		ns ns	
20	ThDS(A)	/DS Rise to Address Valid Hold Time	3.0 V 5.5 V	70 70		ns ns	

Notes:
1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
Standard Test Load
All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

Figure 11 shows additional timing. Table 10 describes the additional timing.

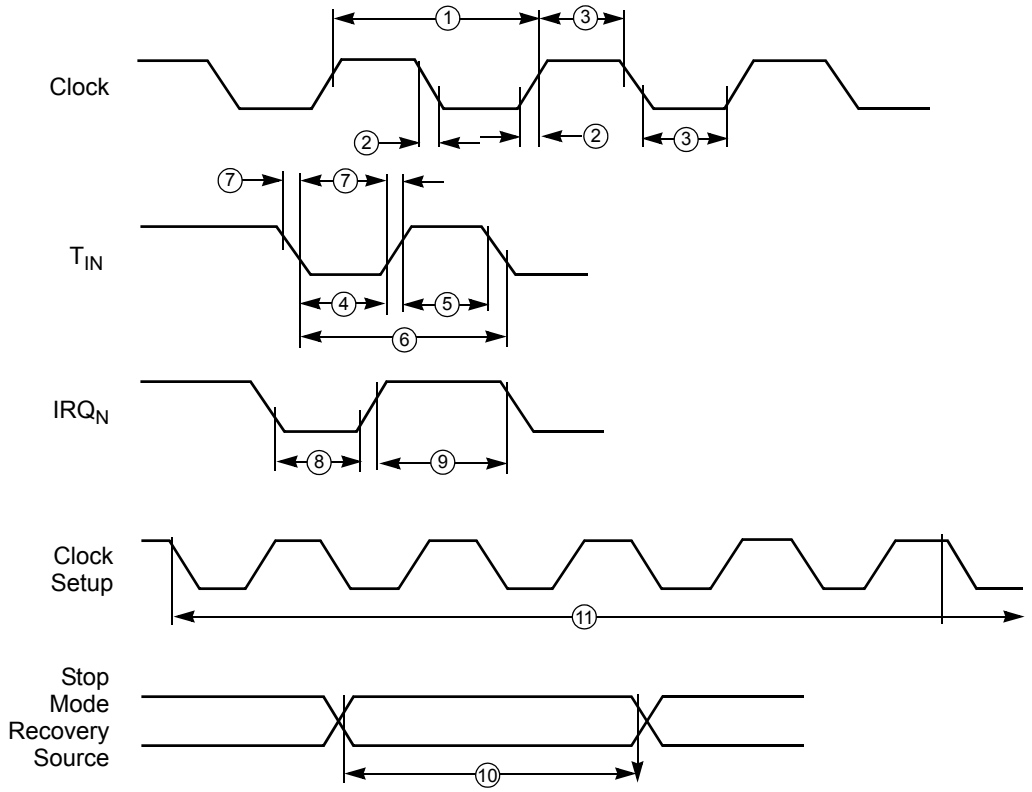

Figure 11. Additional Timing

Table 10. Additional Timing

			T_A = 0°C to +70°C				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.0 V 5.5 V	121 121	DC DC	ns ns	1 1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0 V 5.5 V		25 25	ns ns	1 1
3	TwC	Input Clock Width	3.0 V 5.5 V	37 37		ns ns	1
4	TwTinL	Timer Input Low Width	3.0 V 5.5 V	100 70		ns ns	1
5	TwTinH	Timer Input High Width	3.0 V 5.5 V	3TpC 3TpC			1