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Z87200

Spread-Spectrum Transceiver

Product Specification

PS010202-0601

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Z87200
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PS010202-0601

Z87200

SPREAD-SPECTRUM TRANSCEIVER

FEATURES

Device	Min PN Rate* (Mchips)	Max Data Rate* (Mbps)	Speed (MHz)	Package
Z87200	11	2.048	20/45	100-Pin PQFP

Note: *45 MHz only

- Complete Direct Sequence Spread-Spectrum Transceiver in a Single CMOS IC
- Programmable Functionality Supports Many Different Operational Modes
- Acquires Within One Symbol Duration Using Digital PN Matched Filter
- Two Independent PN Sequences, Each up to 64 Chips Long for Distinct Processing of the Acquisition/Preamble Symbol and Subsequent Data Symbols
- Power Management Features
- Optional Spectral Whitening Code Generation
- Full- or Half-Duplex Operation

Benefits

- High Performance and High Reliability for Reduced Manufacturing Costs
- Ideal for a Wide Range of Wireless Applications Including Data Acquisition Systems, Transaction Systems, and Wireless Local Area Networks (WLANs)
- Fast Response and Very Low Overhead when Operating in Burst Modes
- Allows High Processing Gain to Maximize the Acquisition Probability, then Reduced Code Length for Increased Data Rate
- Reduced Power Consumption
- Randomizes Data to Meet Regulatory Requirements
- Permits Dual Frequency (Frequency Division Duplex) or Single Frequency (Time Division Duplex) Operation
- Small Footprint, Surface Mount

GENERAL DESCRIPTION

The Z87200 is a programmable single-chip, spread-spectrum, direct-sequence transceiver. The Z87200 incorporates Stanford Telecom spread-spectrum and wireless technology and is identical to Stanford Telecom's STEL-2000A. By virtue of its fast acquisition capabilities and its ability to support a wide range of data rates and spread-spectrum parameters, the Z87200 spread-spectrum transceiver supports the implementation of a wide range of burst data communications applications.

Available in both 45- and 20-MHz versions, the Z87200 performs all the digital processing required to implement a fast-acquisition direct sequence (such as pseudonoise- or PN-modulated), spread-spectrum full- or half-duplex system. Differentially encoded BPSK and QPSK are fully supported. The receiver section can also handle differentially encoded pi/4 QPSK. A block diagram of the Z87200 is shown in Figure 1; its pin configuration is shown in Z87200 receive functions integrate the capabilities of a digital downconverter, PN matched filter, and DPSK demodulator, where the input signal is an analog-to-digital converted I.F. signal. Z87200 transmit functions include a differential BPSK/QPSK encoder, PN modulator (spreader), and BPSK/QPSK modulator, where the transmitter output is a sampled digitally modulated signal ready for external digi-

GENERAL DESCRIPTION (Continued)

tal-to-analog conversion (or, if preferred, the spread baseband signal may be output to an external modulator).

These transceiver functions have been designed and integrated for the transmission and reception of bursts of spread data. In particular, the PN Matched Filter has two distinct PN coefficient registers (rather than a single one) in order to speed and improve signal acquisition performance by automatically switching from one to the other upon signal acquisition. The Z87200 is thus optimized to provide reliable, high-speed wireless data communications.

Symbol-Synchronous PN Modulation

The Z87200 operates with symbol-synchronous PN modulation in both transmit and receive modes. Symbol-synchronous PN modulation refers to operation where the PN code is aligned with the symbol transitions and repeats once per symbol. By synchronizing a full PN code cycle over a symbol duration, acquisition of the PN code at the receiver simultaneously provides symbol synchronization, thereby significantly improving overall acquisition time.

As a result of the Z87200's symbol-synchronous PN modulation, the data rate is defined by the PN chip rate and length of the PN code; that is, by the number of chips per symbol, where a “chip” is a single “bit” of the PN code. The PN chip rate, R_c chips/second, is programmable to as much as 1/4 the rate of RXIFCLK, and the PN code length, N, can be programmed up to a value of 64. When operating with BPSK modulation, the data rate for a PN code of length N and PN chip rate R_C chips/sec is R_C/N bps. When operating with QPSK modulation (or $\pi/4$ QPSK with an external modulator), two bits of data are transmitted per symbol, and the data rate for a PN code of length N and PN chip rate R_c chips/sec is $2R_c/N$ bps. Conversely, for a given data rate R_b bps, the length N of the PN code defines the PN chip rate R_c as N x R_b chips/sec for BPSK or as (N x R_b)/2 chips/sec for QPSK.

The data rate R_b and the PN code length N, however, cannot generally be arbitrarily chosen. United States FCC Part 15.247 regulations require a minimum processing gain of 10 dB for unlicensed operation in the Industrial, Scientific, and Medical (ISM) bands, implying that the value of N must be at least 10. To implement such a short code, a Barker code of length 11 would typically be used in order to obtain desirable auto- and cross-correlation properties, although compliance with FCC regulations depends upon the overall system implementation. The Z87200 further includes transmit and receive code overlay generators to insure that signals spread with such a short PN code length possess the spectral properties required by FCC regulations.

The receiver clock rate established by RXIFCLK must be at least four times the receive PN spreading rate and is limited to a maximum speed of 45.056 MHz in the 45 MHz Z87200 and 20.0 MHz in the 20 MHz Z87200. The ensuing discussion is in terms of the 45 MHz Z87200, but the numerical values may be scaled proportionately for the 20 MHz version. As a result of the maximum 45.056 MHz RXIFCLK, the maximum supported PN chip rate is 11.264 Mchips/second. When operating with BPSK modulation, the maximum data rate for a PN code of length N is 11.264/N Mbps. When operating with QPSK modulation (or $\pi/4$ QPSK with an external modulator), two bits of data are transmitted per symbol, and the data rate for a PN code of length N is 22.528/N Mbps. Conversely, for a given data rate R_b, the length N of the PN code employed must be such that the product of N x R_b is less than 11.264 Mchips/sec (for BPSK) or 22.528 Mchips/sec (for QPSK). For the 45 MHz Z87200, then, a PN code length of 11 implies that the maximum data rate that can be supported in compliance with the processing gain requirements of FCC regulations is 2.048 Mbps using differential QPSK. Note again, however, that FCC compliance using the Z87200 with a PN code of length 11 depends upon the overall system implementation.

Z87200 I.F. Interface

The Z87200 receiver circuitry employs an NCO and complex multiplier referenced to RXIFCLK to perform frequency downconversion, where the input I.F. sampling rate and the clock rate of RXIFCLK must be identical. In "complex input" or Quadrature Sampling Mode, external dual analog-to-digital converters (ADCs) sample quadrature I.F. signals so that the Z87200 can perform true full single sideband downconversion directly from I.F. to baseband. At PN chip rates less than one-eighth the value of RXIFCLK, downconversion may also be effected using a single ADC in "real input" or Direct I.F. Sampling Mode.

The input I.F. frequency is not limited by the capabilities of the Z87200. The highest frequency to which the NCO can be programmed is 50% of the I.F. sampling rate (the frequency of RXIFCLK); moreover, the signal bandwidth, NCO frequency, and I.F. sampling rate are all interrelated, as discussed in Higher I.F. frequencies, however, can be supported by using one of the aliases of the NCO frequency generated by the sampling process. For example, a spread signal presented to the Z87200's receiver ADCs at an I.F. frequency of $f_{I.F.}$, where $f_{RXIFCLK} < f_{I.F.} < 2 \times f_{RXIFCLK}$, can generally, as allowed by the signal's bandwidth, be supported by programming the Z87200's NCO to a frequency of ($f_{I.F.} - f_{RXIFCLK}$), as discussed in Appendix A of this product specification. The maximum I.F. frequency is then limited by the track-and-hold capabilities of the ADC(s) selected. Signals at I.F. frequencies up to about 100 MHz can be processed by currently available 8-bit ADCs, but the implementation cost as well as the performance can typically be improved by using an I.F. frequency of 30 MHz or lower. Downconversion to baseband is then accomplished digitally by the Z87200, with a programmable loop filter provided to establish a frequency tracking loop.

Burst and Continuous Data Modes

The Z87200 is designed to operate in either burst or continuous mode: in burst mode, built-in symbol counters allow bursts of up to 65,533 symbols to be automatically transmitted or received; in continuous mode, the data is simply treated as a burst of infinite length. The Z87200's use of a digital PN Matched Filter for code detection and despreading permits signal and symbol timing acquisition in just one symbol. The fast acquisition properties of this design are exploited by preceding each data burst with a single Acquisition/Preamble symbol, allowing different PN codes (at the same PN chip rate) to independently spread the Acquisition/Preamble and data symbols. In this way, a long PN code with high processing gain can be used for the Acquisition/Preamble symbol to maximize the probability of burst detection, and a shorter PN code can be used thereafter to permit a higher data rate.

To improve performance in the presence of high noise and interference levels, the Z87200 receiver's symbol timing recovery circuit incorporates a "flywheel circuit" to maximize the probability of correct symbol timing. This circuit will insert a symbol clock pulse if the correlation peak obtained by the PN Matched Filter fails to exceed the programmed detect threshold at the expected time during a given symbol. During each burst, a missed detect counter tallies each such event to monitor performance and allow a burst to be aborted in the presence of abnormally high interference. A timing gate circuit further minimizes the probability of false correlation peak detection and consequent false symbol clock generation due to noise or interference.

To minimize power consumption, individual sections of the device can be turned off when not in use. For example, the receiver circuitry can be turned off during transmission and, conversely, the transmitter circuitry can be turned off during reception when the Z87200 is operating in a half-duplex/time division duplex (TDD) system. If the NCO is not being used as the BPSK/QPSK modulator (that is, if an external modulator is being used), the NCO can also be turned off during transmission to conserve still more power.

Conclusion

The fast acquisition characteristics of the Z87200 make it ideal for use in applications where bursts are transmitted relatively infrequently. In such cases, the device can be controlled so that it is in full "sleep" mode with all receiver, transmitter, and NCO functions turned off over the majority of the burst cycle, thereby significantly reducing the aggregate power consumption. Since the multiply operations of the PN Matched Filter consume a major part of the overall power required during receiver operation, two independent power-saving techniques are also built into the PN Matched Filter to reduce consumption during operation by a significant factor for both short and long PN spreading codes.

The above features make the Z87200 an extremely versatile and useful device for spread-spectrum data communications. Operating at its highest rates, the Z87200 is suitable for use in wireless Local Area Network implementations, while its programmability allows it to be used in a variety of data acquisition, telemetry, and transaction system applications.

GENERAL DESCRIPTION (Continued)

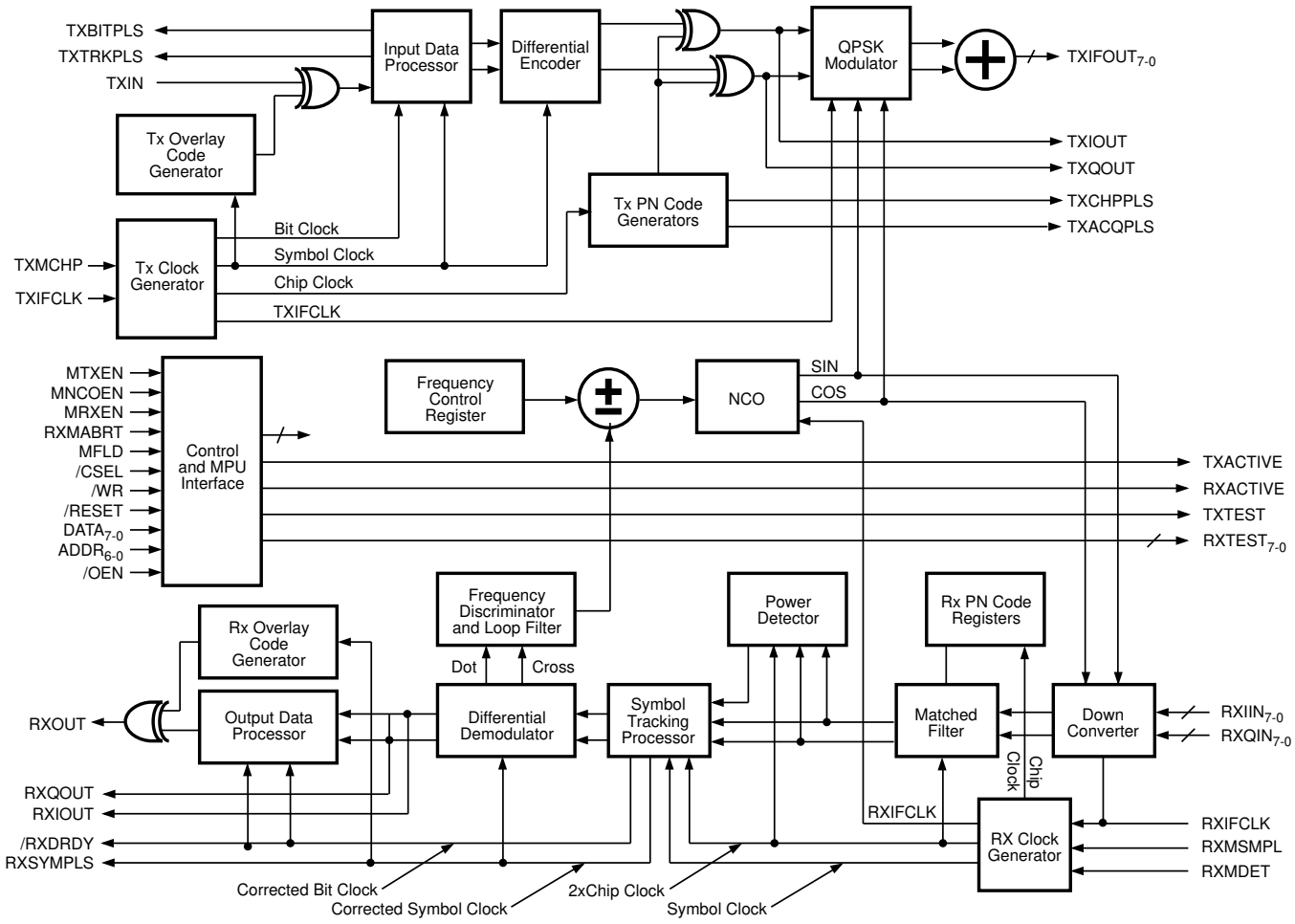

Figure 1. Z87200 Block Diagram

PIN DESCRIPTION

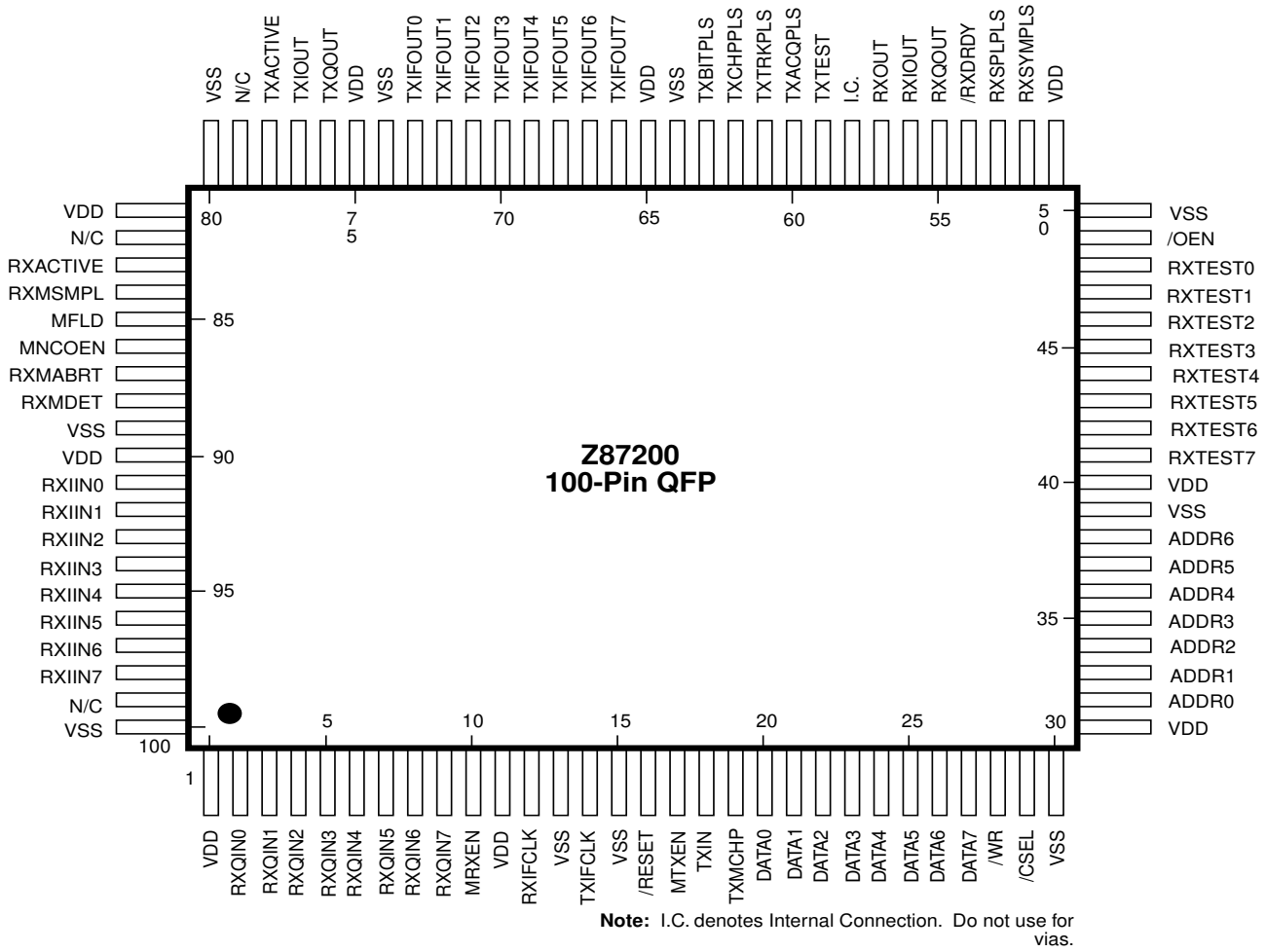

Figure 2. Z87200 100-Pin PQFP Pin Description

PIN DESCRIPTION (Continued)

Table 1. 100-Pin PQFP Pin Description

No	Symbol	Function
1,11,31,40,51,65,75,81,90	V_{DD}	Power Supply
2	RXQIN0	Rx Q-Channel Input (Bit 0; LSB)
3	RXQIN1	Rx Q-Channel Input (Bit 1)
4	RXQIN2	Rx Q-Channel Input (Bit 2)
5	RXQIN3	Rx Q-Channel Input (Bit 3)
6	RXQIN4	Rx Q-Channel Input (Bit 4)
7	RXQIN5	Rx Q-Channel Input (Bit 5)
8	RXQIN6	Rx Q-Channel Input (Bit 6)
9	RXQIN7	Rx Q-Channel Input (Bit 7; MSB)
10	RXXE	Manual Receiver Enable
12	RXIFCLK	Receiver I.F. Clock
13,15,30,39,50,64,74,80,89	V_{SS}	Ground
14	TXIFCLK	Transmitter I.F. Clock
16	/RESET	/Reset
17	MTXE	Manual Transmitter Enable
18	TXIN	Transmitter Input
19	TXMCHP	Transmitter Manual Chip Pulse
20	DATA0	Data Bus (Bit 0; LSB)
21	DATA1	Data Bus (Bit 1)
22	DATA2	Data Bus (Bit 2)
23	DATA3	Data Bus (Bit 3)
24	DATA4	Data Bus (Bit 4)
25	DATA5	Data Bus (Bit 5)
26	DATA6	Data Bus (Bit 6)
27	DATA7	Data Bus (Bit 7; MSB)
28	/WR	Write Bar
29	/CSEL	Chip Select Bar
32	ADDR0	Address Bus (Bit 0; LSB)
33	ADDR1	Address Bus (Bit 1)
34	ADDR2	Address Bus (Bit 2)
35	ADDR3	Address Bus (Bit 3)
36	ADDR4	Address Bus (Bit 4)
37	ADDR5	Address Bus (Bit 5)
38	ADDR6	Address Bus (Bit 6; MSB)
41	RXTEST7	Receiver Test Output (Bit 7)
42	RXTEST6	Receiver Test Output (Bit 6)
43	RXTEST5	Receiver Test Output (Bit 5)
44	RXTEST4	Receiver Test Output (Bit 4)
45	RXTEST3	Receiver Test Output (Bit 3)
46	RXTEST2	Receiver Test Output (Bit 2)
47	RXTEST1	Receiver Test Output (Bit 1)
48	RXTEST0	Receiver Test Output (Bit 0)
49	/OEN	Output Enable Bar
52	RXSYMPLS	Receiver Symbol Pulse
53	RXSPLPLS	Receiver Sample Pulse

Table 1. 100-Pin PQFP Pin Description

No	Symbol	Function
54	/RXDRDY	Receiver Data Ready Bar
55	RXQOUT	Receiver Q Channel Output
56	RXIOUT	Receiver I Channel Output
57	RXOUT	Receiver Output
58	I.C.	[Note]
59	TXTEST	Transmitter Test Output
60	TXACQPLS	Transmitter Acquisition Pulse
61	TXTRKPLS	Transmitter Data Track Pulse
62	TXCHPPLS	Transmitter Chip Pulse
63	TXBITPLS	Transmitter Bit Pulse
66	TXIFOUT7	Tx I.F. Output (Bit 7, MSB)
67	TXIFOUT6	Tx I.F. Output (Bit 6)
68	TXIFOUT5	Tx I.F. Output (Bit 5)
69	TXIFOUT4	Tx I.F. Output (Bit 4)
70	TXIFOUT3	Tx I.F. Output (Bit 3)
71	TXIFOUT2	Tx I.F. Output (Bit 2)
72	TXIFOUT1	Tx I.F. Output (Bit 1)
73	TXIFOUT0	Tx I.F. Output (Bit 0, LSB)
76	TXQOUT	Tx Q-Channel Output
77	TXIOUT	Tx I-Channel Output
78	TXACTIVE	Transmitter Active
79,82	N.C.	No Connection
83	RXACTIVE	Receiver Active
84	RXMSMPL	Receiver Manual Sample Clock
85	MFLD	Manual Frequency Load
86	MNCOEN	Manual NCO Enable
87	RXMABRT	Receiver Manual Abort
88	RXMDET	Receiver Manual Detect
91	RXIIN0	Rx I-Channel Input (Bit 0; LSB)
92	RXIIN1	Rx I-Channel Input (Bit 1)
93	RXIIN2	Rx I-Channel Input (Bit 2)
94	RXIIN3	Rx I-Channel Input (Bit 3)
95	RXIIN4	Rx I-Channel Input (Bit 4)
96	RXIIN5	Rx I-Channel Input (Bit 5)
97	RXIIN6	Rx I-Channel Input (Bit 6)
98	RXIIN7	Rx I-Channel Input (Bit 7; MSB)
99	N.C.	No Connection
100	V_{SS}	Ground

Note: I.C. denotes Internal Connection. Do not use for vias.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Range	Units
T_{STG}	Storage Temperature	–55 to +150	°C
V_{DD} (max)	Supply Voltage on V_{DD}	–0.3 to + 7	Volts
V_I(max)	Input Voltage	–0.3 to V_{DD}+0.3	Volts
I_I	DC Input Current	±10	mA
T_A	Operating Temperature (Ambient)	0 to +70	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

D.C. CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C		Typ		
Symbol	Parameter	Min	Max	@ 25°C	Units	Conditions
I_{DDQ}	Supply Current, Quiescent		1.0		mA	Static, no clock
I_{DD}	Supply Current, Operational		380 170	[Note]	mA mA	$f_{RXIFCLK}$ = 45.056 MHz $f_{RXIFCLK}$ = 20 MHz
V_{IH} (min)	High Level Input Voltage	0.7V_{DD}	V_{DD}+.3	2.6	Volts	Logic ‘1’
V_{IL}(min)	Low Level Input Voltage	V_{SS}–.3	0.2V_{DD}	1.5	Volts	Logic ‘0’
I_{IH} (min)	High Level Input Current		10		µA	All inputs, V_{IN} = V_{DD}
I_{IL} (max)	Low Level Input Current		–10		µA	TXIFCLK, RXIFCLK, /RESET only, V_{IN} = V_{SS}
I_{IL}(max)	Low Level Input Current	–130	–15	–45	µA	All other inputs, V_{IN} = V_{SS}
V_{OH}(min)	High Level Output Voltage	V_{DD}–0.4			Volts	I_O = –2.0 mA, all outputs
V_{OL}(max)	Low Level Output Voltage		0.4	0.1	Volts	I_O = +2.0 mA, all outputs
I_{OS}	Output Short Circuit Current	20	130	65	mA	V_{OUT} = V_{DD}, V_{DD} = max
C	Input Capacitance	2			pF	All inputs
C_{OUT}	Output Capacitance			4	pF	All outputs

Notes:
1. The operational supply current depends on how the Z87200 is configured. Typical current consumption can be approximated as follows:
2. I_{DD}=5x$f_{RXIFCLK}$ +13 x f_{CHIP} mA,
3. where $f_{RXIFCLK}$ is the frequency of RXIFCLK and f_{CHIP} is the PN chip rate, both in MHz.

A.C. CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C			
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
t_{SU}	/CSEL, ADDR, DBUS to WRITE Setup	5		ns	
t_{HD}	WRITE to CSEL, ADDR, DBUS Hold	5		ns	
t_W	WRITE Pulse Width	5		ns	

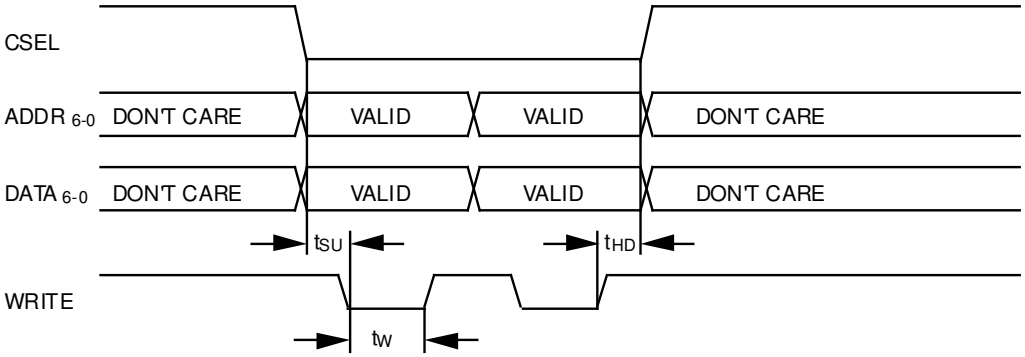

Figure 3. Microprocessor Interface Timing

A.C. CHARACTERISTICS - TRANSMITTER

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A 0°C to +70°C			
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
$f_{TXIFCLK}$	TXIFCLK Frequency		45.056 20.0	MHz MHz	Z0200045FSC Z0200020FSC or if TXIFOUT is used
t_{CH}	TXIFCLK Pulse width, High	10		ns	
t_{CL}	TXIFCLK Pulse width, Low	10		ns	
t_{SU}	TXIN to TXIFCLK setup	3		ns	
t_{HD}	TXIN to TXIFCLK hold	5		ns	
t_{CT}	TXIFCLK to TXBITPLS, TXTRKPLS, XACQPLS, TXIOUT or TXQOUT delay		35	ns	

Notes:

1. The number of TXIFCLK cycles per cycle of TXCHPPLS is determined by the data stored in bits 5-0 of address 41_H. It is shown as 2 in Figure 8 but can be set from 2 to 64.
2. The width of the TXBITPLS, TXTRKPLS and TXACQPLS signal pulses is equal to the period of TXCHPPLS; that is, equal to the PN chip period.
3. In QPSK mode, the TXBITPLS signal pulses high twice during each symbol period, once during the center chip and once during the last chip. If the number of chips per symbol is even, the number of chip periods between the TXBITPLS pulse at the end of the previous symbol and the one in the center of the symbol will be one more than the number of chip periods between the TXBITPLS pulse in the center of the symbol and the one at the end. The falling edge of the second pulse corresponds to the end of the symbol period.
4. The TXTRKPLS signal pulses high once each symbol period, during the last chip period of that symbol. The falling edge corresponds to the end of the symbol period.
5. The TXACQPLS signal pulses high once each burst, transmission, during the last chip of the Acquisition/Preamble symbol. The falling edge corresponds to the end of this symbol period.

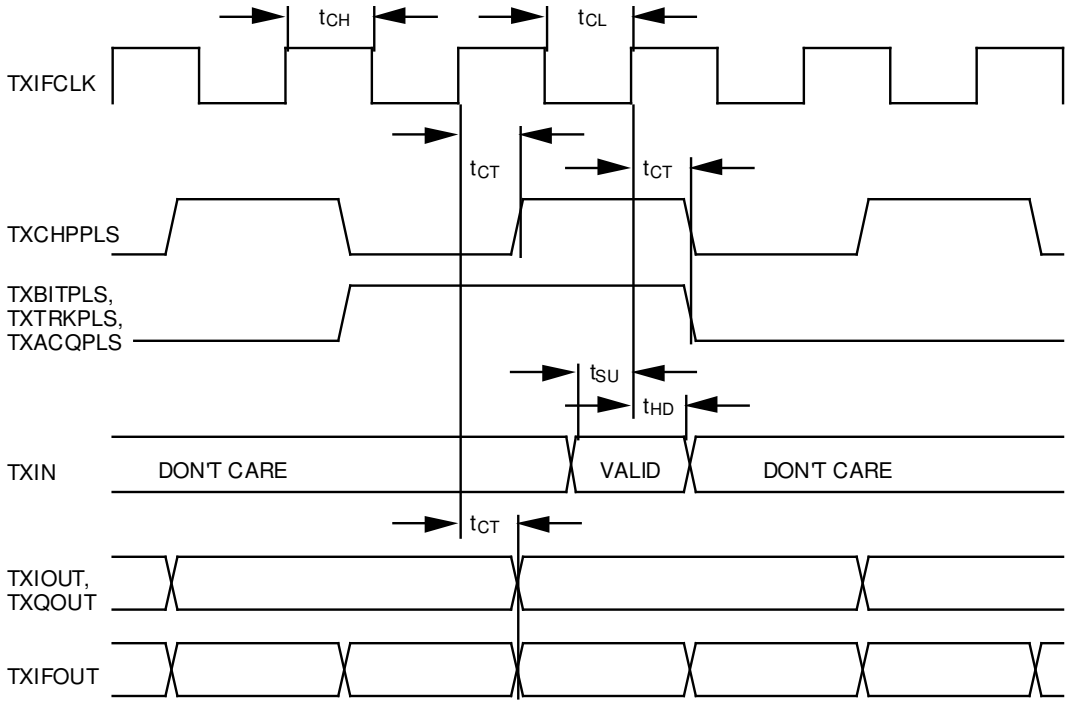

Figure 4. Transmitter Input/Output Timing

A.C. CHARACTERISTICS - RECEIVER

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C			
Symbol	**Parameter**	**Min**	**Max.**	**Units**	**Conditions**
$f_{RXIFCLK}$	RXIFCLK Frequency		45.056 20.0	MHz MHz	Z8720045FSC Z8720020FSC
t_{CH}	RXIFCLK Pulse width, High	10		ns	
t_{CL}	RXIFCLK Pulse width, Low	10		ns	
t_{SU}	RXIIN or RXQIN to RXIFCLK setup	3		ns	
t_{HD}	RXIIN or RXQIN to RXIFCLK hold	7		ns	
t_{CR}	RXIFCLK to RXSPLPLS, RXSYMPLS, or /RXDRDY delay		35	ns	
t_{CD}	RXIFCLK to RXOUT, RXIOUT, or RXQOUT delay		35	ns	

Notes:

1. The number of RXIFCLK cycles per cycle of RXSPLPLS is determined by the data stored in bits 5-0 of address 02_H. It is shown as 2 in Figure 9, but can be set from 2 to 64.
2. The rising edge of /RXDRDY should be used to clock out the data (RXOUT, RXIOUT, or RXQOUT).

A.C. CHARACTERISTICS

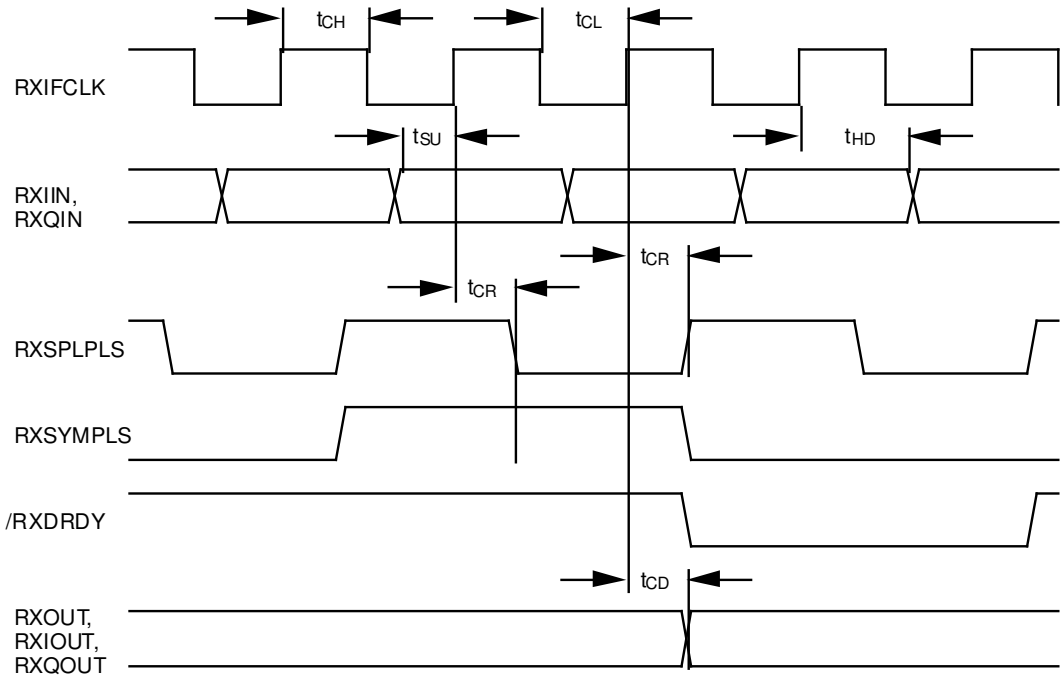

Figure 5. Receiver Input/Output

AC CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C		
Symbol	**Parameter**	**Min**	**Max**	**Units**
t_{D1}	/OEN low to RXTEST $_{7-0}$ active	11		ns
t_{D2}	/OEN high to RXTEST $_{7-0}$ tri-state	7		ns

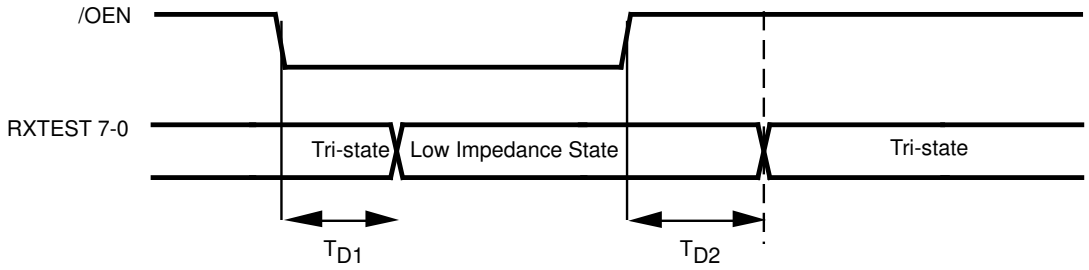

Figure 6. /OEN to RXTEST 7-0 Timing

FUNCTIONAL BLOCKS

Transmit and Receive Clock Generators

Timing in the transmitter and receiver sections of the Z87200 is controlled by the Transmit and Receive Clock Generator Blocks. These blocks are programmable dividers providing signals at the chip and symbol rates (as well as at multiples and sub-multiples of these frequencies) as programmed through the Z87200's control registers. If desired, the complete independence of the transmitter and receiver sections allows the transmit and receive clocks to be mutually asynchronous. Additionally, the Z87200 allows external signals to be provided as references for the transmit (TXMCHP) and receive (RXMSMPL) chip rates. Given the transmit PN chip rate, the PN-synchronous transmit symbol rate is then derived from the programmed number of PN chips per transmit symbol. At the receiver, symbol synchronization and the receive symbol rate are determined from processing of the PN matched filter output, or, if desired, can be provided from the programmed number of PN chips per receive symbol or an external symbol synch symbol, RXMDET. Burst control is achieved by means of the transmit and receive Symbols per Burst counters. These programmable 16-bit counters allow the Z87200 to operate automatically in burst mode, stopping at the end of each burst without the need of any external counters.

Input and Output Processors

When the transmitter and receiver are operating in QPSK mode, the data to be transmitted and the received data are processed in pairs of bits (dibits), one bit for the in-phase (I) channel and one for the quadrature (Q) channel. Dibits are transmitted and received as single differentially encoded QPSK symbols. Single-bit I/O data is converted to and from this format by the Input and Output Processors, accepting TXIN as the serial data to be transmitted and producing RXOUT as the serial data output. If desired, the received data is also available at the RXIOUT and RXQOUT pins in (I and Q) dibit format prior to dibit-to-serial conversion. While receive timing is derived by the Z87200 Symbol Tracking Processor, transmit timing is provided by the Input Processor. In BPSK mode, the Input Processor will generate the TXBITPLS signal once per symbol to request each bit of data, while in QPSK mode it will generate the TXBITPLS signal twice per symbol to request the two bits of data corresponding to each QPSK symbol.

Differential Encoder

Data to be transmitted is differentially encoded before being spread by the transmit PN code. Differential encoding of the signal is fundamental to operation of the Z87200's receiver: the Z87200's DPSK Demodulator computes "Dot" and "Cross" product functions of the current and previous symbols' downconverted I and Q signal components in order to perform differential decoding as an intrinsic part of DPSK demodulation.

The differential encoding scheme depends on whether the modulation format is to be BPSK or QPSK. For DBPSK, the encoding algorithm is straightforward: output bit(k) equals input bit(k) $\oplus$ output bit(k–1), where $\oplus$ represents the logical XOR function. For DQPSK, however, the differential encoding algorithm, as shown in Table 2, is more complex since there are now sixteen possible new states depending on the four possible previous output states and four possible new input states.

Table 2. QPSK Differential Encoder Sequence

New Input		Previously Encoded OUT(I,Q)$_{K-1}$							
IN(I,Q)$_K$		**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**
0	0	0	0	0	1	1	1	1	0
0	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	0	1
1	0	1	0	0	0	0	1	1	1
Newly Encoded OUT (I,Q)K									

Transmitter PN Code Generation

When the Z87200 is used for burst signal operation, each burst is preceded by an Acquisition/Preamble symbol to facilitate acquisition. This Acquisition/Preamble symbol is automatically generated by the Z87200's transmitter before information data symbols are accepted for transmission. Two separate and independent PN codes may be employed: one for spreading the Acquisition/Preamble symbol, and one for the subsequent information data symbols. As a result, a much higher processing gain may be used for signal acquisition than for signal tracking in order to improve burst acquisition performance.

The Transmitter Acquisition/Preamble and Transmitter Data Symbol PN code lengths are completely independent of each other and can be up to 64 chips long. Transmit PN codes are programmed in the Z87200 as binary code values. The number of Transmitter Chips per Acquisition/Preamble Symbol is set by the value stored in bits 5-0 of address 43_H, and the Transmitter Acquisition/Preamble Symbol Code coefficient values are stored in addresses 44_H to $4B_H$. The number of Transmitter Chips per Data Symbol is set by the data stored in address 42_H, and the Transmitter Data Symbol Code coefficient values are stored in addresses $4C_H$ to 53_H.

A rising edge of the MTXEN input or of bit 1 of address 37_H causes the Z87200 to begin the transmit sequence by transmitting a single symbol using the Acquisition/Preamble PN code. The completion of transmission of the Acquisition/Preamble symbol is indicated with TXACQPLS, while the ongoing transmission of data symbols is signaled with TXTRKPLS. Data bits to be transmitted after the Acquisition/Preamble symbol are requested with TXBITPLS, where a single pulse requests data in BPSK mode and two pulses request data in QPSK mode. The user data symbols are then PN modulated using the Transmitter Data Symbol PN code.

The PN spreading codes are XORed with the data bits (in BPSK mode) or bit pairs (in QPSK mode) to transmit one complete code sequence for every Acquisition/Preamble and data symbol at all times. The resulting spread I and Q channel signals are brought out as the TXIOUT and TXQOUT signals for use by an external modulator and are also fed into the Z87200's internal on-chip modulator. In BPSK mode, only TXIOUT is used by the Z87200's modulator. If an external QPSK modulator is used, the carrier should be modulated as shown in Table 3 to be compatible with the Z87200 receiver.

Table 3. DQPSK Differential Encoder Sequence

I, Q BIts		Signal Quadrant	Quadrant Diagram	
0	0	First	2nd	1st
1	0	Second	3rd	4th
1	1	Third		
0	1	Fourth		

BPSK/QPSK Modulator

The Z87200 incorporates an on-chip BPSK/QPSK modulator which modulates the encoded and spread transmit signal with the sine and cosine outputs of the Z87200's NCO to generate a digitized I.F. output signal, $TXIFOUT_{7-0}$. Since the NCO operates at a rate defined by RXIFCLK, the BPSK/QPSK modulator output is also generated at this sampling rate, and, consequently, TXIFCLK must be held common with RXIFCLK to operate the Z87200's BPSK/QPSK Modulator. The digital modulator output signal can then be fed into an external 8-bit DAC (operating at RXIFCLK) to generate an analog I.F. transmit signal, where the chosen I.F. is the Z87200's programmed NCO frequency or one of its aliases with respect to the output sampling rate, RXIFCLK. Please note that operation of the BPSK/QPSK modulator is only specified to 20 MHz; that is, if RXIFCLK/TXIFCLK is greater than 20 MHz in the system design, it is recommended that the baseband transmit outputs of the Z87200 be used with an external BPSK/QPSK modulator.

When the Z87200 is set to transmit in BPSK mode (by setting bit 0 of address 40_H high), identical signals are applied to both the I and Q channels of the modulator so that the modulated output signal occupies only the first and third quadrants of the signal space defined in Note that the modulator itself cannot generate $\pi/4$ QPSK signals, but the Z87200 can receive such signals and can be used with an external modulator for their transmission.

FUNCTIONAL BLOCKS (Continued)

Frequency Control Register and NCO

The Z87200 incorporates a Numerically Controlled Oscillator (NCO) to synthesize a local oscillator signal for both the transmitter's modulator and receiver's downconverter. The NCO is clocked by the master receiver clock signal, RXIFCLK, and generates quadrature outputs with 32-bit frequency resolution. The NCO frequency is controlled by the value stored in the 32-bit Frequency Control Register, occupying 4 bytes at addresses 03_H to 06_H. To avoid destructive in-band aliasing, the NCO should not be programmed to be greater than 50% of RXIFCLK. As desired by the user, the output of the Z87200 receiver's Loop Filter can then be added or subtracted to adjust the NCO's frequency control word and create a closed-loop frequency tracking loop. If the receiver is disabled, either manually or automatically at the end of a burst, the Loop Filter output correcting the NCO's Frequency Control Word is disabled. When simultaneously operating both the transmitter and receiver, however, the receiver's frequency tracking loop affects the NCO signals to both the receive and transmit sides, a feature which can either be used to advantage in the overall system design or must be compensated in the programming of the Z87200 or in the system design.

Downconverter

The Z87200 incorporates a Quadrature (Single Sideband) Downconverter which digitally downconverts the sampled and digitized receive I.F. signal to baseband. Use of the Loop Filter and the NCO's built-in frequency tracking loop permits the received signal to be accurately downconverted to baseband.

The Downconverter includes a complex multiplier in which the 8-bit receiver input signal is multiplied by the sine and cosine signals generated by the NCO. In Quadrature Sampling Mode, two ADCs provide quadrature (complex) inputs I_{IN} and Q_{IN}, while, in Direct I.F. Sampling Mode, a single ADC provides I_{IN} as a real input. The input signals can be accepted in either two's complement or offset binary formats according to the setting of bit 3 of address 01_H. In Direct I.F. Sampling Mode, the unused RXQIN Q channel input (Q_{IN}) should be held to "zero" according to the ADC input format selected. The outputs of the Downconverter's complex multiplier are then:

$$I_{OUT} = I_{IN} \cdot \cos(\omega t) - Q_{IN} \cdot \sin(\omega t)$$

$$Q_{OUT} = I_{IN} \cdot \sin(\omega t) + Q_{IN} \cdot \cos(\omega t)$$

$$\text{where } \omega = 2\pi f_{nco}$$

These outputs are fed into the I and Q channel Integrate and Dump Filters. The Integrate and Dump Filters allow the samples from the complex multiplier (at the I.F. sampling rate, the frequency of RXIFCLK) to be integrated over a number of sample periods. The dump rate of these filters (the baseband sampling rate) can be controlled either by an internally generated dump clock or by an external input signal (RXMSMPL) according to the setting of bit 0 of address 01_H. Note that, while the receiver will extract exact PN and symbol timing information from the received signal, the baseband sampling rate must be twice the nominal PN chip rate for proper receiver operation and less than or equal to one-half the frequency of RXIFCLK. If twice the PN chip rate is a convenient integer sub-multiple of RXIFCLK, then an internal clock can be derived by frequency dividing RXIFCLK according to the divisor stored in bits 5-0 of address 02_H; otherwise, an external baseband sampling clock provided by RXMSMPL must be used.

The I.F. sampling rate, the baseband sampling rate, and the input signal levels determine the magnitudes of the Integrate and Dump Filters' accumulator outputs, and a programmable viewport is provided at the outputs of the Integrate and Dump Filters to select the appropriate output bits as the 3-bit inputs to the PN Matched Filter. The viewport circuitry here and elsewhere within the Z87200's receiver is designed with saturation protection so that extreme values above or below the selected range are limited to the correct maximum or minimum value for the selected viewport range. Both viewports for the I and Q channels of the Integrate and Dump Filters are controlled by the values stored in bits 7-4 of address 01_H.

Receiver PN Code Register and PN Matched Filter

As discussed for the Z87200 transmitter, the Z87200 receiver is designed for burst signal operation in which each burst begins with a single Acquisition/Preamble symbol and is then followed by data symbols for information transmittal. Complementing operation of the Z87200's transmitter, two separate and independent PN codes may be employed in the receiver's PN Matched Filter, one for despreading the Acquisition/Preamble symbol, and one for the information data symbols. The code lengths are completely independent of each other and can be each up to 64 chips long. A block diagram of the PN Matched Filter is shown in Figure 3.

The Z87200 contains a fully programmable 64-tap complex (dual I and Q channel) PN Matched Filter with coefficients which can be set to ±1 or zero according to the contents of either the Acquisition/Preamble or Data Symbol Code Coefficient Registers. By setting the coefficients of the end taps of the filter to zero, the effective length of the filter can be reduced for use with PN codes shorter than 64 bits. Power consumption may also be reduced by turning off those blocks of 7 taps for which all the coefficients are zero, using bits 6-0 of address 39H. Each ternary coefficient is stored as a 2-bit number so that a PN code of length N is stored as N 2-bit non-zero PN coefficients. Note that, as a convention, throughout this document the first PN Matched Filter tap encountered by the signal as it enters the I and Q channel tapped delay lines is referred to as “Tap 0.” Tap 63 is then the last tap of the PN Matched Filter.

The start of each burst is expected to be a single symbol PN-spread by the Acquisition/Preamble code. The receiver section of the Z87200 is automatically configured into acquisition mode so that the Matched Filter Acquisition/Preamble Coefficients stored in addresses 07_H to 16_H are used to despread the received signal. Provided that this symbol is successfully detected, the receiver will automatically switch from acquisition mode, and the Matched Filter Data Symbol Coefficients stored in addresses 17_H to 26_H will then be used to despread subsequent symbols.

To allow the system to sample the incoming signal asynchronously (at the I.F. sampling rate) with respect to the PN spreading rate, the PN Matched Filter is designed to operate with two signal samples (at the baseband sampling rate) per chip. A front end processor (FEP) operating on both the I and Q channels averages the incoming data over each chip period by adding each incoming baseband sample to the previous one:

$$FEP_{OUT} = FEP_{IN} (1 + z^{-1})$$

After the addition, the output of the FEP is rounded to a 3-bit offset 2’s complement word with an effective range of ±3.5 such that the rounding process does not introduce any bias to the data. The FEP can be disabled by setting bit 0 of address 27_H to 1, but for normal operation the FEP should be enabled.

The PN Matched Filter computes the cross-correlation between the I and Q channel signals and the locally stored PN code coefficients at the baseband sampling rate, which is twice per chip. The 3-bit signals from each tap in the PN Matched Filter are multiplied by the corresponding coefficient in two parallel tapped delay lines. Each delay line consists of 64 multipliers which multiply the delayed 3-bit signals by zero or ±1 according to the value of the tap coefficient. The products from the I and Q tapped delay lines are added together in the I and Q Adders to form the sums of the products, representing the complex cross-correlation factor. The correlation I and Q outputs are thus:

$$Output_{(I, Q)} = \sum_{n=0}^{n=63} Data_{n(I, Q)} * Coefficient_{n(I, Q)}$$

These I and Q channel PN Matched Filter outputs are 10-bit signals, with I and Q channel programmable viewports provided to select the appropriate output bits as the 8-bit inputs to the Power Detector and DPSK Demodulator blocks. Both I and Q channel viewports are jointly controlled by the data stored in bits 1-0 of address 28_H and are saturation protected.

Two power saving methods are used in the PN Matched Filter of the Z87200. As discussed previously, the first method allows power to be shut off in the unused taps of the PN Matched Filter when the filter length is configured to be less than 64 taps. The second method is a proprietary technique that (transparently to the user) shuts down the entire PN Matched Filter during portions of each symbol period.

FUNCTIONAL BLOCKS (Continued)

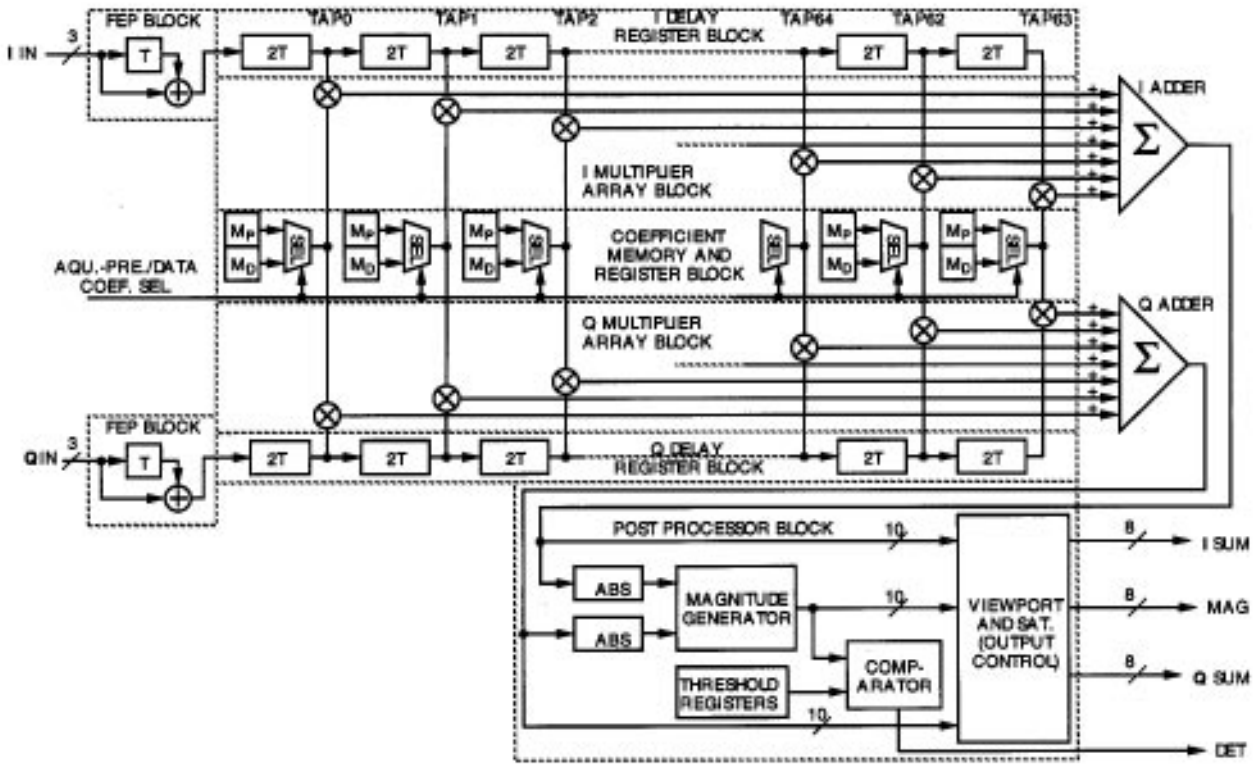

Figure 7. PN Matched Filter

Power Detector

The complex output of the PN Matched Filter is fed into a Power Detector which, for every cycle of the internal baseband sampling clock, computes the magnitude of the vector of the I and Q channel correlation sums,

$$\sqrt{I^2(K)+Q^2(k)}$$

, where the magnitude is approximated as

$$\text{Max}\{\text{Abs}(I),\text{Abs}(Q)\} + 1/2\ \text{Min}\{\text{Abs}(I), \text{Abs}(Q)\}.$$

This 10-bit value represents the power level of the correlated signal during each chip period and is used in the Symbol Tracking Processor.

Symbol Tracking Processor

The output of the Power Detector Block represents the signal power during each chip period. Ideally, this output will have a high peak value once per symbol (that is, once per PN code cycle) when the code sequence of the received signal in the PN Matched Filter is the same as (and is aligned in time with) the reference PN code used in the PN Matched Filter. At that instant, the I and Q channel outputs of the PN Matched Filter are, theoretically, the optimally despread I and Q symbols.

To detect this maximum correlation in each symbol period, the signal power value is compared against a 10-bit user-programmable threshold value. A symbol clock pulse is generated each time the power value exceeds the threshold value to indicate a symbol detect. Since the Acquisition/Preamble symbol and subsequent data symbols can have different PN codes with different peak correlation values (which depend on the PN code length and code properties), the Z87200 is equipped with two separate threshold registers to store the Acquisition/Preamble Threshold value (stored in addresses 29_H and $2A_H$) and the Data Symbol Threshold value (stored in addresses $2B_H$ and $2C_H$). The device will automatically use the appropriate value depending on whether it is in acquisition mode or not.

Since spread-spectrum receivers are frequently designed to operate under extremely adverse signal-to-noise ratio conditions, the Z87200 is equipped with a “flywheel circuit” to enhance the operation of the symbol tracking function by introducing memory to the PN Matched Filter operation. This circuit is designed to ignore false detects at inappropriate times in each symbol period and to insert a symbol clock pulse at the appropriate time if the symbol detection is missed. The flywheel circuit operates by its *a priori* knowledge of when the next detect pulse is expected. *A priori*, the expected pulse will occur one symbol period after the last correctly detected one, and a window of ±1 baseband sample time is therefore used to gate the detect pulse. Any detects generated outside this time window are ignored, while a symbol detect pulse will be inserted into the symbol clock stream if the power level does not exceed the threshold within the window, corresponding to a missed detect. An inserted symbol detect signal will be generated precisely one symbol after the last valid detect, the nominal symbol length being determined by the value of Rx Chips Per Data Symbol stored in address $2D_H$.

The cross-correlation characteristics of a noisy received signal with the noise-free local PN code used in the Z87200’s PN Matched Filter may result in “smearing” of the peak power value over adjacent chip periods. Such smearing can result in two or three consecutive power values (typically, the on-time and one-sample early and late values) exceeding the threshold. A maximum power selector circuit is incorporated in the Z87200 to choose the highest of any three consecutive power levels each time this occurs, thereby enhancing the probability that the optimum symbol timing will be chosen in such cases. If desired, this function can be disabled by setting bit 3 of address 30_H high.

The Z87200 also includes a circuit to keep track of missed detects; that is, those cases where no peak power level exceeds the set threshold. An excessively high rate of missed detects is an indication of poor signal quality and can be used to abort the reception of a burst of data. The number of symbols expected in each receive burst, up to a maximum of 65,533, is stored in addresses $2E_H$ and 30_H. A counter is used to count the number of missed detects in each burst, and the system can be configured to automatically abort a burst and return to acquisition mode if this number exceeds the Missed Detects per Burst Threshold value stored in address $2F_H$. Under normal operating conditions, the Z87200 will automatically return to acquisition mode when the number of symbols processed in the burst is equal to the value of the data stored in address $2E_H$ and 30_H. To permit the processing of longer bursts or continuous data, this function can be disabled by setting bit 6 of address 30_H high.

Differential Demodulator

Both DPSK demodulation and carrier discrimination are supported in the Z87200 receiver by the calculation of “Dot” and “Cross” products using the despread I and Q channel information generated by the PN Matched Filter for the current and previous symbols. A block diagram of the DPSK Demodulator’s I and Q channel processing is shown in Let I_k and Q_k represent the I and Q channel outputs, respectively, for the k^{th} symbol. The Dot and Cross products can then be defined as:

$$\text{Dot}(k) = I_k I_{k-1} + Q_k Q_{k-1}; \text{ and,}$$

$$\text{Cross}(k) = Q_k I_{k-1} - I_k Q_{k-1}.$$

Examination of these products in the complex plane reveals that the Dot and Cross products are the real and imaginary results, respectively, of complex multiplication of the current and previous symbols. The Dot product alone thus allows determination of the phase shift between successive BPSK symbols, while the Dot and Cross products together allow determination of the integer number of π/2 phase shifts between successive QPSK symbols. Differential encoding of the source data implies that an absolute phase reference is not required, and thus knowledge of the phase shift between successive symbols derived from the Dot and Cross products unambiguously permits correct demodulation.

Implementation of this approach is simplified if the polarities (the signs) alone of the Dot and Cross products provide the information required to make the correct symbol decision. For BPSK and π/4 QPSK signals, no modifications are needed: in BPSK, the sign of the Dot product fully captures the signal constellation, while, in π/4 QPSK, the signal constellation intrinsically includes the phase rotation needed to align the decision boundaries with the four possible combinations of the Dot and Cross product polarities. For QPSK signals, a fixed phase rotation of π/4 (45°) is introduced in the DPSK Demodulator to the previous symbol to simplify the decision algorithm. Rotation of the previous symbol is controlled by the settings of bits 0 and 1 of address 33_H, allowing the previous symbol to be rotated by 0° or ±45°. As noted, for BPSK or π/4 QPSK signals, a rotation of 0° should be programmed, but, for QPSK signals,

FUNCTIONAL BLOCKS (Continued)

a –45° signal rotation must be programmed to optimize the constellation boundaries in the comparison process between successive symbols. Note also that introduction of a ±45° rotation introduces a scaling factor of 1/√2 to the signal level in the system as discussed in Theory of Operation, where this factor should be taken into account when calculating optimum signal levels and viewport settings after the DPSK Demodulator

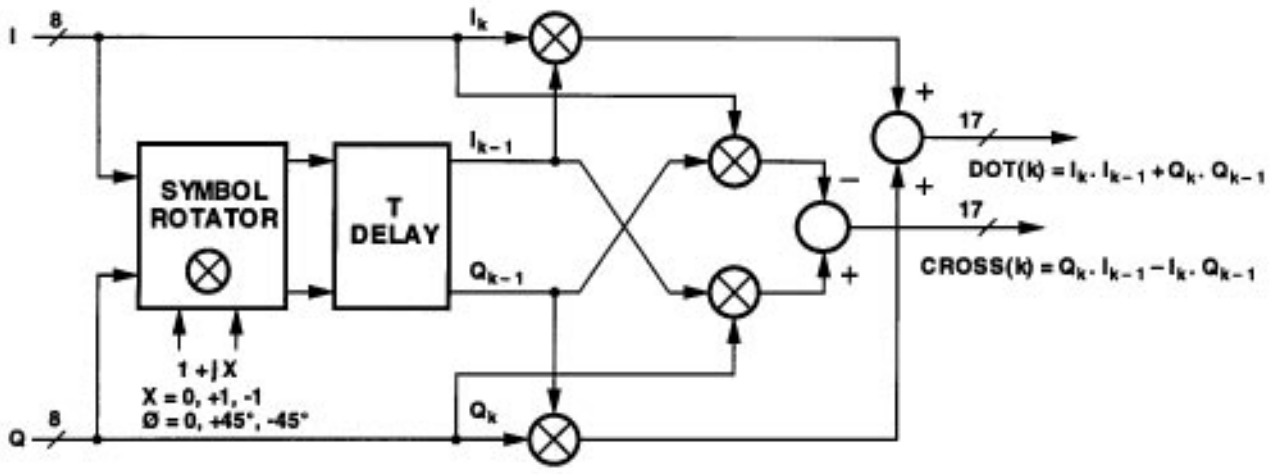

Figure 8. DPSK Demodulator I and Q Channel Processing

Frequency Discriminator and Loop Filter

The Frequency Discriminator uses the Dot and Cross products discussed above to generate the AFC signal for the frequency acquisition and tracking loop, as illustrated in The specific algorithm used depends on the signal modulation type and is controlled by the setting of bit 2 of address 33_H. When bit 2 is set low, the Frequency Discriminator circuit is in BPSK mode and the following algorithm is used to compute the Frequency Discriminator (FD) function:

FD = Cross x Sign[Dot],

where Sign[.] represents the polarity of the argument. When bit 2 is set high, the discriminator circuitry is in QPSK mode and the carrier discriminator function is instead calculated as:

FD = (Cross x Sign[Dot]) – (Dot x Sign[Cross]).

In both cases, the Frequency Discriminator function provides an error signal that reflects the change in phase between successive symbols. With the symbol period known, the error signal can equivalently be seen as a frequency error signal. As a practical matter, the computation of the Frequency Discriminator function results in a 17-bit signal, and a programmable saturation protected viewport is provided to select the desired output bits as the 8-bit input to the Loop Filter Block. The viewport is controlled by the value stored in bits 7-4 of address 33_H.

The Loop Filter is implemented with a direct gain (K1) path and an integrated or accumulated (K2) path to filter the Frequency Discriminator error signal and correct the frequency tracking of the Downconverter. The order of the Loop Filter transfer function can be set by enabling or disabling the K1 and K2 paths, and the coefficient values can be adjusted in powers of 2 from 2^0 to 2^{21}. The Loop Filter transfer function is:

Transfer Fn. = K1 + 1/4 K2

The factor of 1/4 results from truncation of the 2 LSBs of the signal in the integrator path of the loop so that, when added to the signal in the direct path, the LSBs of the signals are aligned. The coefficients K1 and K2 are defined by the data stored in bits 4-0 of addresses 35_H and 34_H, respectively. In addition, bit 5 of addresses 35_H and 34_H control whether the K1 and K2 paths, respectively, are enabled. These parameters thus give the user full control of the Loop Filter characteristics.

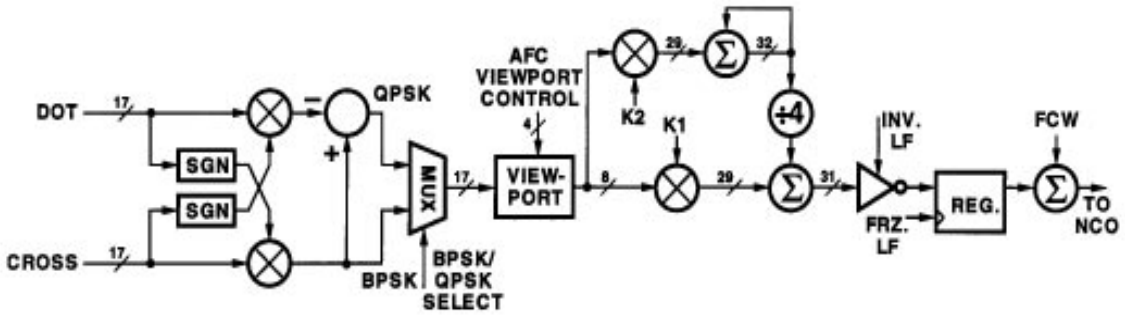

Figure 9. Frequency Discriminator and Loop Filter Detail

$RXIIN_{7-0}$ (Pins 91-98)

Receiver In-Phase Input. RXIIN is an 8-bit input port for in-phase data from external A/D converters. Data may be received in either two's complement or offset binary format as selected by bit 3 of address 01_H. The sampling rate of the RXIIN signals (the I.F. sampling rate of the A/Ds) may be independent of the baseband sampling rate (the Downconverter integrate and dump rate) and the PN chip rate, but must be equal to RXIFCLK and at least two times greater than the baseband sampling rate. Since the baseband sampling rate must be set at twice the PN chip rate, the I.F. sampling rate must thus be at least four times the PN chip rate. Data on the pins is latched and processed by RXIFCLK.

$RXQIN_{7-0}$ (Pins 2-9)

Receiver Quadrature-Phase Input. RXQIN is an 8-bit input port for quadrature-phase data from external A/D converters. Data may be received in either two's complement or offset binary format as selected by bit 3 of address 01_H. As with RXIIN, the sampling rate of the RXQIN signals may be independent of the baseband sampling and PN chip rates in the receiver, but must be at least two times greater than the baseband sample rate (or, equivalently, at least four times greater than the PN chip rate). Data on the pins is latched and processed by RXIFCLK.

FUNCTIONAL BLOCKS (Continued)

Note that if the Z87200 is to be used in Direct I.F. Sampling Mode, then the I.F. signal should be input to the RXIIN input port only. RXQIN must then be held to arithmetic zero according to the chosen ADC format as selected by bit 3 of address 01_H. In other words, to support Direct I.F. Sampling, RXQIN must be tied to a value of 127 or 128 if offset binary input format has been selected or to a value of 0 if two's complement input format has been selected.

RXMSMPL (Pin 84)
Receiver Manual Sample Clock. RXMSMPL enables the user to externally generate (independent of the I.F. sampling clock, RXIFCLK) the baseband sampling clock used for all processing after the digital downconverter, including the dump rate of the Integrate and Dump filters. This feature is useful in cases where a specific baseband sample rate is required that may not be derived by the internal sample rate timing generator which generates clock signals at integer sub-multiples of RXIFCLK. The signal is internally synchronized to RXIFCLK to avoid intrinsic race or hazard timing conditions. There must be at least two cycles of RXIFCLK to every cycle of RXMSMPL, and RXMSMPL should be set to twice the nominal receive PN chip rate.

When bit 0 of address 01_H is set high, a rising edge on RXMSMPL will initiate a baseband sampling clock pulse to the Integrate and Dump filters and subsequent circuitry (e.g., PN Matched Filter, DPSK Demodulator, Power Estimator, etc.). The rising edge of RXMSMPL is synchronized internally so that, on the second rising edge of RXIFCLK that follows the rising edge of RXMSMPL, a pulse is internally generated that clocks the circuitry that follows. On the third rising RXIFCLK edge, the contents of the Integrate and Dump Filters of the Downconverter are transferred to the PN Matched Filter. The extra one RXIFCLK delay before transfer of the contents of the filters enables the internally generated baseband sampling clock to be free of race conditions at the interface between the Downconverter and PN Matched Filter.

RXMDET (Pin 88)
Receiver Manual Detect. RXMDET enables the user to externally generate symbol timing, bypassing and overriding the internal symbol power estimation and tracking circuitry. This function may be useful when the dynamic characteristics of the transmission environment require unusual adjustments to the symbol timing.

When bit 0 of address 30_H is set high (Manual Detect Enable) and when bit 0 of address 31_H is set low, a rising edge of RXMDET will generate a symbol correlation detect pulse. The function can also be performed by means of bit 0 of address 31_H. The RXMDET input and bit 0 of address 31_H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the manual detect function. The rising edge of RXMDET is synchronized internally so that, on the second rising edge of the baseband sampling clock that follows the rising edge of RXMDET, the correlated outputs of the PN Matched Filter I and Q channels will be transferred to the DPSK demodulator.

RXMABRT (Pin 87)
Receiver Manual Abort. RXMABRT enables the user to manually force the Z87200 to cease reception of the current burst of data symbols and prepare for acquisition of a new burst. This function can be used to reset the receiver and prepare to receive a priority transmission signal under precise timing control, giving the user the ability to control the current status of the receiver for reasons of priority, signal integrity, etc.

When bit 0 of address 32_H is set low, a rising edge on RXMABRT will execute the abort function. The function can also be performed under microprocessor control by means of bit 0 of address 32_H. The RXMABRT input and bit 0 of address 32_H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the abort function. The second rising edge of the baseband sampling clock that follows a rising edge of RXMABRT will execute the abort and also clear the symbols-per-burst, samples-per-symbol, and missed-detects-per-burst counters. The counters will be reactivated on the detection of the next burst preamble or by a manual detect signal.

RXIFCLK (Pin 12)
Receiver I.F. Clock. RXIFCLK is the master clock of the NCO and all the receiver blocks. All clocks in the receiver section and the NCO, internal or external, are generated or synchronized internally to the rising edge of RXIFCLK. The frequency of RXIFCLK must be at least four times the PN chip rate of the received signal. When bit 0 of address 01_H is set low, the baseband sampling clock, required to be at twice the nominal PN chip rate, will be derived from RXIFCLK according to the setting of bits 5-0 of address 02_H.

MNCOEN (Pin 86)
Manual NCO Enable. MNCOEN allows the power consumed by the operation of the NCO circuitry to be minimized when the Z87200 is not receiving and not transmitting data. The NCO can also be disabled while the Z87200 is transmitting as long as the Z87200's on-chip BPSK/QPSK modulator is not being used. With the instantaneous acquisition properties of the PN Matched Filter, it is often desirable to shut down the receiver circuitry to reduce power consumption, resuming reception periodically until an Acquisition/Preamble symbol is acquired. Setting MNCOEN low holds the NCO in a reset state; setting MNCOEN high then reactivates the NCO, where it is necessary to then reload the frequency control word into the

NCO. Note that MNCOEN operates independently of MTXEN and MRXEN, where those pins have similar control over the transmit and receive circuitry, respectively.

MNCOEN performs the same function as bit 0 of address 37_H, and these two signals are logically ORed together to form the overall control function. When bit 0 of address 37_H is set low, MNCOEN controls the activity of the NCO circuitry; when MNCOEN is set low, bit 0 of address 37_H controls the activity of the NCO circuitry. When either bit 0 or MNCOEN (whichever is in control, as defined above) goes low, a reset sequence occurs on the following RXIFCLK cycle to effectively disable all of the NCO circuitry, although the user programmable control registers are not affected by this power down sequence.

Upon reactivation (when either MNCOEN or bit 0 of address 37_H return high), the NCO must be reloaded with frequency control information either by means of the MFLD input or by writing 01_H into address 00_H.

MTXEN (Pin 17)

Manual Transmitter Enable. A rising edge on MTXEN causes the transmit sequence to begin, where the Z87200 first transmits a single Acquisition/Preamble symbol followed by data symbols. MTXEN should be set low after the last symbol has been transmitted. When MTXEN is set low, power consumption of the transmitter circuit is minimized. MTXEN operates independently of MRXEN and MNCOEN, where these signals have similar control over the receive and NCO circuitry, respectively.

MTXEN performs the same function as bit 1 of address 37_H. and these two signals are logically ORed together to form the overall control function. When bit 1 of address 37_H is set low, MTXEN controls the activity of the transmitter circuitry, and, when MTXEN is set low, bit 1 of address 37H controls the activity of the transmitter circuitry. A rising edge on either MTXEN or bit 1 (whichever is in control, as defined above) initiates a transmit sequence. A falling edge initiates a reset sequence on the following TXIFCLK cycle to disable all of the transmitter data path, although the user programmable control registers are not affected by the power down sequence.

MRXEN (Pin 10)

Manual Receiver Enable. MRXEN allows power consumption of the Z87200 receiver circuitry to be minimized when the device is not receiving. With the instantaneous acquisition properties of the PN Matched Filter, it is often desirable to shut down the receiver circuitry to reduce power consumption, resuming reception periodically until an Acquisition/Preamble symbol is acquired. Setting MRXEN low reduces the power consumption substantially. When MRXEN is set high, the receiver will automatically power up in acquisition mode regardless of its prior state when it was powered down. MRXEN operates independently of MTXEN and MNCOEN, where these signals have similar control over the transmit and NCO circuitry, respectively.

MRXEN performs the same function as bit 2 of address 37_H, and these two signals are logically ORed together to form the overall control function. When bit 2 of address 37_H is set low, MRXEN controls the activity of the receiver circuitry and, when MRXEN is set low, bit 2 of address 37_H controls the activity of the receiver circuitry. When either MRXEN or bit 2 (whichever is in control, as defined above) goes low, a reset sequence begins on the following RXIFCLK cycle and continues through a total of six RXIFCLK cycles to virtually disable all of the receiver data paths. The user-programmable control registers are not affected by the power-down sequence, with the exception of $RXTEST_{7-0}$ Function Select (address 38_H), which is reset to 0. If the $RXTEST_{7-0}$ bus is being used to read any function other than the PN Matched Filter I and Q inputs, the value required must be rewritten after re-enabling the receiver.

TXIN (Pin 18)

Transmit Input. TXIN supports input of the information data to be transmitted by the Z87200. In BPSK mode, the transmitter requires one bit per symbol period; in QPSK mode, two bits are required per symbol period.

To initiate and enable transmission of the data, the user must raise MTXEN high. Data for transmission is requested with TXBITPLS, where one or two pulses per symbol are generated depending on whether the device is in BPSK or QPSK mode as set by bit 0 of address 40_H. To allow monitoring of the state of the transmitter, the Z87200 will pulse TXACQPLS after the initial Acquisition/Preamble symbol is transmitted; the transmission of each subsequent symbol is indicated by pulses of TXTRKPLS.

If programmed for BPSK mode, data is requested by the Z87200 by a rising edge of output signal TXBITPLS, where TKBITPLS is generated once per symbol, one chip period before the end of the current symbol. At the end of the symbol duration, the TXIN data is latched into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, which latches the TXIN value, and is generated repeatedly at the symbol rate as long as the input signal MTXEN remains high.

In QPSK mode, data is requested by the Z87200 by a rising edge of output signal TXBITPLS, where this signal is generated twice per symbol, first one chip period before the middle of the symbol and then one chip period before the end of the symbol. TXBITPLS requests the data exactly one chip cycle before latching the TXIN data into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, which latches the TXIN value.