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Z87001/Z87L01

ROMLESS SPREAD SPECTRUM CORDLESS PHONE CONTROLLER

FEATURES

Device	ROM * (KWords)	RAM (Words)	I/O Lines	Package Information
Z87001	64	512	32	144-Pin QFP
Z87L01	64	512	32	144-Pin QFP

Note: *Maximum accessible external ROM

- Transceiver/Controller Chip Optimized for Implementation of 900 MHz Spread Spectrum Cordless Telephone
  - Adaptive Frequency Hopping
  - Transmit Power Control
  - Error Control Signaling
  - Handset Power Management
  - Support of 32 kbps ADPCM Speech Coding for High Voice Quality
- DSP Core Acts as Phone Controller
  - Zilog-Provided Embedded Transceiver Software to Control Transceiver Operation and Base Station-Handset Communications Protocol
  - User-Modifiable Software Governs Telephone Features
- Transceiver Circuitry Provides Primary Cordless Phone Communications Functions
  - Digital Downconversion with Automatic Frequency Control (AFC) Loop
  - FSK Demodulator
  - FSK Modulator
  - Symbol Synchronizer
  - Time Division Duplex (TDD) Transmit and Receive Buffers
- On-Chip A/D and D/A to Support 10.7 MHz IF Interface
- Up to 64 Kw of External Program Memory Accessible by the DSP Core
- Bus Interface to Z87010 ADPCM Processor
- Static CMOS for Low Power Consumption
- 3.0V to 3.6V, -20°C to +70°C, Z87L01
  4.5V to 5.5V, -20°C to +70°C, Z87001
- 16.384 MHz Base Clock

GENERAL DESCRIPTION

The Z87001 /Z87L01 FHSS Cordless Telephone Transceiver/Controller is expressly designed to implement a 900 MHz frequency hopping spread spectrum cordless telephone compliant with US FCC regulations for unlicensed operation. The Z87001 and Z87L01 are distinct 5V and 3.3V versions, respectively, of the core device. For the sake of brevity, all subsequent references to the Z87001 in this document also apply to the Z87L01 unless specifically noted.

The Z87001 is the ROMless version of the Z87000 Spread Spectrum Controller IC. Specifically intended to facilitate user specific software development, the Z87001 can access up to 64 kwords of external program ROM.

The Z87001 supports a specific cordless phone system design that uses frequency hopping and digital modulation to provide extended range, high voice quality, and low system costs.

The Z87001 uses a Zilog 16-bit fixed-point two's complement static CMOS Digital Signal Processor core as the phone and RF section controller. The Z87001's DSP core processor further supports control of the RF section's frequency synthesizer for frequency hopping and the generation of the control messages needed to coordinate incorporation of the phone's handset and base station. Additional on-chip transceiver circuitry supports Frequency Shift Keying modulation/demodulation and multiplexing/demulti-

GENERAL DESCRIPTION (Continued)

plexing of the 32 kbps voice data and 4 kbps command data between handset and base station. The Z87001 provides thirty-two I/O pins, including four wake-up inputs and two CPU interrupt inputs. These programmable I/O pins allow a variety of user-determined phone features and board layout configurations. Additionally, the pins may be used so that phone features and interfaces are supported by an optional microcontroller rather than by the Z87001's DSP core.

In combination with an RF section designed according to the system specifications, Zilog's Z87010/Z87L10 ADPCM Processor, a standard 8-bit PCM telephone codec and minimal additional phone circuity, the Z87001 and its embedded software provide a total system solution.

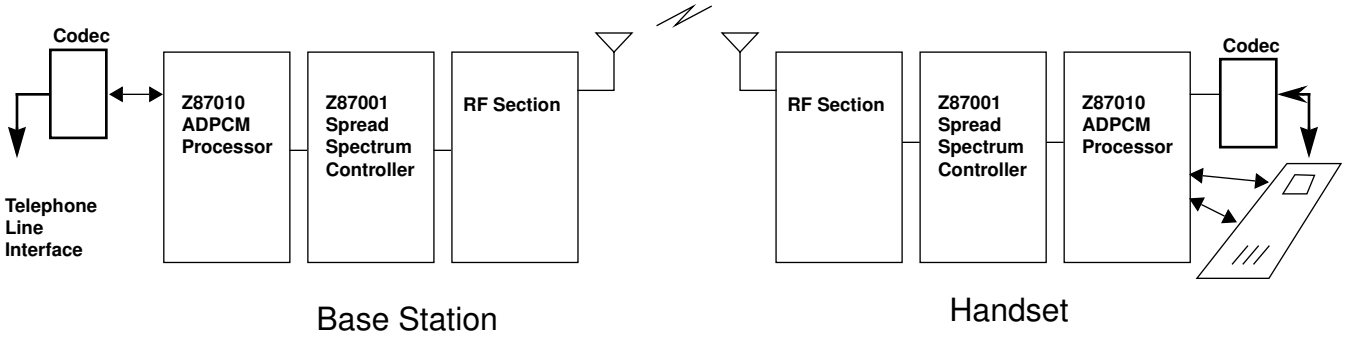


Figure 1. System Block Diagram of a Z87001/Z87010 Based Phone

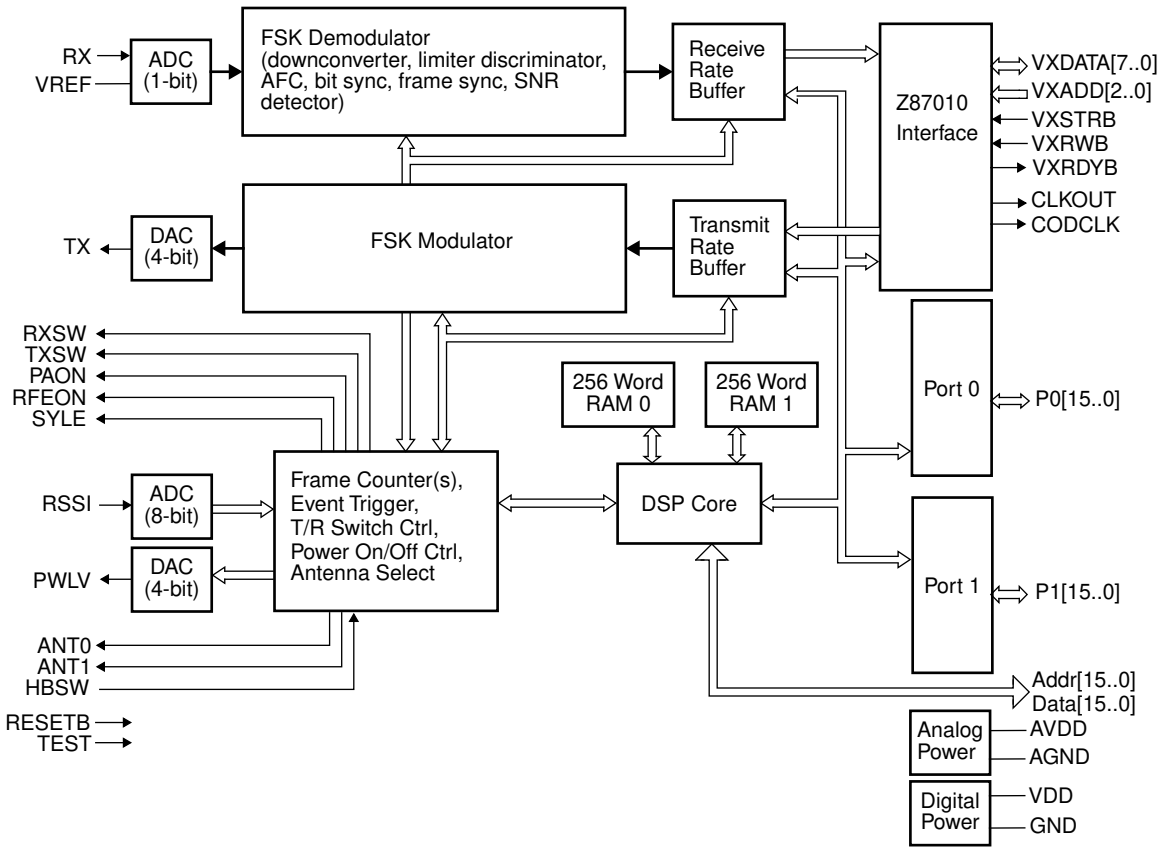


Figure 2. Z87001 Functional Block Diagram

PIN DESCRIPTION

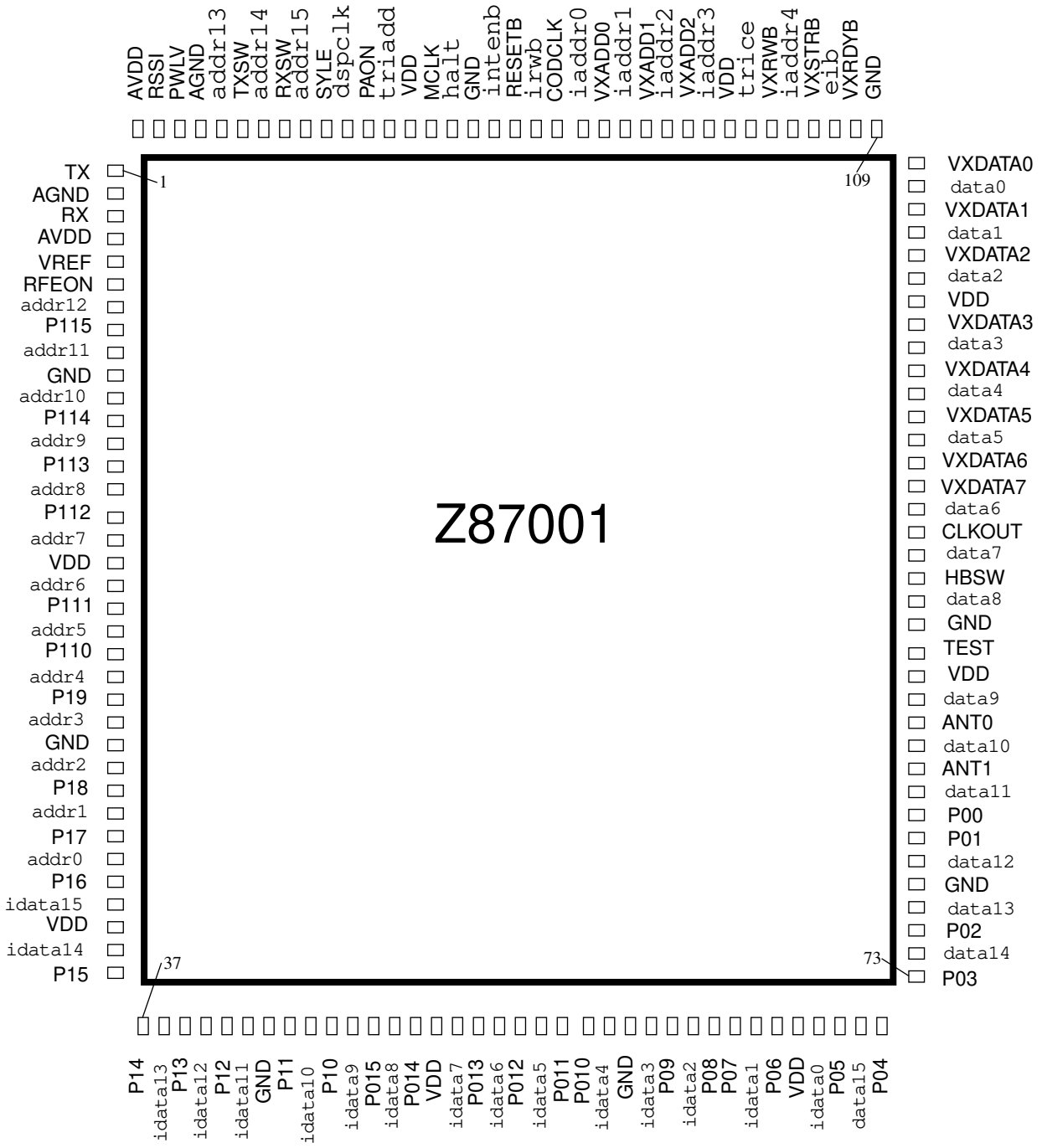


Figure 3. 144 Pin QFP Pin Configuration

Table 1. 144 Pin QFP Pin Configuration

No	Symbol	Function	Direction
1	TX	Analog transmit IF signal	Output
2,141	AGND	Analog ground	–
3	RX	Analog receive IF signal	Input
4,144	AV_{DD}	Analog power supply	–
5	VREF	Analog reference voltage for RX signal	–
6	RFEON	RF on/off control	Output
7,9,11,13,15,17,19, 21,23,25,27,29,31, 136,138,140	addr[15..0]	DSP core program address bus	Output
8,12,14,16,20,22,24, 28,30,32,36,37,39, 41,44,46	P1[15..0]	General-purpose I/O port 1	Input/Output
10,26,43,60,77,88, 109,128	GND	Digital ground	–
18,34,51,68,86,102, 116,131	V_{DD}	Digital power supply	–
33,35,38,40,42,45, 47,49,52,54,56,59, 61,63,66,69	idata[15..0]	DSP core internal data bus	Output
48,50,53,55,57,58, 62,64,65,67,70,72, 73,75,79,80	P0[15..0]	General-purpose I/O port 0	Input/Output
71,74,76,78,81,83, 85,89,91,93,96,98, 100,103,105,107	data[15..0]	DSP core program data bus	Input
82,84	ANT[1..0]	RF antenna diversity control	Output
87	TEST	Test mode select	Input
90	HBSW	Handset/base mode select	Input
92	CLKOUT	Clock, ADPCM processor (16.384 MHz)	Output
94,95,97,99,101, 104,106,108	VXDATA[7..0]	ADPCM processor data bus	Input
110	VXRDYB	ADPCM processor ready	Output
111	eib	External register data strobe	Output
112	VXSTRB	ADPCM processor data strobe	Input
113,117,119,121, 123	iaddr[4..0]	External register address bus	Output
114	VXRWB	ADPCM processor read/write control	Input
115	trice	ROMless mode select	Input
118,120,122	VXADD[2..0]	ADPCM processor address bus	Input
124	CODCLK	Clock to codec (2.048 MHz)	Output
125	irwb	External register read/write control	Output
126	/RESETB	Master reset	Input
127	intenb	Interrupt enable	Input

PIN DESCRIPTION (Continued)

Table 1. 144 Pin QFP Pin Configuration

No	Symbol	Function	Direction
129	halt	Halt/ single step control	Input
130	MCLK	Master clock (16.384 MHz)	Input
132	triadd	Program address bus enable	Input
133	PAON	RF transmit enable	Output
134	dspclk	DSP core clock	Output
135	SYLE	RF synthesizer load enable	Output
137	RXSW	Demodulator “on” indication	Output
139	TXSW	RF receive enable	Output
142	PWLV	RF transmit power level	Input
143	RSSI	RF receive signal strength indicator	Input

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_{DD}, AV_{DD}	DC Supply Voltage(1)	-0.5	7.0	V
V_{IN}	Input Voltage(2)	-0.5	V_{DD} + 0.5	V
V_{OUT}	Output Voltage(3)	-0.5	V_{DD} + 0.5	V
T_A	Operating Temperature	-20	+70	°C
T_{STG}	Storage Temperature	-65	+150	°C

Notes:
1. Voltage on all pins with respect to GND.
2. Voltage on all inputs WRT VDD
3. Voltage on all outputs WRT VDD

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The electrical characteristics listed below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pins. Standard test conditions are as follows:

- 3.0V < V_{DD} < 3.6V (Z87L01)
- 4.5V < V_{DD} < 5.5V (Z87001)
- GND = 0V
- T_A = -20 to +70 °C

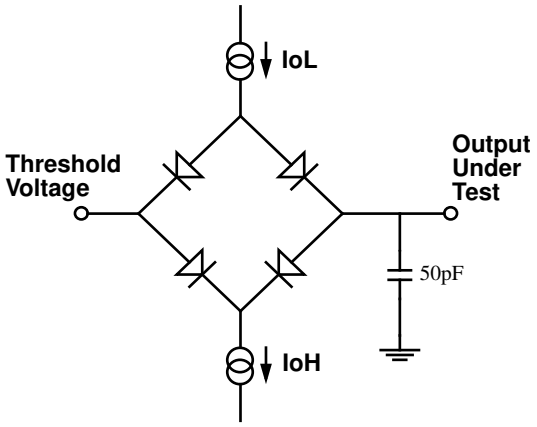


Figure 5. Test Load Diagram

RECOMMENDED OPERATING CONDITIONS

Table 3. 5V ± 0.5V Operation (Z87001)

Symbol	Parameter	Min	Max	Units
V_{DD}, AV_{DD}	Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.0	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	GND -0.3	0.8	V
I_{OH}	Output High Current		-2.0	mA
I_{OHICE}	Output High Current, ICE pins (1)		-0.5	mA
I_{OL1}	Output Low Current		4.0	mA
I_{OL2}	Output Low Current, GPIO (limited usage, 2)		12.0	mA
I_{OLICE}	Output Low Current, ICE pins (1)		0.5	mA
T_A	Operating Temperature	-20	+70	°C

Notes:
1. ICE pins are addr[15..0], iaddr[15..0], idata[15..0], eib and irwb
2. Maximum 3 pins total from P0[15..0] and P1[15..0]

Table 4. 3.3V ± 0.3V Operation (Z87L01)

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply Voltage	3.0	3.6	V
V_{IH}	Input High Voltage	0.7 V_{DD}	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	GND -0.3	0.1 V_{DD}	V
I_{OH}	Output High Current		-1.0	mA
I_{OHICE}	Output High Current, ICE pins (1)		-0.5	mA
I_{OL1}	Output Low Current		2.0	mA
I_{OL2}	Output Low Current, Ports (limited usage, 2)		6.0	mA
I_{OLICE}	Output Low Current, ICE pins (1))		0.5	mA
T_A	Operating Temperature	-20	+70	°C

Notes:
1. ICE pins are addr[15..0], iaddr[15..0], idata[15..0], eib and irwb
2. Maximum 3 pins total from P0[15..0] and P1[15..0]

DC ELECTRICAL CHARACTERISTICS

Conditions for DC characteristics are corresponding operating conditions, and standard test conditions, unless otherwise specified.

Table 5. 5V ± 0.5V Operation (Z87001)

Symbol	Parameter	Test Condition	Min	Max	Units
V_{OH}	Output High Voltage	V_{DD} min, I_{OH} max	2.4		V
V_{OHICE}	Output High Voltage, ICE pins (1)	V_{DD} min, I_{OHICE} max	2.4		V
V_{OL1}	Output Low Voltage	V_{DD} min, I_{OL1} max		0.6	V
V_{OL2}	Output Low Voltage, GPIO (2)	V_{DD} min, I_{OL2} max		1.2	V
V_{OLICE}	Output Low Voltage, ICE pins (1)	V_{DD} min, I_{OLICE} max		0.4	V
I_L	Input Leakage	V_{IN} = 0V, V_{DD}	-2	2	µA
I_{CC}	Supply Current			80	mA
I_{CC2}	Standby Mode Current (3)			4	mA

Notes:
1. ICE pins are addr[15..0], iaddr[15..0], idata[15..0], eib and irwb
2. Maximum 3 pins total from P0[15..0] and P1[15..0]
3. 2.3 mA typical at 25°C, 5 volts.

Table 6. 3.3V ± 0.3V Operation (Z87L01)

Symbol	Parameter	Test Condition	Min	Max	Units
V_{OH}	Output High Voltage	V_{DD} min, I_{OH} max	1.6		V
V_{OHICE}	Output High Voltage, ICE pins (1)	V_{DD} min, I_{OHICE} max	1.6		V
V_{OL1}	Output Low Voltage	V_{DD} min, I_{OL1} max		0.4	V
V_{OL2}	Output Low Voltage, Ports(2)	V_{DD} min, I_{OL2} max		1.2	V
V_{OLICE}	Output Low Voltage, ICE pins (1)	V_{DD} min, I_{OLICE} max		0.4	V
I_L	Input Leakage	V_{IN} = 0V, V_{DD}	-2	2	µA
I_{CC}	Supply Current			55	mA
I_{CC2}	Standby Mode Current(2)		1.4		mA

Notes:
1. ICE pins are addr[15..0], iaddr[15..0], idata[15..0], eib and irwb
2. Maximum 3 pins total from P0[15..0] and P1[15..0]
3. 1.6 mA typical at 25°C, 3.3 volts.

ANALOG CHARACTERISTICS

Table 7. 1-Bit ADC (Temperature: -20/+70°C)

Parameter	Minimum	Typical	Maximum	Units
Resolution	-	1	-	bit
Power dissipation	0.54 (70°c)	1.0 (40°c)	2.75 (-20°c)	mW
Power dissipation, Stop mode	0.06 (70°c)	0.2 (40°c)	1.1 (-20°c)	mW
Sample frequency	-	8.192	-	MHz
Sample window(1)	29	31	33	ns
Bandwidth	-	60	-	MHz
Supply Range(=AV_{DD})				
Z87L01	3.0		3.6	V
Z87001	4.5		5.5	V
Acquisition time	2	3	8	ns
Settling time	8	10	18	ns
Conversion time	4	6	18	ns
Aperture delay	2	3	8.5	ns
Aperture uncertainty(2)	-	-	0.5	ns
Input voltage range (p-p)	800	1000	1200	mV
Reference voltage				
Z87L01	1.7 (AV_{DD}= 3V)	1.9 (AV_{DD}= 3.3V)	2.1 (AV_{DD}= 3.6V)	V
Z87001	2.7 (AV_{DD}=4.5V)	3.0 (AV_{DD}= 5V)	3.3 (AV_{DD}= 5.5V)	V
Input resistance	10	18	25	KOhm
Input capacitance	-	10	-	pF

Notes:
Window of time while input signal is applied to sampling capacitor; see next figure.
Uncertainty in sampling time due to random variations such as thermal noise.

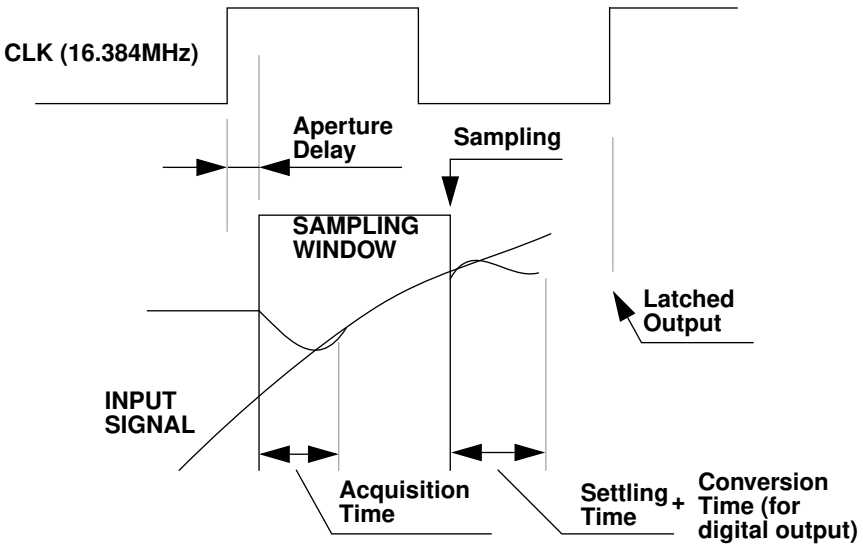


Figure 6. 1-Bit ADC Definition of Terms

Table 8. 8-bit ADC (Temperature -20/+70°C)

Parameter	Minimum	Typical	Maximum	Units
Resolution	-	6	-	bit
Integral non-linearity	-	0.5	1	LSB
Differential non-linearity	-	-	0.5	LSB
Power Dissipation (peak)		35	70	mW
Sample window	5	-	120	ns
Bandwidth	-	-	2	Msps
Supply Range (=AV_{DD})				
Z87L01	3.0	3.3	3.6	V
Z87001	4.5	5.0	5.5	V
Input voltage range		0-AV_{DD}		V
Conversion time	0.5	-	-	µs
Aperture delay	2	3	8.5	ns
Aperture uncertainty	-	-	1	ns
Input resistance	-	25	-	Kohm
Input capacitance	-	10	-	pF

Notes:
1. 8-bit ADC only tested for 6-bit resolution.

Table 9. 4-bit DAC (Temperature: -20/+70°C)

Parameter	Minimum	Typical	Maximum	Units
Resolution	-	4	-	bit
Integral non-linearity	-	0.25	0.5	LSB
Differential non-linearity	-	0.25	1	LSB
Settling time (1/2 LSB)	-	-	22.5	ns
Zero error at 25°C	-	1	2	mV
Conversion time (input change to output change)	14	19	76	ns
Power dissipation, 25 pF load	1.2 (70°c)	20 (40°c)	24.1 (-20°c)	mW
Power dissipation, 25 pF load, Stop mode	0.18 (70°c)	1.0 (40°c)	1.1 (-20°c)	mW
Conversion time (input change to output change)	14.5	19.1	75.8	ns
Rise time (full swing)	11	15	71	ns
Output slew rate	8	67	96	V/µs
Output voltage range	-	0.2 AV_{DD} to 0.6AV_{DD}	-	V
Supply Range (=AV_{DD})				
Z87L01	3.0	3.3	3.6	V
Z87001	4.5	5.0	5.5	V
Output load resistance		330		Ohm
Output load capacitance	-	25	-	pF

INPUT/OUTPUT PIN CHARACTERISTICS

All digital pins (all pins except V_{DD}, AV_{DD}, GND, AGND, V_{REF}, RX, TX, RSSI and PWLV) have an internal capacitance of 5 pF.

The RX analog input pin has an input capacitance of 10 pF.

The RSSI analog input pin has an input capacitance of 10 pF.

AC ELECTRICAL CHARACTERISTICS

Clocks, Reset and RF Interface

Table 10. Clocks, Reset and RF Interface

No.	Symbol	Parameter	Min	Max	Units
1	TpC	MCLK input clock period (1)	61	61	ns
2	TwC	MCLK input clock pulse width	20	40	ns
3	TrC, TfC	MCLK input clock rise/fall time		15	ns
4	TrCC, TfCC	CLKOUT output clock rise/fall time	2	6	ns
5	TrCO, TfCO	CODCLK output clock rise/fall time	2	6	ns
6	TwR	RESETB input low width	18		TpC
7	TrRF, TfRF	RF output controls rise/fall time (2)	2	6	ns

Notes:
1. MCLK is 16.384 MHz ± 25 ppm
2. RF Controls are PAON, TXSW, RFEON, SYLE.

ADPCM Processor Interface

The Z87001 is a peripheral device for the ADPCM Processor. The interface from the Z87001 perspective is composed of an input address bus, a bidirectional data bus, strobe and read/write input control signals and a ready/wait output control signal.

READ CYCLES refer to data transfers from the Z87001 to the ADPCM Processor.

WRITE CYCLES refer to data transfers from the ADPCM Processor to the Z87001.

Table 11. Read Cycles

Signal Name	Function	Direction
VXADD[2..0]	Address Bus	ADPCM Proc. to Z87001
VXDATA[7..0]	Data Bus	Bidirectional
VXSTRB	Strobe Control Signal	ADPCM Proc. to Z87001
VXRWB	Read/Write Control Signal	ADPCM Proc. to Z87001
VXRDYB	Ready Control Signal	Z87001 to ADPCM Proc.

Table 12. Write Cycles

No.	Symbol	Parameter	Min	Max	Units
8	TsAS	Address, Read/Write setup time before Strobe falls	10		ns
9	ThSA	Address, Read/Write hold time after Strobe rises	3		ns
10	TaDrS	Data read access time after Strobe falls		30 (1)	ns
11	ThDrS	Data read hold time after Strobe rises	8.5	40 (2)	ns
12	TwS	Strobe pulse width	20		
13	TsDwS	Data write setup time before Strobe rises	10		ns
14	ThDwS	Data write hold time after Strobe rises	3		ns
15	TaDrRY	Data read valid before Ready falls	22		ns
16	TdSRY	Strobe high after Ready falls	0		ns

Notes:
1. Requires wait state on ADPCM Processor read cycles
2. Requires no write cycle directly following read cycle on ADPCM Processor

AC TIMING DIAGRAMS

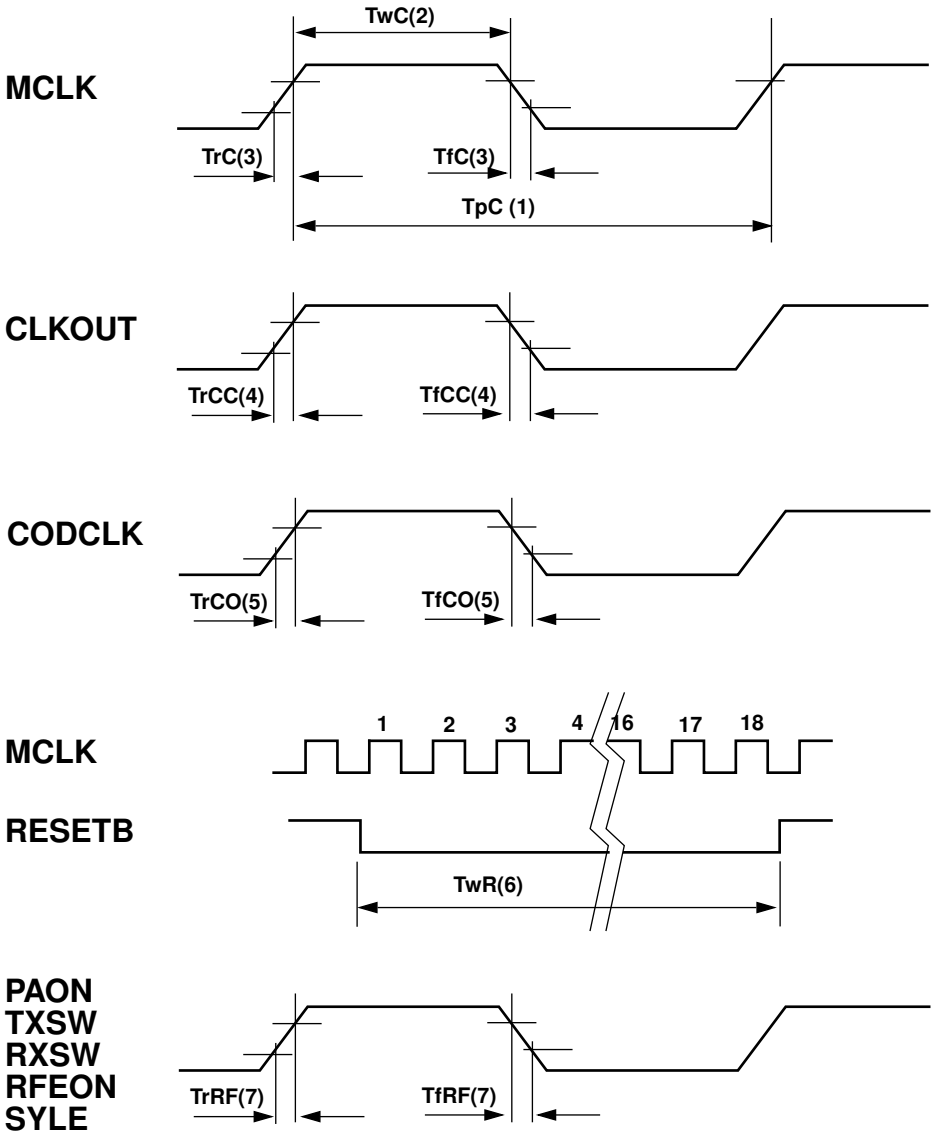


Figure 7. Transceiver Output Signal

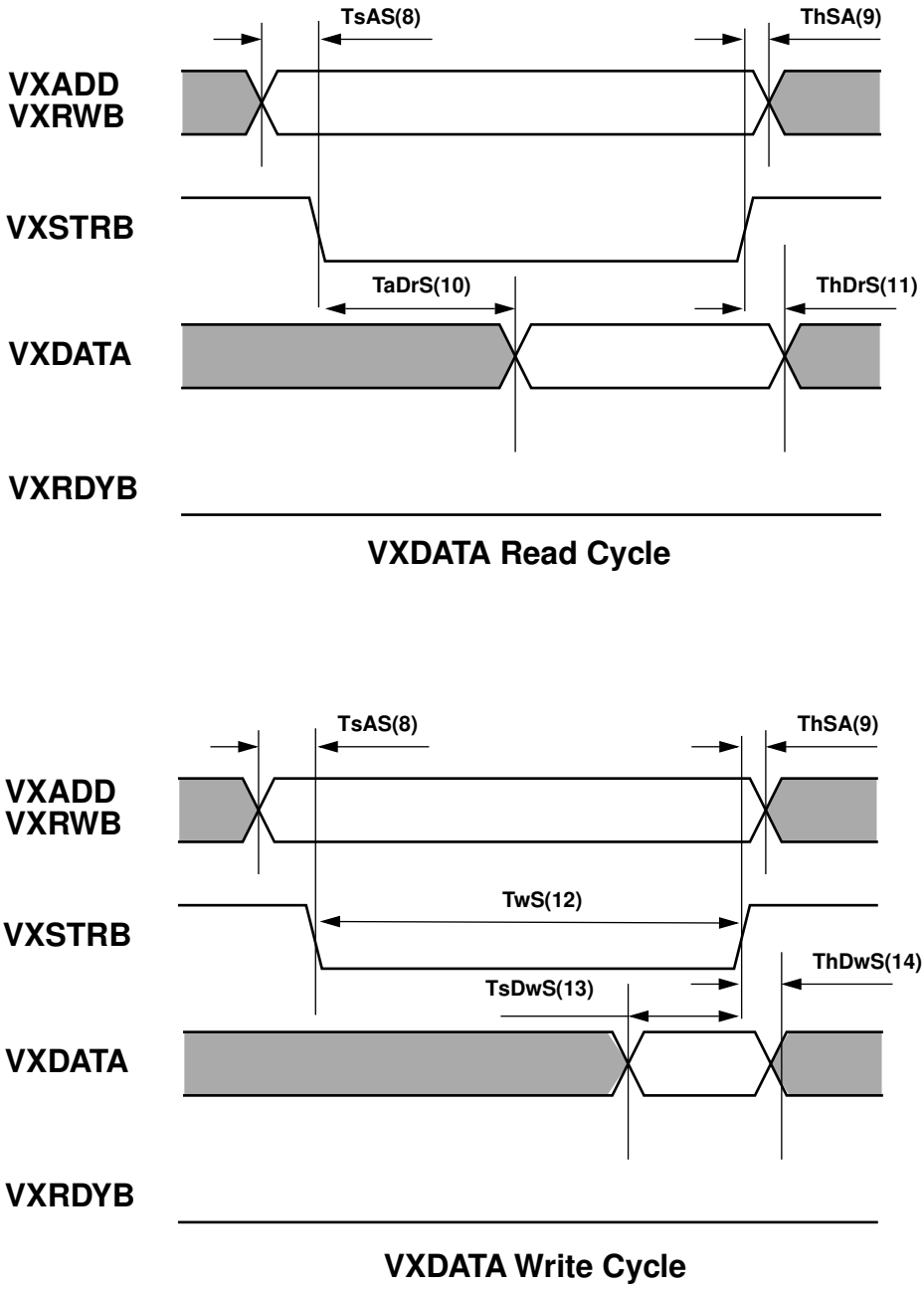
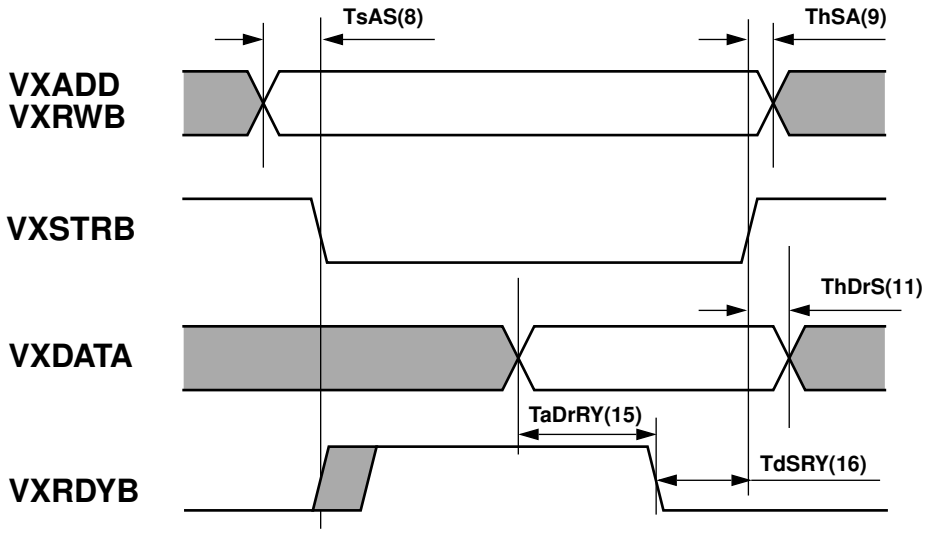
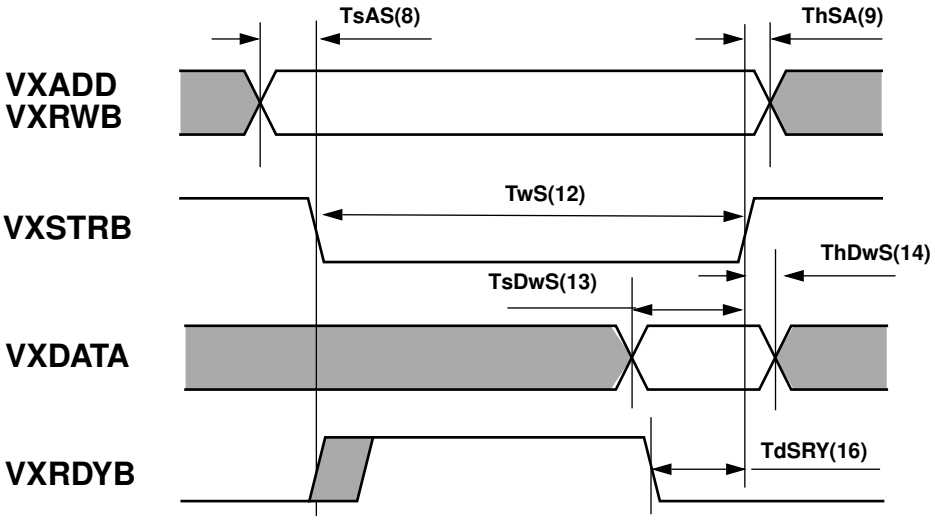


Figure 8. Read/Write Cycle TImings



VXDATA Read Cycle with Wait State



VXDATA Write Cycle with Wait State

Figure 9. Read/Write Cycle Timing with Wait StatE

PIN FUNCTIONS

V_{DD}. Digital power supply.

GND. Digital ground.

AV_{DD}. Analog power supply.

AGND. Analog ground.

V_{REF} (analog reference)**.** This signal is the reference voltage used by the high speed analog comparator to sample the RX input signal.

RX (analog input)**.** This is the RX IF receive signal from the RF module, input to the analog comparator and FSK demodulator. It is internally biased to the V_{REF} DC voltage. The IF signal from the RF module should be AC coupled to the RX pin.

TX (analog output)**.** This is the IF transmit signal to the RF module, output from the FSK modulator and transmit 4-bit D/A converter.

RXSW (output; active high or low programmable)**.** This pin reflects the programming of the demodulator turn-on time.

TXSW (output; active high or low programmable)**.** Control for the receive switch on the RF module. Active during receive periods.

PAON (output; active high or low programmable)**.** Control for the transmit switch on the RF module. Active during transmit periods.

RFEON (output; active high or low programmable)**.** On/off control for the RF module. Active (on) during wake periods. Inactive (off) during sleep periods on the handset.

RSSI (analog input)**.** Receive signal strength indicator from RF module, input to the RSSI 8-bit ADC.

PWLV (analog output)**.** Power level control for RF module, output from the transmit power 4-bit DAC.

SYLE (output)**.** RF synthesizer load enable: latches new frequency hopping control word of external RF synthesizer. Programmable polarity.

ANT[1..0] (output)**.** Control for optional antenna diversity on the RF module.

MCLK (input)**.** Master clock input.

CLKOUT (output)**.** Clock output for external ADPCM processor.

CODCLK (output)**.** Clock output for external voice codec.

/**RESETB** (input, active low). Reset signal.

VXADD[2..0] (input)**.** Address bus controlled by external ADPCM processor. The Z87001 acts as peripheral of the Z87010 ADPCM processor.

VXDATA[7..0](input/output)**.** Read/write data bus controlled by external Z87010 ADPCM processor.

VXSTRB (input)**.** Data strobe signal for the VXDATA bus, controlled by external Z87010.

VXRWB (input)**.** Read/write control for the VXDATA bus, controlled by external Z87010.

VXRDYB (output, active low)**.** Ready control for the VXDATA bus. This signal is driven high (de-asserted) by the Z87001 to insert wait states in the Z87010 ADPCM processor accesses.

TEST (input, active high)**.** Main test mode control. Must be set to GND.

HBSW (input with internal pull-up)**.** Control for handset/base configuration. Must be driven high or not connected for handset, low for base.

P0[15..0] (input/output)**.** General-purpose I/O port. Direction is bit-programmable. Pins P0[3..0],when configured in input mode, can also be individually programmed as wake-up pins for the Z87001 (wake-up active low; signal internally debounced and synchronized to the bit clock).

P0 0	WAKEUP0
P0 1	WAKEUP1
P0 2	WAKEUP2
P0 3	WAKEUP3

P1[15..0] (input/output).General-purpose I/O port. Direction is bit-programmable. Pins P114 and P115, when configured in input mode, also behave as individually maskable interrupt pins for the core processor (positive edge-triggered).

P1 14	INT0
P1 15	INT2

FUNCTIONAL DESCRIPTION

The functional partitioning of the Z87001 is shown in Figure 2. The chip consists of a receiver, a transmitter, and several additional functional blocks.The receiver consists of the following blocks:

- Receive 1-bit ADC
- Demodulator, including:
  - IF Downconverter
  - AFC (Automatic Frequency Control)
  - Limiter-Discriminator
  - Matched Filter
  - Bit Synchronizer
  - Bit Inversion
  - Frame Synchronizer (unique word detector)
  - SNR Detector
- Receive Frame Timing Counter
- Receive Buffer and Voice Interface

The Transmitter Consists of the Following Blocks:

- Transmit Buffer and Voice Interface
- Transmit Frame Timing Counter (used on base station only)
- Modulator, including:
  - NCO
  - Bit Inversion
- Transmit 4-Bit DAC

In Addition, there are the following Shared Blocks.

- Event Trigger Block, Controlling:
  - Transmit/Receive Switch
  - Power On/Off Switches (Modulator, Demodulator, RF Module)
  - Antenna Switch Control (used on Base Station only for Antenna Diversity)
- 4-Bit DAC for Setting Transmit Power Level
- 8-Bit ADC for Sampling the Received Signal Strength Indicator (RSSI)
- DSP Core Processor
- Two 16-Bit General-Purpose I/O Ports
- Z87010 ADPCM Processor Interface

Basic Operation

The transmitter and receiver operate in time-division duplex (TDD): handset and base station transmit and receive alternately. The TDD duty cycle lasts 4 ms and consists of the following events:

- At the beginning of the cycle, the frequency is changed (hopping)
- The base station transmits a frame of 144 bits while the handset receives
- The handset then transmits a frame of 148 bits while the base receives.

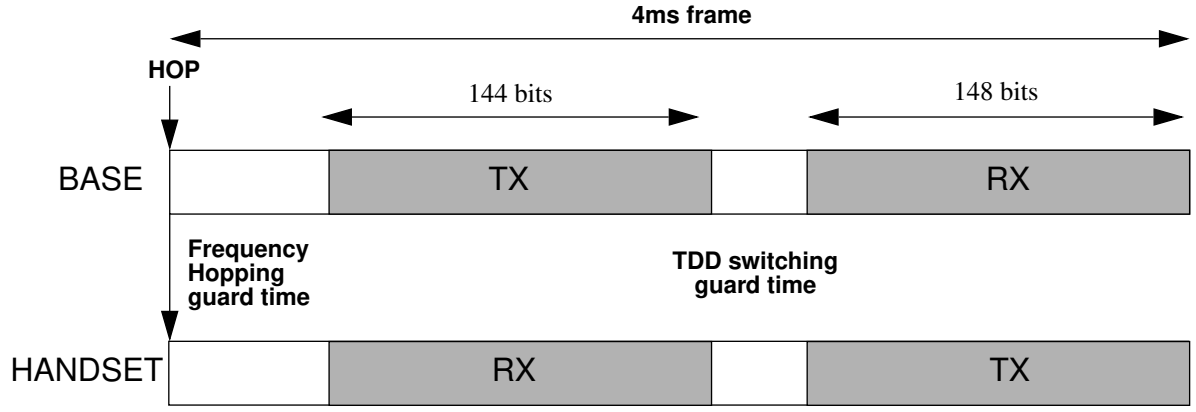


Figure 1. Basic Time Duplex Timing

Receive 1-Bit ADC

The incoming receive signal at the RX analog input pin is sampled by a 1-bit analog-to-digital converter at 8.192 MHz.

The receive signal is FSK-modulated (Frequency Shift Keying) with a carrier frequency of 10.7 MHz (Intermediate Frequency, or IF). The instantaneous frequency varies between 10.7 MHz plus or minus 32.58 kHz. Since the data rate is 93.09 kbps, there are 88 samples per data bit. This oversampled data is further processed by the demodulator to retrieve the baseband information.

The 1-bit converter is implemented with a fast comparator, which determines whether the RX signal is larger or smaller than a reference signal (VREF). The Z87001 internally generates the DC level of both VREF and RX input pins. The received signal at 10.7 MHz should thus be AC coupled to the RX pin via a coupling capacitor. To ensure accurate operation of the converter, the user should also attach to the VREF pin a network whose impedance matches the DC impedance seen by the RX pin.

Demodulator

The demodulator includes a two-stage IF downconverter that brings the sampled receive signal to baseband.

The narrow-band 10.7 MHz receive signal, sampled at 8.192 MHz by the 1-bit ADC, provides a 2.508 MHz useful image. The first local oscillator used to downconvert this IF signal is obtained from a Numerically Controlled Oscillator (NCO) internal to the Z87001, at the nominal frequency of 460 kHz. The resulting signal is thus at 2.048 MHz (= 2.508 MHz - 460 kHz). A second downconversion by a 2.048 MHz signal brings the receive signal to baseband.

The exact frequency of the 460 kHz NCO is slightly adjusted by the Automatic Frequency Control (AFC) loop for exact downconversion of the end signal to the zero frequency. The AFC circuit detects any DC component in the output of the limiter-discriminator (see below) when receiving a known sequence of data (preamble). This DC component is called the “frequency bias”. The bias estimate out of the AFC can be read by the DSP processor on every frame and subsequently filtered. The processor then adds or subtract this filtered bias to/from the NCO control word to correct the NCO frequency output.

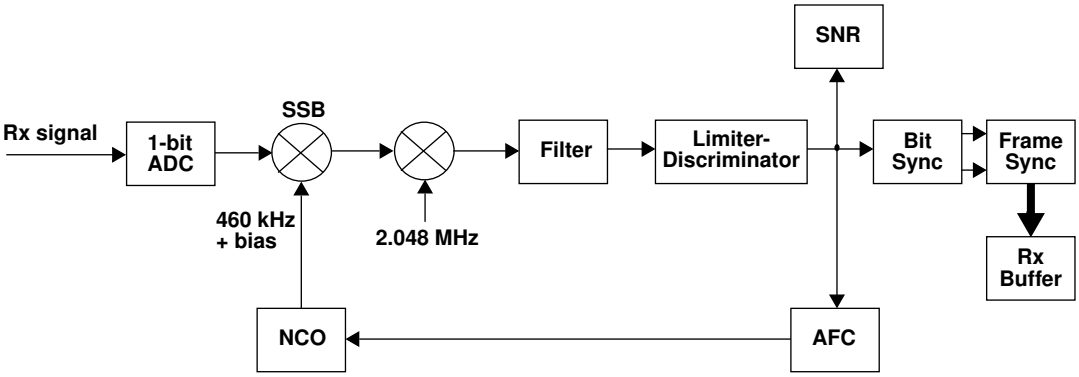


Figure 2. Demodulator Block Diagram

The main element of the demodulator is its limiter-discriminator. The limiter-discriminator detects the frequency variations (ideally up to ± 32.58 kHz) and converts them to “0” or “1” information bits. First, the data is processed through low-pass filters to eliminate high frequency spurious components introduced by the 1-bit ADC. The resulting signal is then differentiated and fed to a matched filter. In the matched filter, an integrate-and-dump operation is performed to extract the digital information from its background noise.

The symbol clock is provided by the bit synchronizer. The bit synchronizer circuit detects 0-to-1 and 1-to-0 transitions in the incoming data stream in order to synchronize a digital phase-lock loop (DPLL). The PLL output is the recovered bit clock, used to time the receiver on the base station, and both receiver and transmitter on the handset.

To ensure enough transitions in the voice data stream, a pseudo-random bit inversion operation is performed on the outgoing voice data. The inversion is then reversed on the demodulated data.

Since the data is packed in frames sent alternately from base and handset every 4 ms (TDD), additional synchronization means are necessary. This is realized in a frame

FUNCTIONAL DESCRIPTION (Continued)

synchronizer, based on detection of a “unique word” following the preamble.

The receiver also features a signal-to-noise ratio detector, which allows the DSP software to detect noisy channels and eliminate them from the frequency hopping cycle. The SNR information is also used by the Z87001 software as a measure the current range between handset and base station. This information allows the adaptive power control algorithm to provide sufficient output power to the RF transmitter.

Receive Frame Counter

The receive frame counter is responsible to keep track of time within the frame. It is initialized by the frame synchronizer logic on detection of the unique word. It is then clocked by the recovered bit clock from the bit synchronizer.

On the base station, the receive frame counter is used as time base for the receiver. On the handset, it is used as time base for both receiver and transmitter.

Receive Rate Buffer and Voice Interface

The voice signal is generated at the fixed rate of 32 kips by the Z87010 processor, and transmitted/received in bursts of 93.09 kips across the air. Data buffers in the transmitter and receiver are thus necessary to absorb the rate differences over time. These buffers are called “rate buffers”. They can store up to 144 data bits and are organized as an array of 36 4-bit nibbles.

The receive rate buffer stores the received data from the demodulator. Incoming bits are arranged in 4-bit nibbles and transferred to successive locations of the rate buffer. When the last location is reached, transfers resume from the beginning (circular buffer). The system design guarantees that no buffer overrun nor enduring can occur.

The receive rate buffer can be read by the DSP core processor of the Z87001 or by the Z87010 chip. On the Z87001 side, the buffer can be read as a random-access memory: the processor writes the nibble address in an address register and reads the 4-bit data from a data register. On the Z87010 side, a voice processor interface logic handles the addressing to automatically present the successive voice nibbles to the Z87010 in the order they were received.

Transmit Rate Buffer and Voice Interface

The transmit rate buffer stores the data to be modulated. The data is sourced from the Z87010 or the Z87001 core processor. As for the receive rate buffer, the Z87010 sees a unique pipe to write to, while the Z87001 DSP core accesses the rate buffer as random-access memory. The modulator reads from the rate buffer as from a circular buffer.

Transmit Frame Timing Counter

On the handset, transmission does not start until the receiver has synchronized itself to the signal received from the base station. The transmission timing is based on the recovered clock. No additional counter is necessary.

On the base station, the situation is different. Transmission timing is based on a local clock, while the reception’s timing is based on the clock recovered from the incoming received signal. Two counters, respectively clocked by local and recovered clocks, are necessary to track the transmit and receive signals.

Note that the receive clock on the base station tracks the handset’s transmit clock, which is also the handset’s receive clock and tracks the transmit clock of the base station. As a result, receive and transmit clocks of the base station have exactly the same frequency; only their phases differ.

Modulator

The modulator consists of a numerically controlled oscillator (NCO) which generates an FSK (Frequency Shift Keying) signal at the carrier frequency of 2.508 MHz. The carrier frequency is shifted plus or minus 32.58 kHz for a “1” or a “0” data bit. To facilitate conformance to FCC regulations, the transitions from “1” to “0” or vice-versa are smoothed in order to decrease the amplitude of the side lobes of the transmit signal. In practice, the jump from one frequency to the next is performed in several smaller steps.

The carrier frequency is adjustable by the DSP core processor in order to provide additional frequency adjustment between base and handset. This is provided in case of a frequency offset too large for possible correction by the AFC.

The modulator also includes bit inversion logic as discussed in the receiver section.

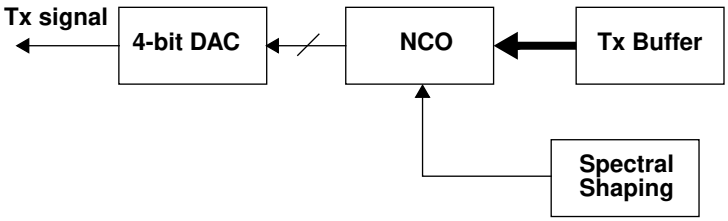


Figure 3. Modulator Block Diagram

Transmit 4-Bit DAC

The transmit DAC clocks one new NCO value out of the Z87001 every 8.192 MHz period. Only the 10.7 MHz alias frequency component of the transmit signal (2.508 + 8.192 MHz image) is filtered, amplified and upconverted to the 900 MHz ISM band by the companion RF module.

Event Trigger Block

The event trigger block is responsible for scheduling the different events happening at the bit and frame levels. The event trigger block receives input from the frame counters as well as the register interface of the DSP core processor.

The event trigger schedules the following events:

- Start of the 4 ms frame: a synthesizer load enable pulse is issued on the SYLE pin
- Power-up of the modulator section and transmission of the frame on handset and base station
- Use of the bit inversion as function of mode
- Power-up of the demodulator section and reception of the frame on handset and base station
- Control of PAON and TXSW output pins, to be used as TDD control signals for the T/R switch as well as the transmitter and receiver chains on the RF module
- Control of RFEON pin, to be used as general on/off switch on the RF module
- Control of the Z87001 sleep mode

4-Bit DAC for Setting Transmit Power Level

In order to save battery life, the Z87001 only transmits the amount of RF power needed to reach the remote receiver with a sufficient SNR margin. The on-board transmit power 4-bit DAC provides 4 different voltage levels to the power amplifier in the RF module for that purpose. This DAC is directly controlled by the Z87001 software through an output register.

8-Bit ADC for Sampling the Received Signal Strength Indicator (RSSI)

RSSI information is typically generated from the last stage of the RF receiver. The RSSI is sampled once per frame by the 8-bit ADC and used by the Z87001 software to compute the necessary Transmit Power Level voltages.

DSP Core Processor

A DSP core processor constitutes the heart of the Z87001. The DSP runs the application software which performs the following functions:

- Register initialization
- Implementation of high-level phone features; control of phone user interface (keypad, Led, etc.)
- Control of the Z87010 ADPCM Processor
- Control of the phone line interface
- Ring detection by DSP processing
- Communication protocol between handset and base station supporting voice and signalling channels
- Control of the RF synthesizer and adaptive frequency hopping algorithm
- Control of the RF power and adaptive power algorithm
- Control of the demodulator (bit synchronizer loop filter, AFC bias estimate filtering)
- Control of the modulator (carrier frequency) and adaptive frequency alignment
- Signalling between base and handset to support above features

FUNCTIONAL DESCRIPTION (Continued)

The DSP core is characterized by an efficient hardware architecture that allows fast arithmetic operations such as multiplication, addition, subtraction and multiply-accumulate of two 16-bit operands. Most instructions are executed in one clock cycle.

The DSP core is operated at the internal speed of 8.192 MHz. It has an internal RAM memory of 512 16-bit words divided in two banks. Six register pointers provide circular buffering capabilities and dual operand fetching. Three vectored interrupts are complemented by a six-level stack. One interrupt is used by the transceiver, while the two remaining vectors are mapped into port P1. In the phone system, one of these interrupts is customarily reserved for the Z87010 ADPCM Processor. The other interrupt can be used for custom purposes.

The Z87001 may access up to 64K 16 bit words of external ROM including 4 words for interrupt and reset vectors. The ROM is mapped at addresses 0000h to 3FFFh, as shown in Figure 13.

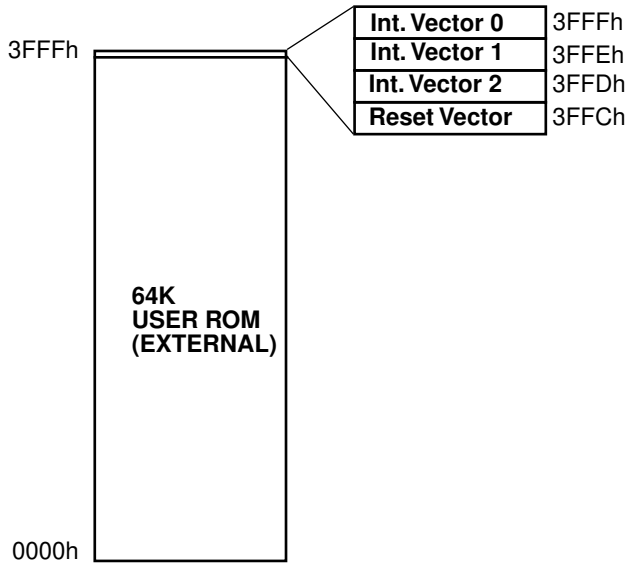


Figure 4. ROM Mapping

Two 16-Bit General-Purpose I/O Ports

Two 16-bit general-purpose I/O ports are directly accessible by the DSP core. These input and output pins are typically used for:

- Implementation of the phone's user interface (keypad, LED, optional display, etc.)
- Control of phone line interface (on/off hook, ring detect)
- Control of battery charging and detection of low battery conditions
- Implementation of additional features for customizing of the phone

Z87010 Interface

In addition to providing clock signals to the Z87010 processor, the Z87001 interfaces to the Z87010 through two different paths:

- A command/status interface
- A data interface

The command/status interface consists of two dual-port registers accessible by both Z87001 and Z87010 DSP core processors. On the Z87001 side, the registers are mapped into the DSP core processor's register interface. To allow access by the Z87010, the internal command/status registers can also be decoded on the pinto of the Z87001. Arbitration logic resolves access contentions.

The data interface allows the Z87010 processor direct access to the Z87001's receive and transmit rate buffers. The rate buffers are decoded on the pin to of the Z87001, and dedicated voice processor interface logic handles the addressing within the rate buffers.

The physical interface between Z87001 and Z87010 consists of an 8-bit data bus, a 3-bit address bus and control signals, as summarized in the following:

VXDATA[7.0]	Data bus
VXADD[2.0]	Address bus
VXSTRB	Data Strobe
VXRWB	Read/Write Control
VXRDYB	Read Control

This bus is controlled by the Z87010. Although in the system the Z87010 is enslaved to the Z87001 master, at the physical level the Z87001 acts as a peripheral of the Z87010.

The mapping of the command status and data interfaces from the Z87010 side is given below.

Interface	Address (VXADD [2.0])	Read /Write	Data (VXDATA[7.0])
Transmit rate buffer	1	W	----3210
Receive rate buffer	1	R	----3210
Command	0	R	76543210
Status	0	W	76543210

OPERATION

Automatic Frequency Control Loop (Receiver) and Modulator

AFC Loop

The AFC loop consists of a bias estimator block, which determines frequency offsets in the incoming signal, an adder, to add this bias to the 460 kHz frequency control word driving the NCO, and various interface points to the DSP core processor. In particular, the DSP can read the bias estimate data and substitute its own calculated bias value to the NCO.

The bias estimator accumulates the discriminator output values (image of instantaneous frequency) that exceed a programmable threshold (BIAS_THRESHOLD). The processor can freeze the bias calculation any time by resetting the BIAS_ENABLE control bit.

The accumulated bias, available in BIAS_ERROR_DATA, can be used directly to correct the NCO frequency. Alternately, the estimated bias can be read by the DSP, further processed, and written to the CORE_BIAS_DATA field. The DSP controls which value is used by setting the USE_CORE_BIAS field. The selected value is added to the 460 kHz signal which downconverts the receive IF signal.

The CORE_BIAS_DATA and BIAS_ERROR_DATA are two's complement numbers in units of 125 Hz.

In addition to correcting the difference in clock frequencies on the receiver using the AFC loop, a Z87001-base system can also modify the frequency of the remote transmit IF signals. The software has access to this frequency through the MOD_FREQ register fields.

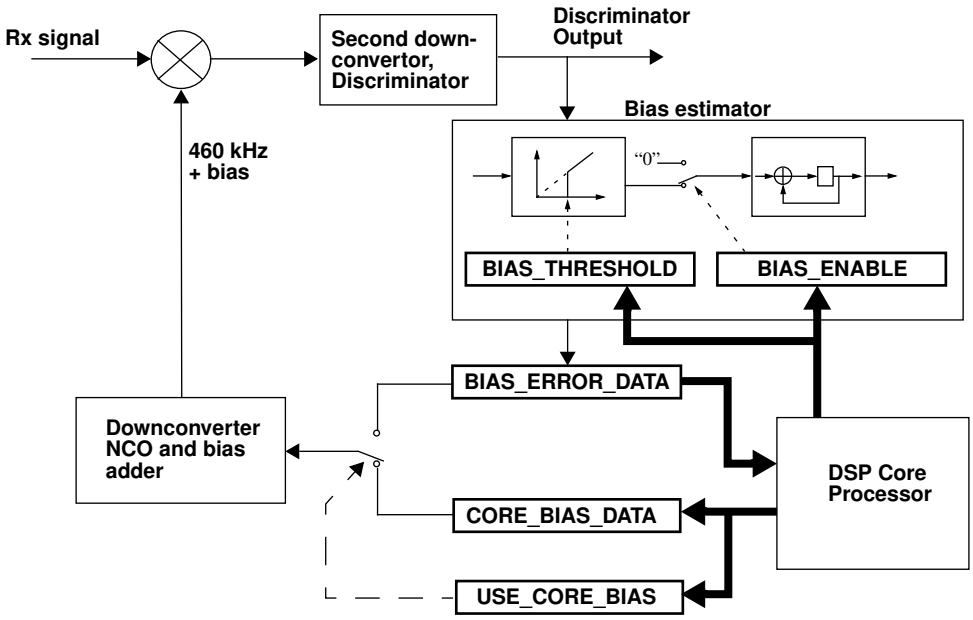


Figure 5. AFC Loop and Processor Control

OPERATION (Continued)

Modulator Control

The MOD_FREQ fields specify the carrier center frequency (should be programmed to 2.508 MHz) and deviation for the FSK signal (should be programmed to ± 32.58 kHz). In addition, wave shaping is performed on bit transitions, in order to satisfy FCC regulations. Up to four different intermediate deviation values are programmable for each of the two FSK states. The MOD_FREQ fields are programmable in units of 62.5 Hz.

Table 1. AFC and Modulator Control Fields

Field	Register	Bank	EXT
BIAS_THRESHOLD	CONFIG1	3	EXT0
BIAS_ENABLE	SSPSTATE	3	EXT2
BIAS_ERROR_DATA	BIAS_ERROR	2	EXT2
CORE_BIAS_DATA	CORE_BIAS	2	EXT4

Bit Synchronizer

The bit synchronizer circuit is an implementation of the Data-Transition-Tracking Loop (DTTL), best described in "Telecommunications Systems Engineering", by W. Lindsey and M. Simon (Dover 1973; oh. 9 p. 442). Its operation is summarized in the following block diagram.

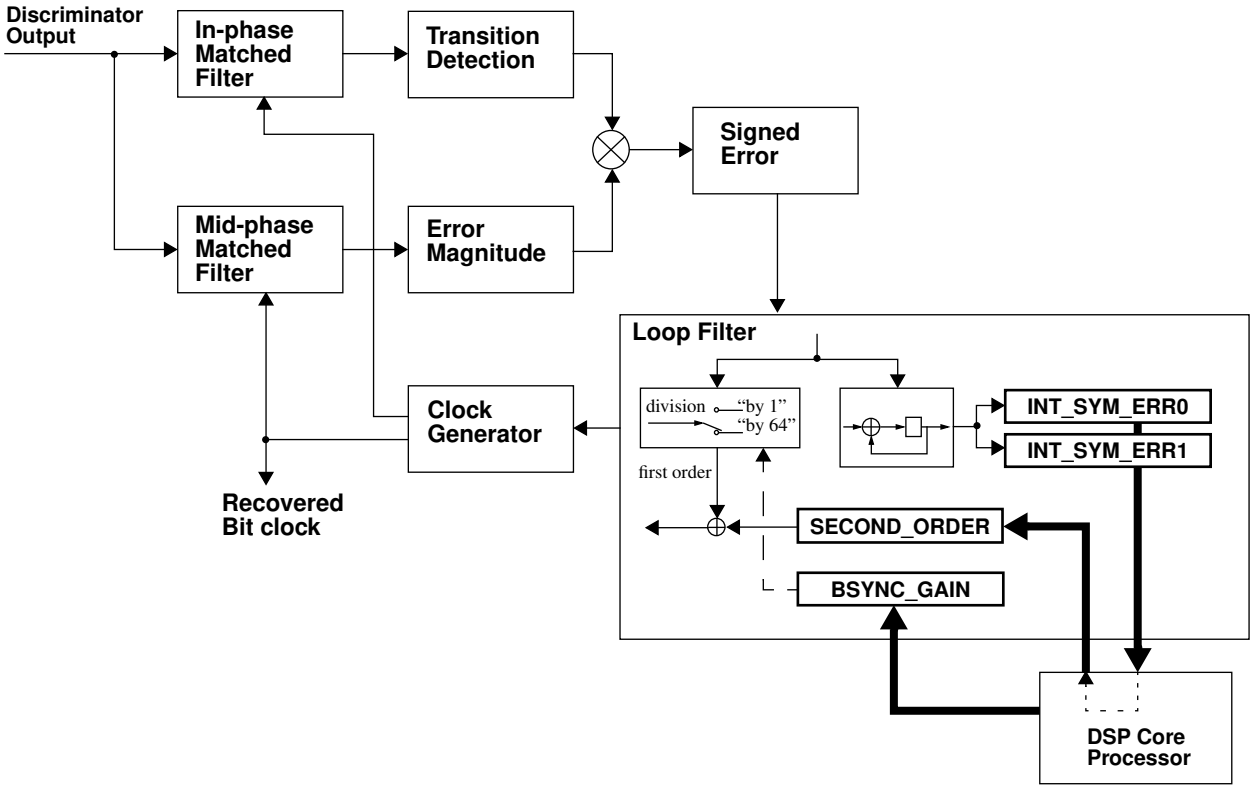


Figure 6. Bit Synchronizer Loop and Processor Control