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Totally Logical

Z89223/273/323/373

16-BIT DIGITAL SIGNAL PROCESSORS WITH A/D CONVERTER

FEATURES

Device	Package	ROM (Kwords)	OTP (Kwords)	Data RAM (Words)	MIPS
Z89223	44-PLCC, 44-PQFP	8		512	20
Z89273	44-PLCC		8	512	20
Z89323	64-TQFP, 68-PLCC, 80-PQFP	8		512	20
Z89373	64-TQFP, 68-PLCC, 80-PQFP		8	512	20

Operating Range

- 5V ±10%
- 0°C to 70°C Standard Temperature
  –40°C to +85°C Extended Temperature

DSP Core

- 16-Bit Fixed Point DSP, 24-Bit ALU and Accumulator
- Single-Cycle Multiply and ALU Operations
- Six-Level Hardware Stack
- Six Data RAM Pointers and Sixteen Program Memory Pointers
- RISC Processor with 30 Instruction Types

On-Chip Peripherals

- 4-Channel, 8-Bit Half-Flash A/D Converter
- Serial Peripheral Interface (SPI)
- Three General-Purpose Counter/Timers
  - Two Pulse Width Modulators (PWM)
  - Two Watch-Dog Timers (WDT)
- Up to 40 Bits of I/O
- PLL System Clock
- Three Vectored Interrupts Servicing Eight Sources
- Low Power Clock Modes with Wake-up Options

GENERAL DESCRIPTION

The Z893x3 products are high-performance Digital Signal Processors (DSP) with a modified Harvard architecture featuring separate program and dual data memory banks. The design is optimized for processing power with a minimum of silicon area.

The Z893x3 16/24-Bit architecture accommodates advanced signal processing algorithms. The operating performance and efficient architecture provide deterministic instruction execution. Compression, filtering, frequency detection, audio, voice detection, speech synthesis, and other vital algorithms can all be implemented.

Six data RAM pointers provide circular buffer capabilities and simultaneous dual operand fetching. Three vectored interrupts are complemented by a six-level stack.

By integrating a high-speed 4-channel, 8-bit A/D, SPI, three Counter/Timers with PWM and WDT support, and up to 40 bits of I/O, the Z893x3 family provides a compact low-cost system solution.

To support a wide variety of development requirements, the Z893x3 DSP product family features the cost-effective Z89223/323 with 8 KWords of ROM. The Z89273/373, an

GENERAL DESCRIPTION (Continued)

OTP version of the Z89223/323, is ideal for prototypes and early production builds.

Throughout this specification, references to the Z893x3 device apply equally to the Z89223/273/323/373, unless otherwise specified.

Notes: All signals with an overline are active Low. For example, in RD/$\overline{WR}$, RD is active High and $\overline{WR}$ is active Low. For I/O ports, P1.3 denotes Port1 bit 3. Pins called NC are "No Connection"—they do not connect any power, grounds, or signals.

Power connections follow conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

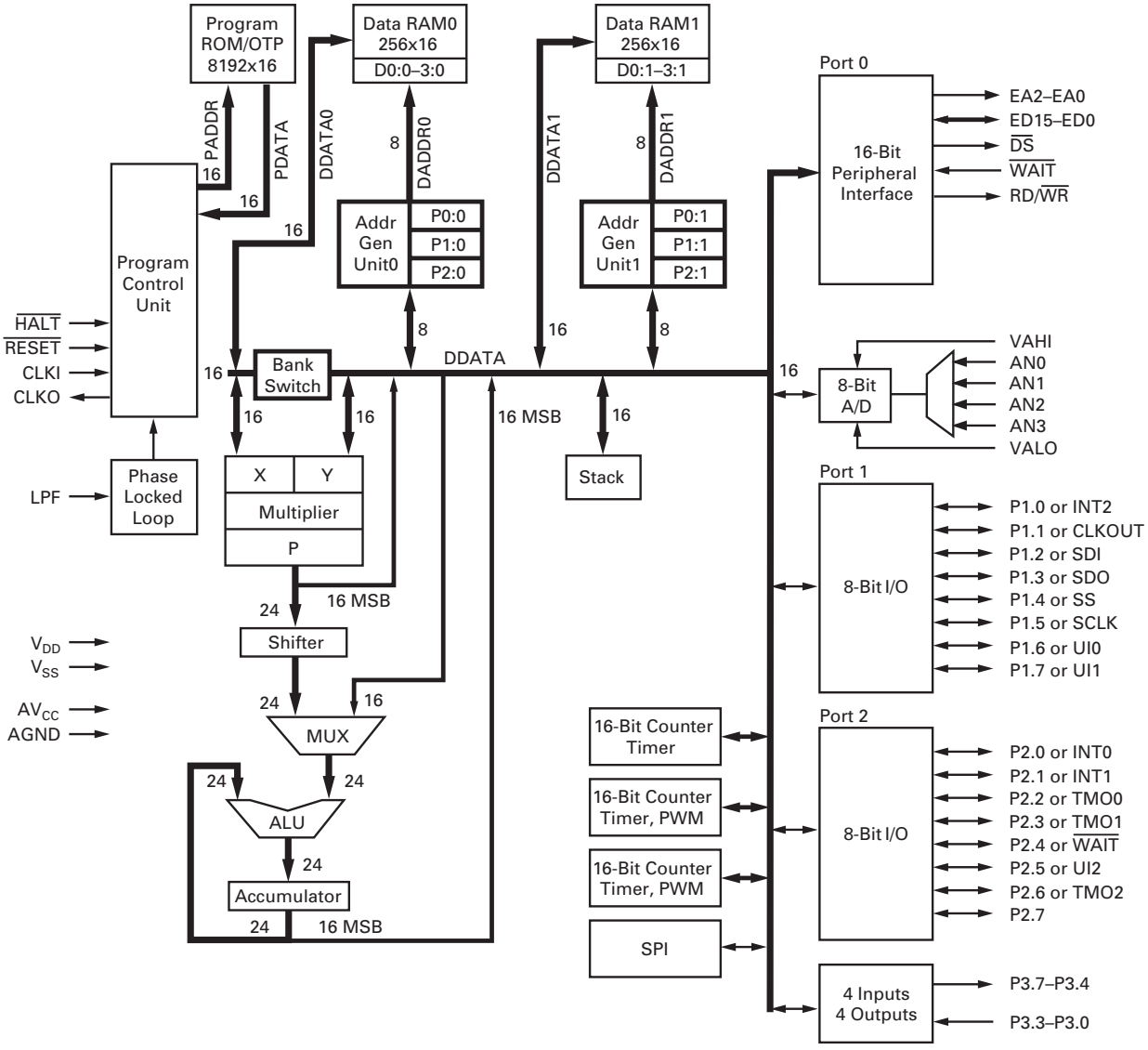


Figure 1. Z892X3/3x3 Functional Block Diagram

External Bus and External Registers. The following is made to clarify naming conventions used in this specification. The external bus and external registers are external to the DSP core, and are used to access internal and external peripherals.

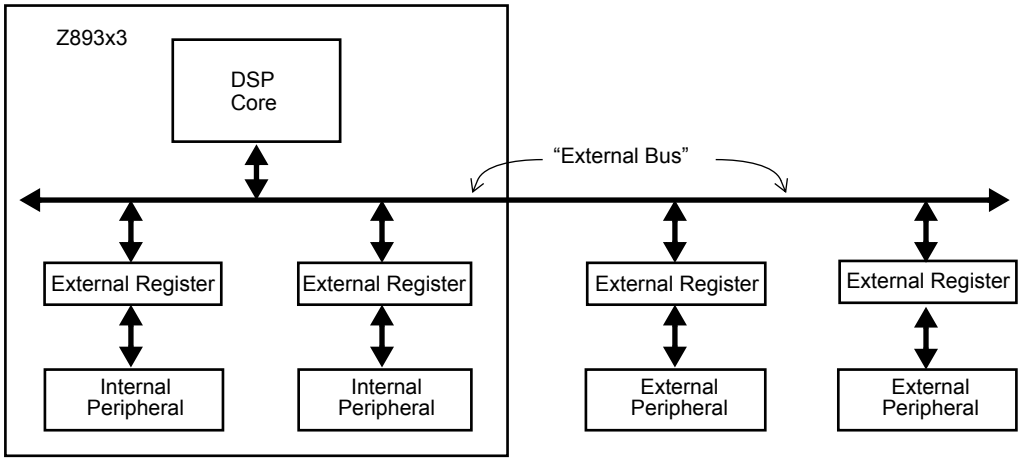


Figure 2. "External" Bus

PIN FUNCTIONS

EA2–EA0. External Address Bus (output, latched). These pins provide the External Register Address. This address bus is driven during both internal and external accesses. One of up to seven user-defined external registers is selected by the processor for reads or writes. EXT7 is always reserved for use by the processor.

ED15–ED0. External Data Bus (input/output). These pins are the data bus for the user-defined external registers, and are shared by Port0. These pins are normally tristated, except when these registers are specified as destination registers in a write instruction to an external peripheral, or when Port0 is enabled for output. This bus uses the control signals RD/$\overline{WR}$, $\overline{DS}$, and $\overline{WAIT}$, and address pins EA2–EA0.

$\overline{DS}$. Data Strobe (output). This pin provides the data strobe signal for the ED Bus. $\overline{DS}$ is active for transfers to/from external peripherals only.

RD/$\overline{WR}$. Read/$\overline{Write}$ Select (output). This pin controls the data direction signal for the External Data Bus. Data is available from the processor on ED15–ED0 when this signal and $\overline{DS}$ are both Low.

$\overline{WAIT}$. Wait State (input). This pin is sampled at the rising edge of the clock with appropriate setup and hold times. A single wait-state can be generated internally by setting the appropriate bits in the wait state register. The user must drive this line if multiple wait states are required. This pin is shared with Port2.

CLKI. Clock (input). This pin is the clock circuit input. It can be driven by a signal or connected to a 32 KHz crystal.

CLKO. Clock (output). This pin is the clock circuit output. It is used for operation with a 32 KHz crystal and the PLL to generate the system clock.

$\overline{HALT}$. Halt State (input). This pin stops program execution. The processor continuously executes NOPs and the program counter remains constant while this pin is held Low. This pin offers an internal pull-up.

$\overline{RESET}$. Reset (input). This pin resets the processor. It pushes the contents of the Program Counter (PC) onto the stack and then fetches a new PC value from program memory address 0FFCH after the $\overline{RESET}$ signal is released. The Status register is set to all zeros. At power-up RAM and other registers are undefined, however, they are left unchanged with subsequent resets. $\overline{RESET}$ can be asserted asynchronously.

AN0–AN3. Analog Inputs (input). These are the analog input pins. The analog input signal should be between VALO and VAHI for accurate conversions.

VAHI. Analog High Reference Voltage (input). This pin provides the reference for the full scale voltage of the analog input signals.

VALO. Analog Low Reference Voltage (input). This pin provides the reference for the zero voltage of the analog input signals.

AV_{CC}–AGND. Filtered Analog Power and Ground must be provided on separate pins to reduce digital noise in the analog circuits.

Multifunction Pins. The Z89223/273/323/373 DSP family offers a user-configurable I/O structure, which means that most of the I/O pins offer dual functions. The function, direction (input or output), and for output, the characteristics (push-pull or open drain) are all under user-control, by programming the configuration registers appropriately as described in the I/O Ports section. The following share I/O Port pins:

INT0–INT2. External Interrupts (input, edge-triggered). These pins provide three of the eight interrupt sources to the Interrupt Controller. Each is programmable to be rising-edge or falling-edge triggered. The other five interrupt sources are from the on-chip peripherals.

CLKOUT. System Clock (output). This pin provides access to the internal processor clock.

SDI. Serial Data In (input). This pin is the SPI serial data input.

SDO. Serial Data Out (output). This pin is the SPI serial data output.

SS. Slave Select (input). This pin is used in SPI Slave Mode only. SS advises the SPI that it is the target of a serial transfer from an external Master.

SCLK. SPI Clock (output/input). This pin is an output in Master mode and an input in Slave mode.

UI0, UI1. User inputs (input). These general-purpose input pins are directly tested by the conditional branch instructions. They can also be read as bits in the status register. These are asynchronous input signals that require no special clock synchronization. Counter/Timer0 and Counter/Timer1 may use either of these pins as input.

UI2. User Input (input). This pin is the input to Counter/Timer 2.

TMO0/UO0. Counter/Timer Output or User Output 0 (output). Counter/Timer 0 and Counter/Timer 1 can be programmed to provide output on this pin. When User Outputs are enabled, and the Counter/Timer is disabled, this pin provides the complement of Status Register bit 5.

TMO1/UO1. Counter/Timer Output or User Output 1 (output). Counter/Timer 0 and Counter/Timer 1 can be programmed to provide output on this pin. When User Outputs are enabled, and the Counter/Timer is disabled, this pin provides the complement of Status Register bit 6.

TMO2. Counter/Timer 2 Output (output). This pin is the output of Counter/Timer 2

P0.15–P0.0. Port0 (input/output). This is a 16-bit user I/O port. Bits can be configured as input or output or globally as open-drain output. When enabled, Port0 uses the 16 data lines of the ED bus. The function of these pins can be dynamically changed by writing to the Port0 configuration registers. The High byte can also be configured to Port1 as described in the I/O Port section.

P1.7–P1.0. Port1 (input/output). These pins are Port1 inputs or outputs when not configured for use as special purpose peripheral interface. The following eight pin functions preempt use of these pins when enabled. INT2, CLKOUT, SDI, SDO, SS, SCLK, UI0, UI1.

Note: These pins are not bonded out on the 44-pin packages.

P2.7–P2.0. Port2 (input/output). These pins are Port2 inputs or outputs when not configured as peripheral interfaces. The following seven pin functions preempt use of P2.6–P2.0 when enabled. INT0, INT1, TMO0/UO0, TMO1/UO1, $\overline{\text{WAIT}}$, UI2, TMO2. P2.7 does not include a dual function.

Note: P2.7–P2.5 are not bonded out on the 44-pin packages.

The following port pins are available only on the 80-pin package:

P3.7–P3.4. Port3 (output). These pins are Port3 outputs.

P3.3–P3.0. Port3 (input). These pins are Port3 inputs.

PIN CONFIGURATIONS

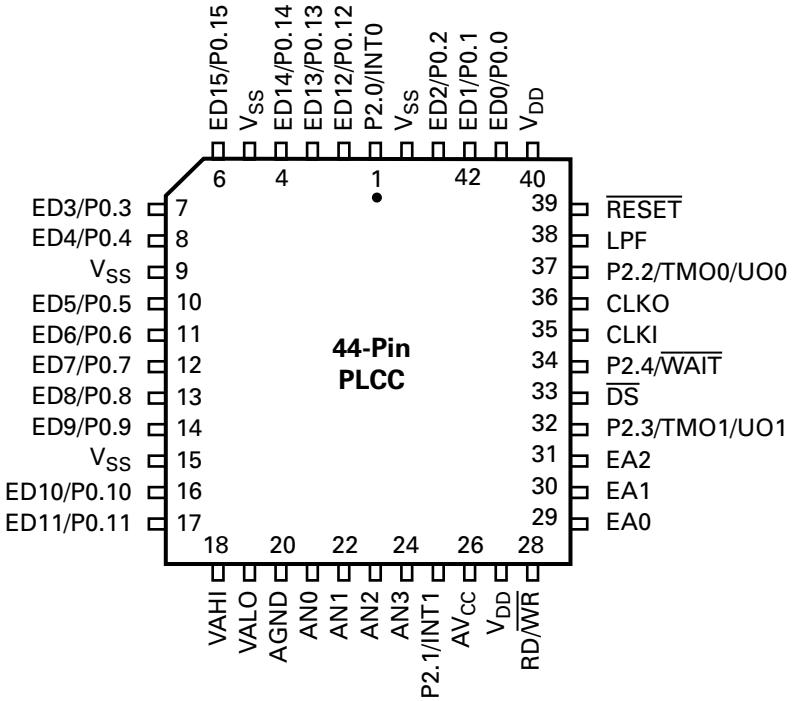


Figure 3. 44-Pin PLCC Z89223/273 Pin Configuration

Table 1. 44-Pin PLCC Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output	23	AN2	A/D Input 2	Input
2	ED12/P0.12	External Data Bus/Port0	Input/Output	24	AN3	A/D Input 3	Input
3	ED13/P0.13	External Data Bus/Port0	Input/Output	25	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output
4	ED14/P0.14	External Data Bus/Port0	Input/Output	26	AV_{CC}	Analog Power	
5	V_{SS}	Ground		27	V_{DD}	Power Supply	
6	ED15/P0.15	External Data Bus/Port0	Input/Output	28	RD/$\overline{WR}$	R/W External Bus	Output
7	ED3/P0.3	External Data Bus/Port0	Input/Output	29	EA0	Ext Address 0	Output
8	ED4/P0.4	External Data Bus/Port0	Input/Output	30	EA1	Ext Address 1	Output
9	V_{SS}	Ground		31	EA2	Ext Address 2	Output
10	ED5/P0.5	External Data Bus/Port0	Input/Output	32	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
11	ED6/P0.6	External Data Bus/Port0	Input/Output	33	$\overline{DS}$	Ext Data Strobe	Output
12	ED7/P0.7	External Data Bus/Port0	Input/Output	34	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
13	ED8/P0.8	External Data Bus/Port0	Input/Output	35	CLKI	Clock/Crystal In	Input
14	ED9/P0.9	External Data Bus/Port0	Input/Output	36	CLKO	Clock/Crystal Out	Output
15	V_{SS}	Ground		37	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
16	ED10/P0.10	External Data Bus/Port0	Input/Output	38	LPF	PLL Low Pass Filter	Input
17	ED11/P0.11	External Data Bus/Port0	Input/Output	39	$\overline{RESET}$	Reset	Input
18	VAHI	Analog High Ref. Voltage	Input	40	V_{DD}	Power	
19	VALO	Analog Low Ref. Voltage	Input	41	ED0/P0.0	External Data Bus/Port0	Input/Output
20	AGND	Analog Ground		42	ED1/P0.1	External Data Bus/Port0	Input/Output
21	AN0	A/D Input 0	Input	43	ED2/P0.2	External Data Bus/Port0	Input/Output
22	AN1	A/D Input 1	Input	44	V_{SS}	Ground	

PIN CONFIGURATIONS (Continued)

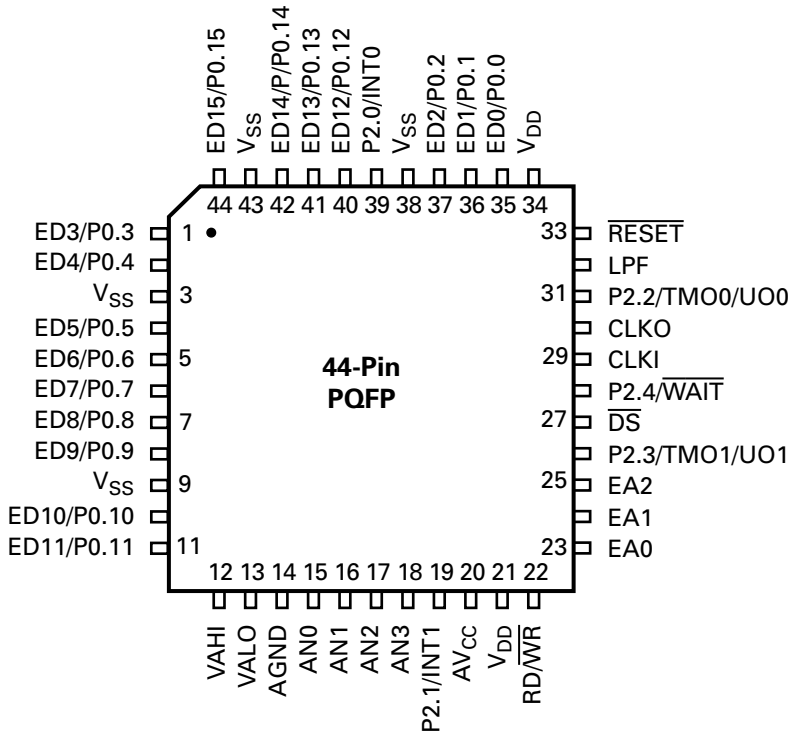


Figure 4. 44-Pin PQFP Z89223/273 Pin Configuration

Table 2. 44-Pin PQFP Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	ED3/P0.3	External Data Bus/Port0	Input/Output	23	EA0	Ext Address 0	Output
2	ED4/P0.4	External Data Bus/Port0	Input/Output	24	EA1	Ext Address 1	Output
3	V_{SS}	Ground		25	EA2	Ext Address 2	Output
4	ED5/P0.5	External Data Bus/Port0	Input/Output	26	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
5	ED6/P0.6	External Data Bus/Port0	Input/Output	27	$\overline{DS}$	Ext Data Strobe	Output
6	ED7/P0.7	External Data Bus/Port0	Input/Output	28	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
7	ED8/P0.8	External Data Bus/Port0	Input/Output	29	CLKI	Clock/Crystal In	Input
8	ED9/P0.9	External Data Bus/Port0	Input/Output	30	CLKO	Clock/Crystal Out	Output
9	V_{SS}	Ground		31	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
10	ED10/P0.10	External Data Bus/Port0	Input/Output	32	LPF	PLL Low Pass Filter	Input
11	ED11/P0.11	External Data Bus/Port0	Input/Output	33	$\overline{RESET}$	Reset	Input
12	VAHI	Analog High Ref. Voltage	Input	34	V_{DD}	Power Supply	
13	VALO	Analog Low Ref. Voltage	Input	35	ED0/P0.0	External Data Bus/Port0	Input/Output
14	AGND	Analog Ground		36	ED1/P0.1	External Data Bus/Port0	Input/Output
15	AN0	A/D Input 0	Input	37	ED2/P0.2	External Data Bus/Port0	Input/Output
16	AN1	A/D Input 1	Input	38	V_{SS}	Ground	
17	AN2	A/D Input 2	Input	39	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output
18	AN3	A/D Input 3	Input	40	ED12/P0.12	External Data Bus/Port0	Input/Output
19	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output	41	ED13/P0.13	External Data Bus/Port0	Input/Output
20	AV_{CC}	Analog Power		42	ED14/P0.14	External Data Bus/Port0	Input/Output
21	V_{DD}	Power		43	V_{SS}	Ground	
22	RD/$\overline{WR}$	R/W Exteral Output Bus		44	ED15/P0.15	External Data Bus/Port0	Input/Output

PIN CONFIGURATIONS (Continued)

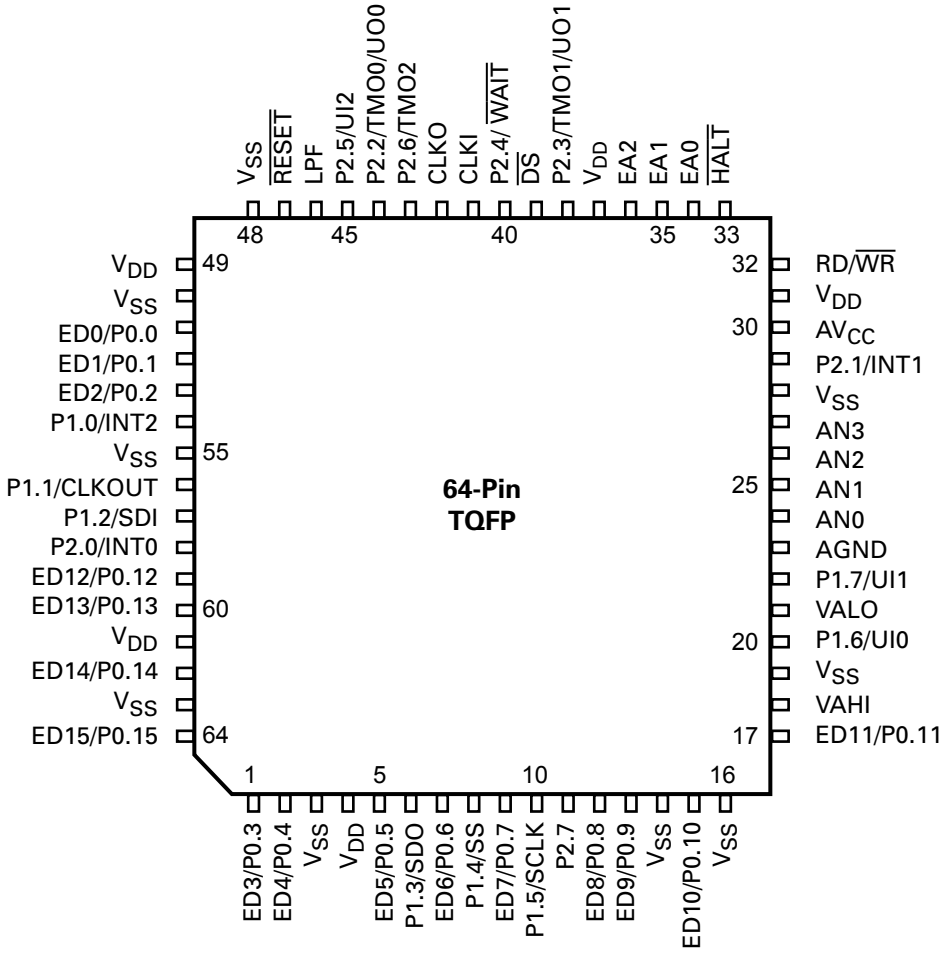


Figure 5. 64-Pin TQFP Z89323/373 Pin Configuration

Table 3. 64-Pin TQFP Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	ED3/P0.3	External Data Bus/Port0	Input/Output	33	$\overline{HALT}$	Halt Execution	Input
2	ED4/P0.4	External Data Bus/Port0	Input/Output	34	EA0	Ext Address 0	Output
3	V_{SS}	Ground		35	EA1	Ext Address 1	Output
4	V_{DD}	Power Supply		36	EA2	Ext Address 2	Output
5	ED5/P0.5	External Data Bus/Port0	Input/Output	37	V_{DD}	Power Supply	
6	P1.3/SDO	Port 1.3/Serial Output	Input/Output	38	P2.3/TMO1	Port2.3/Timer Output 1	Input/Output
7	ED6/P0.6	External Data Bus/Port0	Input/Output	39	$\overline{DS}$	Ext Data Strobe	Output
8	P1.4/SS	Port 1.4/Slave Select	Input/Output	40	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
9	ED7/P0.7	External Data Bus/Port0	Input/Output	41	CLKI	Clock/Crystal In	Input
10	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	42	CLKO	Clock/Crystal Out	Output
11	P2.7	Port 2.7	Input/Output	43	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
12	ED8/P0.8	External Data Bus/Port0	Input/Output	44	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
13	ED9/P0.9	External Data Bus/Port0	Input/Output	45	P2.5/UI2	Port 2.5/User Input 2	Input/Output
14	V_{SS}	Ground		46	LPF	PLL Low Pass Filter	Input
15	ED10/P0.10	External Data Bus/Port0	Input/Output	47	$\overline{RESET}$	Reset	Input
16	V_{SS}	Ground		48	V_{SS}	Ground	
17	ED11/P0.11	External Data Bus/Port0	Input/Output	49	V_{DD}	Power Supply	
18	VAHI	Analog High Ref. Voltage	Input	50	V_{SS}	Ground	
19	V_{SS}	Ground		51	ED0/P0.0	External Data Bus/Port0	Input/Output
20	P1.6/UI0	Port 1.6/User Input 0	Input/Output	52	ED1/P0.1	External Data Bus/Port0	Input/Output
21	VALO	Analog Low Ref. Voltage	Input	53	ED2/P0.2	External Data Bus/Port0	Input/Output
22	P1.7/UI1	Port 1.7/User Input 1	Input/Output	54	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
23	AGND	Analog Ground		55	V_{SS}	Ground	
24	AN0	A/D Input 0	Input	56	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output
25	AN1	A/D Input 1	Input	57	P1.2/SDI	Port 1.2/Serial Input	Input/Output
26	AN2	A/D Input 2	Input	58	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output
27	AN3	A/D Input 3	Input	59	ED12/P0.12	External Data Bus/Port0	Input/Output
28	V_{SS}	Ground		60	ED13/P0.13	External Data Bus/Port0	Input/Output
29	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output	61	V_{DD}	Power Supply	
30	AVCC	Analog Power		62	ED14/P0.14	External Data Bus/Port0	Input/Output
31	V_{DD}	Power Supply		63	V_{SS}	Ground	
32	RD/$\overline{WR}$	R/W External Bus	Output	64	ED15/P0.15	External Data Bus/Port0	Input/Output

PIN CONFIGURATIONS (Continued)

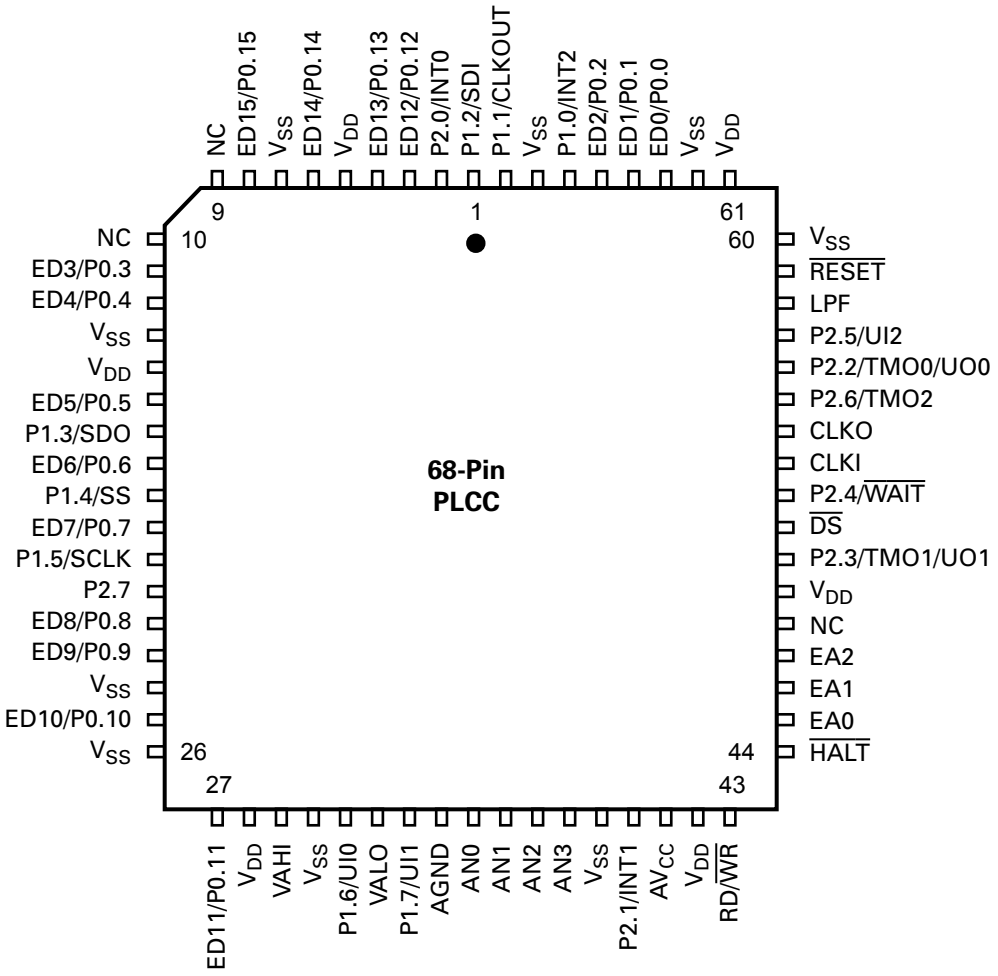


Figure 6. 68-Pin PLCC Z89323/373 Pin Configuration

Table 4. 68-Pin PLCC Z89323/373 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	P1.2/SDI	Port 1.2/Serial Input	Input/Output	35	AN0	A/D Input 0	Input
2	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output	36	AN1	A/D Input 1	Input
3	ED12/P0.12	External Data Bus/Port0	Input/Output	37	AN2	A/D Input 2	Input
4	ED13/P0.13	External Data Bus/Port0	Input/Output	38	AN3	A/D Input 3	Input
5	V_{DD}	Power Supply		39	V_{SS}	Ground	
6	ED14/P0.14	External Data Bus/Port0	Input/Output	40	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output
7	V_{SS}	Ground		41	AVCC	Analog Power	
8	ED15/P0.15	External Data Bus/Port0	Input/Output	42	V_{DD}	Power Supply	
9	NC	No Connection		43	RD/$\overline{WR}$	R/W External Bus	Output
10	NC	No Connection		44	$\overline{HALT}$	Halt Execution	Input
11	ED3/P0.3	External Data Bus/Port0	Input/Output	45	EA0	Ext Address 0	Output
12	ED4/P0.4	External Data Bus/Port0	Input/Output	46	EA1	Ext Address 1	Output
13	V_{SS}	Ground		47	EA2	Ext Address 2	Output
14	V_{DD}	Power Supply		48	NC	No Connection	
15	ED5/P0.5	External Data Bus/Port0	Input/Output	49	V_{DD}	Power Supply	
16	P1.3/SDO	Port 1.3/Serial Output	Input/Output	50	P2.3/TMO1	Port2.3/Timer Output 1	Input/Output
17	ED6/P0.6	External Data Bus/Port0	Input/Output	51	$\overline{DS}$	Ext Data Strobe	Output
18	P1.4/SS	Port 1.4/Slave Select	Input/Output	52	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
19	ED7/P0.7	External Data Bus/Port0	Input/Output	53	CLKI	Clock/Crystal In	Input
20	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	54	CLKO	Clock/Crystal Out	Output
21	P2.7	Port 2.7	Input/Output	55	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
22	ED8/P0.8	External Data Bus/Port0	Input/Output	56	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
23	ED9/P0.9	External Data Bus/Port0	Input/Output	57	P2.5/UI2	Port 2.5/User Input 2	Input/Output
24	V_{SS}	Ground		58	LPF	PLL Low Pass Filter	Input
25	ED10/P0.10	External Data Bus/Port0	Input/Output	59	$\overline{RESET}$	Reset	Input
26	V_{SS}	Ground		60	V_{SS}	Ground	
27	ED11/P0.11	External Data Bus/Port0	Input/Output	61	V_{DD}	Power Supply	
28	V_{DD}	Power Supply		62	V_{SS}	Ground	
29	VAHI	Analog High Ref. Voltage	Input	63	ED0/P0.0	External Data Bus/Port0	Input/Output
30	V_{SS}	Ground		64	ED1/P0.1	External Data Bus/Port0	Input/Output
31	P1.6/UI0	Port 1.6/User Input 0	Input/Output	65	ED2/P0.2	External Data Bus/Port0	Input/Output
32	VALO	Analog Low Ref. Voltage	Input	66	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
33	P1.7/UI1	Port 1.7/User Input 1	Input/Output	67	V_{SS}	Ground	
34	AGND	Analog Ground		68	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output

PIN CONFIGURATIONS (Continued)

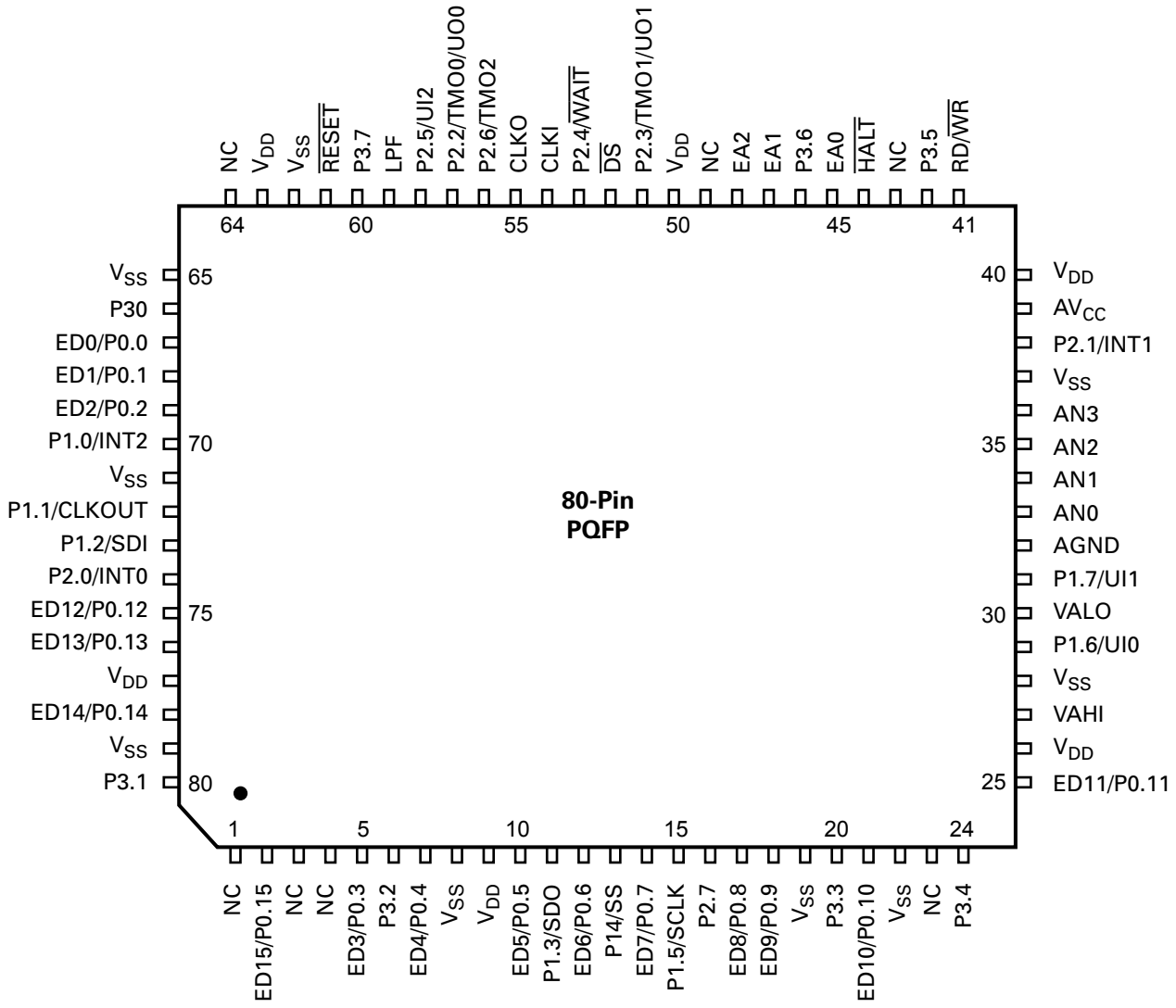


Figure 7. 80-Pin PQFP Z89323/373 Pin Configuration

Table 5. 80-Pin PQFP Z89323/373 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	NC	No Connection		41	RD/$\overline{WR}$	R/W External Bus	Output
2	ED15/P0.15	External Data Bus/Port0	Input/Output	42	P3.5	Port 3.5	Output
3	NC	No Connection		43	NC	No Connection	
4	NC	No Connection		44	$\overline{HALT}$	Halt Execution	Input
5	ED3/P0.3	External Data Bus/Port0	Input/Output	45	EA0	Ext Address 0	Output
6	P3.2	Port 3.2	Input	46	P3.6	Port 3.6	Output
7	ED4/P0.4	External Data Bus/Port0	Input/Output	47	EA1	Ext Address 1	Output
8	V_{SS}	Ground		48	EA2	Ext Address 2	Output
9	V_{DD}	Power Supply		49	NC	No Connection	
10	ED5/P0.5	External Data Bus/Port0	Input/Output	50	V_{DD}	Power Supply	
11	P1.3/SDO	Port 1.3/Serial Output	Input/Output	51	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
12	ED6/P0.6	External Data Bus/Port0	Input/Output	52	$\overline{DS}$	Ext Data Strobe	Output
13	P1.4/SS	Port 1.4/Slave Select	Input/Output	53	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
14	ED7/P0.7	External Data Bus/Port0	Input/Output	54	CLKI	Clock/Crystal In	Input
15	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	55	CLKO	Clock/Crystal Out	Output
16	P2.7	Port 2 7	Input/Output	56	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
17	ED8/P0.8	External Data Bus/Port0	Input/Output	57	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
18	ED9/P0.9	External Data Bus/Port0	Input/Output	58	P2.5/UI2	Port 2.5/User Input 2	Input/Output
19	V_{SS}	Ground		59	LPF	PLL Low Pass Filter	Input
20	P3.3	Port 3 3	Input	60	P3.7	Port 3.7	Output
21	ED10/P0.10	External Data Bus/Port0	Input/Output	61	$\overline{RESET}$	Reset	Input
22	V_{SS}	Ground		62	V_{SS}	Ground	
23	NC	No Connection		63	V_{DD}	Power Supply	
24	P3.4	Port 3.4	Output	64	NC	No Connection	
25	ED11/P0.11	External Data Bus/Port0	Input/Output	65	V_{SS}	Ground	
26	V_{DD}	Power Supply		66	P3.0	Port 3.0	Input
27	VAHI	Analog High Ref. Voltage	Input	67	ED0/P0.0	External Data Bus/Port0	Input/Output
28	V_{SS}	Ground		68	ED1/P0.1	External Data Bus/Port0	Input/Output
29	P1.6/UI0	Port 1 6/User Input 0	Input/Output	69	ED2/P0.2	External Data Bus/Port0	Input/Output
30	VALO	Analog Low Ref. Voltage	Input	70	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
31	P1.7/UI1	Port 1 7/User Input 1	Input/Output	71	V_{SS}	Ground	
32	AGND	Analog Ground		72	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output
33	AN0	A/D Input 0	Input	73	P1.2/SDI	Port 1.2/Serial Input	Input/Output
34	AN1	A/D Input 1	Input	74	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output
35	AN2	A/D Input 2	Input	75	ED12/P0.12	External Data Bus/Port0	Input/Output
36	AN3	A/D Input 3	Input	76	ED13/P0.13	External Data Bus/Port0	Input/Output
37	V_{SS}	Ground		77	V_{DD}	Power Supply	
38	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output	78	ED14/P0.14	External Data Bus/Port0	Input/Output
39	AV_{CC}	Analog Power		79	V_{SS}	Ground	
40	V_{DD}	Power Supply		80	P3.1	Port 3.1	Input

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	–0.3	7.0	V
T_{STG}	Storage Temperature	–65	150	°C
T_A	Ambient Operating Temperature			
	"S" device	0	70	°C
	"E" device	–40	85	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin.

Positive current $I_{(+)}$ flows in to the referenced pin.

Negative current $I_{(-)}$ flows out of the referenced pin.

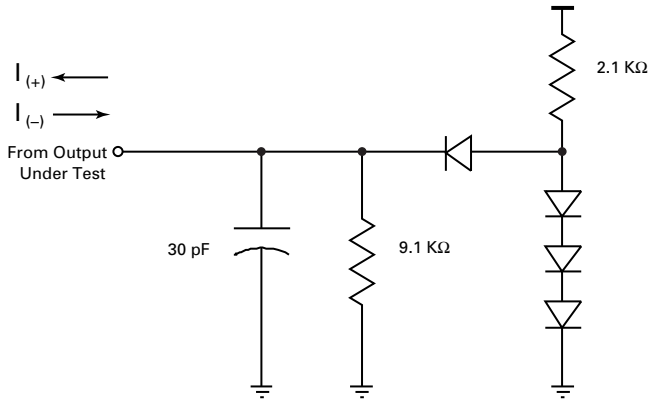


Figure 8. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

Table 6. ROM Version: V_{DD} = 5V ±10%, T_A = 0°C to +70°C for "S" temperature range T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted; IDD measured with peripherals disabled

Symbol	Parameter	Condition	Min	Typical	Max
$I_{DD–PLL}$	Supply Current using PLL	V_{DD} = 5.0V, 20 MHz		60mA	66mA
$I_{DD–ECD}$	Supply Current using External Clock Direct	V_{DD} = 5.0V, 20 MHz		55 mA	61mA
$I_{DD–XOD}$	Supply Current using XTAL Oscillator Direct	V_{DD} = 5.0V, 32-kHz XTAL		250µA	275µA
$I_{DD–DEEP}$	Supply Current during Deep Sleep	V_{DD} = 5.0V, 32kHz XTAL		175µA	193µA
V_{IH}	Input High Level		2.7V		
V_{IL}	Input Low Level				0.8V
I_L	Input Leakage		-10µA		10µA
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{DD}–0.2V		
		I_{OH} = –160 µA	2.4V		
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4V
		I_{OL} = 2.0 mA			0.5V
I_{FL}	Output Floating Leakage Current		-10µA		10µA

Table 7. OTP Version: V_{DD} = 5V ±10%, T_A = 0°C to +70°C for "S" temperature range T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted; IDD measured with peripherals disabled

Symbol	Parameter	Condition	Min	Typical	Max
$I_{DD–PLL}$	Supply Current using PLL	V_{DD} = 5.0V, 20 MHz		78mA	86mA
$I_{DD–ECD}$	Supply Current using External Clock Direct	V_{DD} = 5.0V, 20 MHz		75mA	83mA
$I_{DD–XOD}$	Supply Current using XTAL Oscillator Direct	V_{DD} = 5.0V, 32-kHz XTAL		17mA	19mA
$I_{DD–DEEP}$	Supply Current during Deep Sleep	V_{DD} = 5.0V, 32kHz XTAL		17mA	19mA
V_{IH}	Input High Level		2.7V		
V_{IL}	Input Low Level				0.8V
I_L	Input Leakage		-10µA		10µA
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{DD}–0.2V		
		I_{OH} = –160 µA	2.4V		
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4V
		I_{OL} = 2.0 mA			0.5V
I_{FL}	Output Floating Leakage Current		-10µA		10µA

DC ELECTRICAL CHARACTERISTICS (Continued)

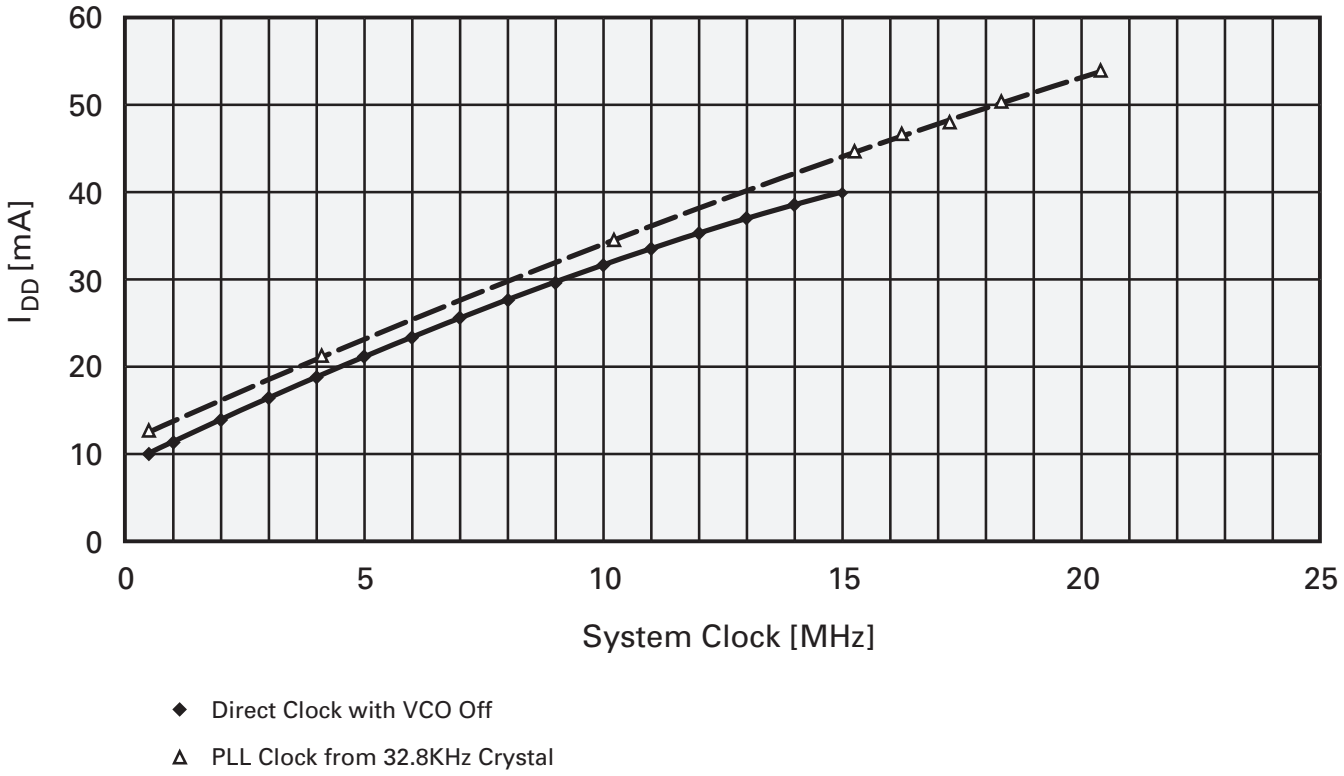


Figure 9. Z89373 Typical OTP Current Consumption

AC ELECTRICAL CHARACTERISTICS

Table 8. V_{DD}= 5V ±10%, T_A = 0°C to +70°C for "S" Temperature Range T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted

Symbol	Parameter	Min [ns]	Max [ns]
Clock			
TCY	CLKI Cycle Time for user-supplied clock	50	31250
CPWH	CLKI Pulse Width High	21	
CPWL	CLKI Pulse Width Low	21	
Tr	CLKI Rise Time for 20-MHz user-supplied clock		2
Tf	CLKI Fall Time for 20-MHz user-supplied clock		2
External Peripheral Bus			
EASET	EA Setup Time to $\overline{DS}$ Fall	10	
EAHOLD	EA Hold Time from $\overline{DS}$ Rise	4	
RWSET	Read/Write Setup Time to $\overline{DS}$ Fall	10	
RWHOLD	Read/Write Hold Time from $\overline{DS}$ Rise	0	
RDSET	Data Read Setup Time to $\overline{DS}$ Rise	15	
RDHOLD	Data Read Hold Time from $\overline{DS}$ Rise	0	
WRVALID	Data Write Valid Time from $\overline{DS}$ Fall		5
WRHOLD	Data Write Hold Time from $\overline{DS}$ Rise	2	
Reset			
RRISE	Reset Rise Time		20 TCY
RWIDTH	Reset Low Pulse Width	2 TCY	
Interrupt			
IWIDTH	Interrupt Pulse Width	1TCY	
Halt			
HWIDTH	Halt Low Pulse Width	3 TCY	
Wait State			
WLAT	Wait Latency Time from $\overline{DS}$ Fall		7
WDEA	Wait Deassert Setup Time to CLKOUT Rise	TBD	
SPI			
SDI–SCLK	Serial Data In to Serial Clock Setup Time	10	
SCLK–SDO	Serial Clock to Serial Data Out Valid	15	
SS–SCLK	Slave Select to Serial Clock Setup Time	1/2 SCLK Period	
SS–SDO	Slave Select to Serial Data Out Valid	15	
SCLK–SDI	Serial Clock to Serial Data In Hold Time	10	

8-BIT ANALOG/DIGITAL CONVERTER

Table 9. AV_{CC}–AGND = 5V ±10%
T_A = 0°C to +70°C for "S" temperature range, unless otherwise noted

Parameter	Min	Typ	Max	Units
Integral Nonlinearity (INL)		0.5	1	LSB
Differential Nonlinearity (DNL)		0.5	1	LSB
Zero Offset Error		2	3	LSB
Full Scale Offset Error		2	3	LSB
Valid Input Signal Range	VALO		VAHI	V
Input Capacitance		33	40	pF
Conversion Time	2	3		µs
Input Impedance 500kSPS 100kSPS 44kSPS		 10 48 110		 kΩ kΩ kΩ
VAHI	VALO + 2.5		AV_{CC}	V
VALO	AGND		AV_{CC}–2.5	V
VAHI–VALO	2.5		AV_{CC}	V
Reference Ladder Resistance VAHI to VALO		5		kΩ
Power Dissipation		50	85	mW

Table 10. AV_{CC}–AGND = 5V ±10%
T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted

Parameter	Min	Typ	Max	Units
Integral Nonlinearity (INL)			1	LSB
Differential Nonlinearity (DNL)			1	LSB
Zero Offset Error		3	4	LSB
Full Scale Offset Error		3	4	LSB
Valid Input Signal Range	VALO		VAHI	V
Input Capacitance		33	40	pF
Conversion Time	2	3		µs
Input Impedance 500kSPS 100kSPS 44kSPS		 10 48 110		 kΩ kΩ kΩ
VAHI	VALO + 2.5		AV_{CC}	V
VALO	AGND		AV_{CC}–2.5	V
VAHI–VALO	2.5		AV_{CC}	V
Reference Ladder Resistance VAHI to VALO		5		kΩ
Power Dissipation			85	mW

TIMING DIAGRAMS

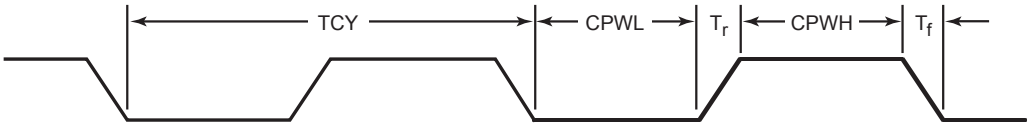


Figure 10. Clock Timing

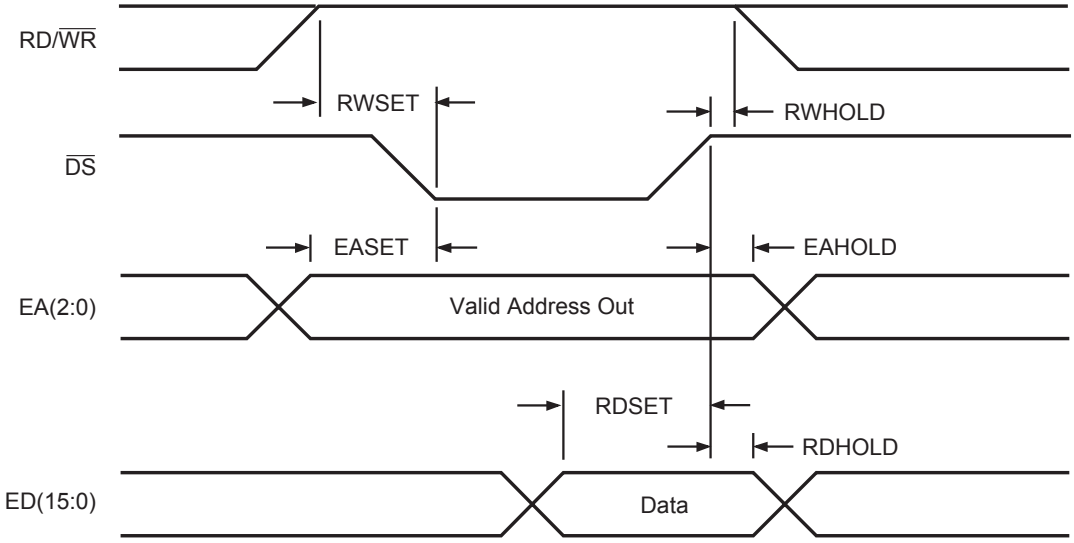


Figure 11. Read Timing

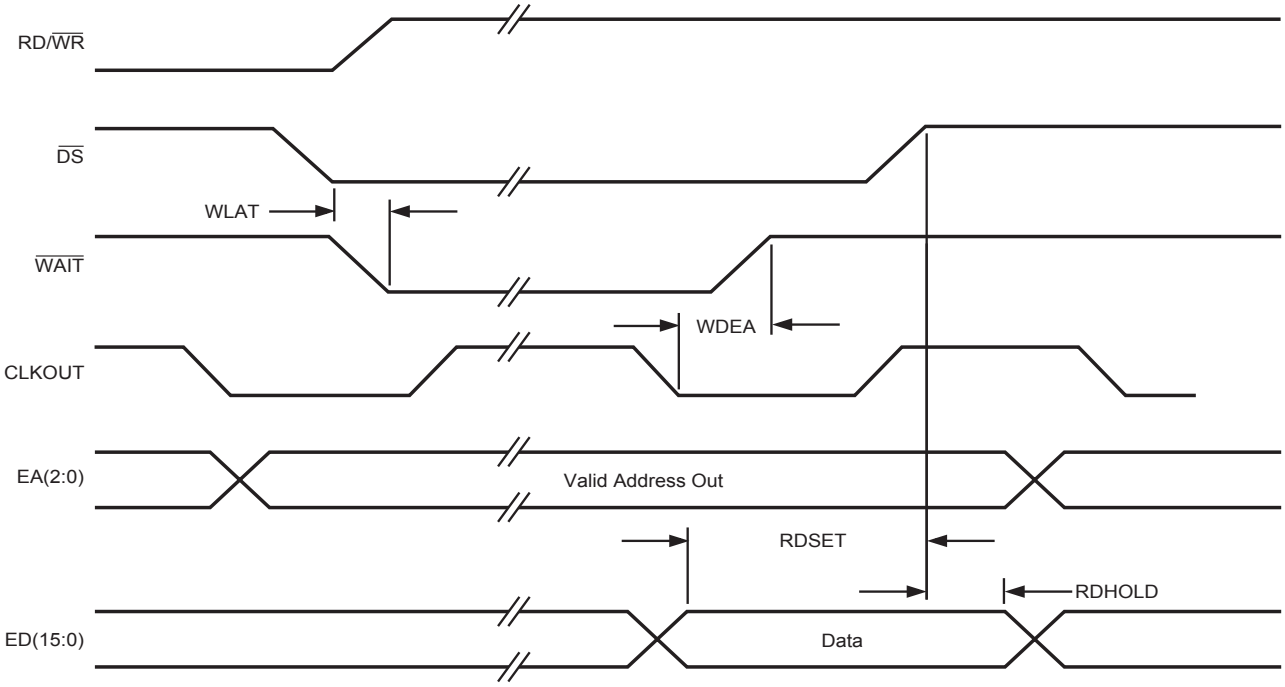


Figure 12. Read Timing Using $\overline{WAIT}$ Pin

TIMING DIAGRAMS (Continued)

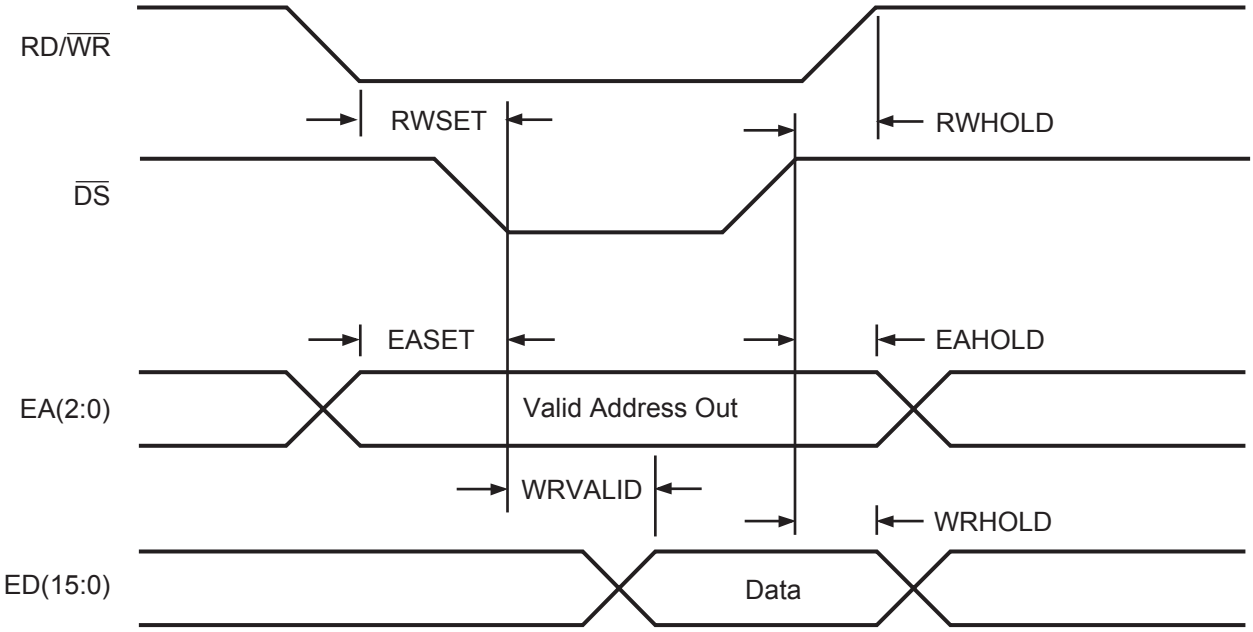


Figure 13. Write Timing

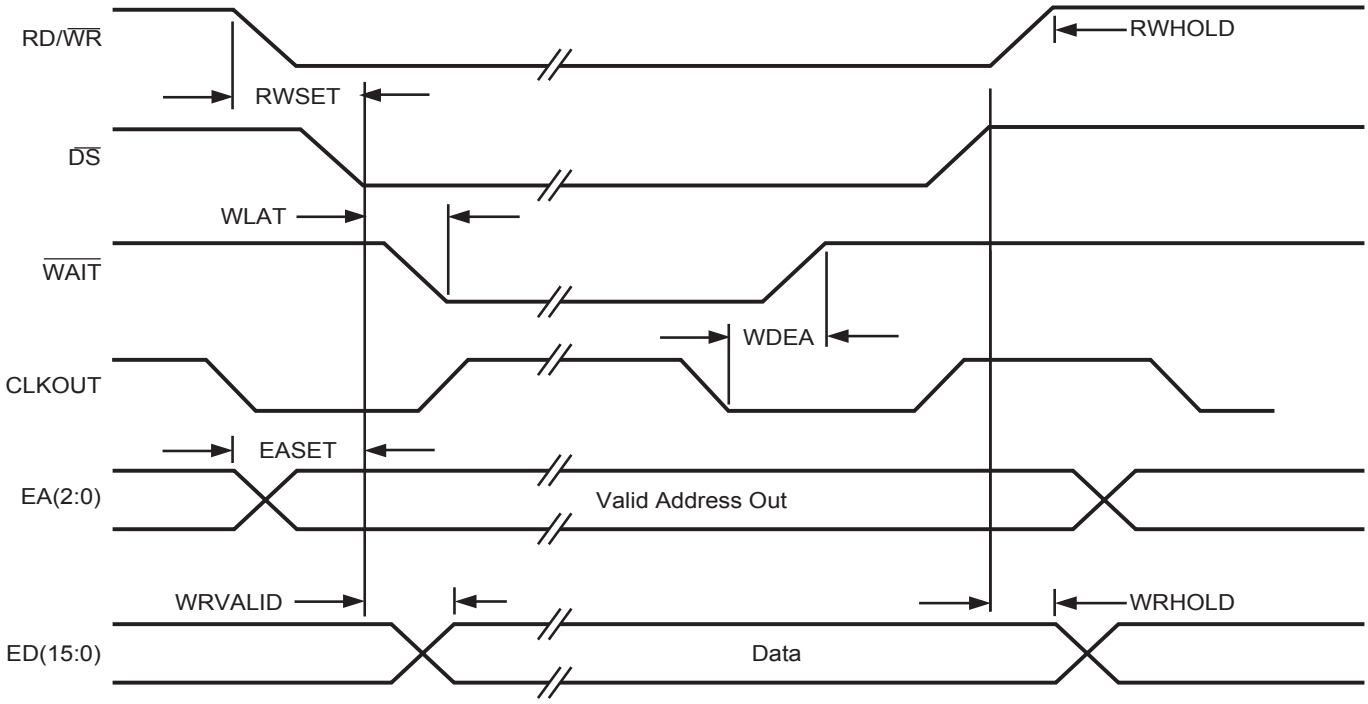
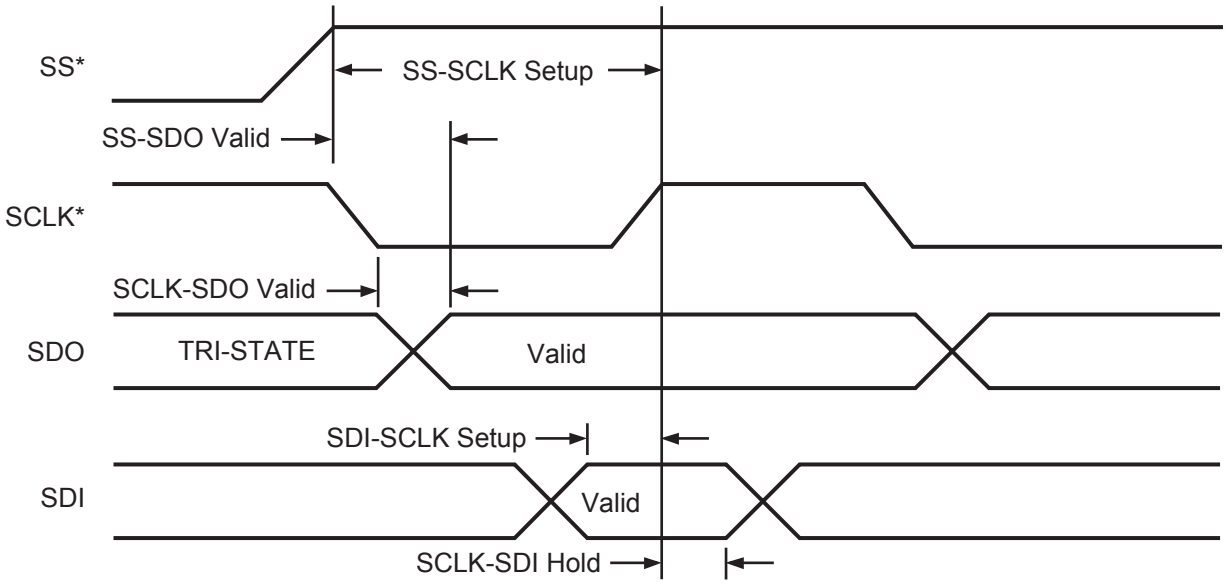


Figure 14. Write Timing Using WAIT Pin



*Notes: The polarity of SCLK and SS are programmable by the user. SS is used in Slave Mode only. This figure illustrates data transmission on the falling edge of SCLK, data reception on the rising edge of SCLK, with SS active Low (default).

Figure 15. SPI Timing (Master and Slave Modes)

FUNCTIONAL DESCRIPTION

Instruction Timing. Most instructions are executed in one machine cycle. A multiplication or multiply/accumulate instruction requires a single cycle. Long immediate instructions, and Jump or Call instructions, are executed in two machine cycles. Specific instruction cycle times are described in the Instruction Description section.

Multiply/Accumulate. The multiplier can perform a 16-bit x 16-bit multiply, or multiply/accumulate, in one machine cycle using the Accumulator and/or both the X and Y inputs. The multiplier produces a 32-bit result, however, only the 24 most significant bits are saved for the next instruction or accumulation. For operations on very small numbers where the least significant bits are important, the data should first be scaled to avoid truncation errors.

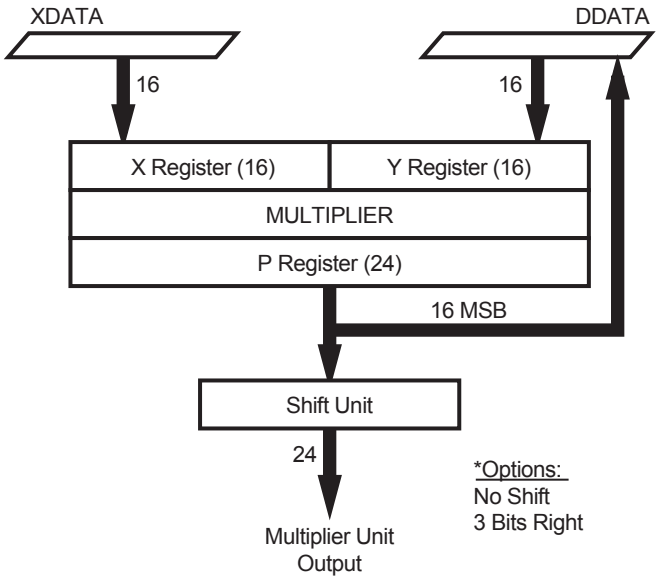


Figure 16. Multiplier Block Diagram

All inputs to the multiplier should be fractional two's-complement, 16-bit binary numbers, which places them in the range [–1 to 0.9999695]. The result is in 24 bits, so the range is [–1 to 0.9999999].

If 8000H is loaded into both the X and Y registers, the multiplication produces an incorrect result. Positive one cannot be represented in fractional notation, and the multiplier actually yields the result 8000H x 8000H = 8000H (–1 x –1 = –1). The user should avoid this case to prevent erroneous results.

A shifter between the P Register and the Multiplier Unit Output can shift the data by three bits right or no shift.

Data Bus Bank Switch. There is a switch that connects the X Bus to the DDATA Bus that allows both the X and Y registers to be loaded with the same operand for a one cycle squaring operation. The switch is also used to read the X register.

ALU. The ALU features two input ports. One is connected to the output of the 24-bit Accumulator. The other input selects either the Multiplier Unit Output or the 16-bit DDATA bus (left-justified with zeros in the eight LSBs). The ALU performs arithmetic, logic, and shift operations.

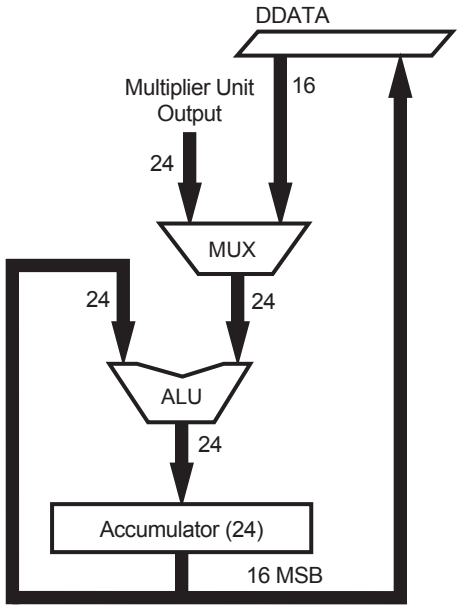


Figure 17. ALU Block Diagram

Hardware Stack. A six-level hardware stack is connected to the DDATA bus to hold subroutine return addresses or data. The CALL instruction pushes PC+2 onto the stack, and the RET instruction pops the contents of the stack to the PC.

User Inputs and Outputs. The Z893x3 features three User Inputs, UI0, UI1, and UI2. Pins UI0 and UI1 are connected directly to status register bits S10 and S11, and can be read, or used as a condition code in any conditional instruction. Pins UI0, UI1 and UI2 may also be used to clock the Counter/Timers. There are two user output bits, UO0 and UO1, which share pins with the timer outputs TMO0 and TMO1 on Port2. When the User Outputs are enabled, they are the complements of bits S5 and S6 of the Status Register.

Interrupts. The Z893x3 features three user interrupt inputs which can be programmed to be positive or negative edge-triggered. There are five interrupts generated by internal peripherals: the A/D converter, the Serial Peripheral Interface, and the three Counter/Timers. Internally there are three priority levels. The internal signals for Interrupt service Requests are denoted ISR0, ISR1, and ISR2, with ISR0 having the highest priority, and ISR2 the lowest. The user can program which interrupt sources are enabled, and which sources are serviced by the highest, middle, and lowest priority service routines. An interrupt is serviced at the end of an instruction execution. Two machine cycles are required to enter an interrupt instruction sequence. The PC is pushed onto the stack. The Interrupt Controller fetches the address of the interrupt service routine from the following locations in program memory:

Device	ISR0	ISR1	ISR2
Z89223/273/323/373	1FFFH	1FFEH	1FFDH

At the end of the interrupt service routine, a RET instruction is used to pop the stack into the PC.

The Set-Interrupt-Enable-Flag (SIEF) instruction enables the interrupts. Interrupts are automatically disabled when entering an interrupt service routine. Before exiting an interrupt service routine the SIEF instruction can be used to reenable interrupts.

Registers. In addition to the internal registers for processing, control, and configuration, the Z893x3 offers up to seven user-defined 16-bit external registers, EXT0–EXT6, depending on the Register Bank Select value. The external register address space is shared by the Z893x3 internal peripherals. Selecting banks 0–4 of the EXT Register Assignment allows access to/from three to seven of these addresses for general-purpose use.

I/O Ports. The Z893X3 DSP family features a user-configurable I/O structure. Most of the I/O pins include dual functions. The Counter/Timer, Serial Peripheral Interface, and External Interrupt Enables determine whether a pin is dedicated to peripheral or I/O port use.

Port0. A 16-bit user I/O port. Bits can be configured as input or output or globally as open-drain output. When enabled, Port0 consumes the 16 data lines used by the ED bus. Port0 function and ED bus use can be dynamically alternated by enabling and disabling Port0.

Port1. A multifunctional 8-bit port. Bits can be configured as input or output or globally as open-drain output. Port1 also supports INT2, CLKOUT, the Serial Peripheral Interface, and User Inputs 0 and 1.

Port2. A multifunctional 8-bit port. Bits can be configured as input or output or globally as open-drain output. Port2 also supports INT0 and INT1, all three Counter/Timer outputs, ED Bus, $\overline{WAIT}$, and UI2.

Port3. Port3 is an 8-bit user I/O port with 4 bits of input and 4 bits of output. It is available only on the 80-pin package.

External Register Usage. The external registers EXT0–EXT6 are accessed using the External Address Bus EA2–EA0, the External Data Bus (ED Bus) ED15–ED0, and control signals $\overline{DS}$, $\overline{WAIT}$, and RD/$\overline{WR}$. These provide a convenient data transfer capability with external peripherals. Data transfers can be performed in a single-cycle. An internal wait state generator is provided to accommodate slower external peripherals. A single wait state can be implemented through control register Bank15/EXT3. For additional wait states, the $\overline{WAIT}$ pin can be used. The $\overline{WAIT}$ pin is monitored only during execution of a read or write instruction to external peripherals on the ED bus.

Wait-State Generator. An internal Wait-State generator is provided to accommodate slow external peripherals. A single Wait-State can be implemented through a control register. For additional states, a dedicated pin ($\overline{WAIT}$) can be held Low. The $\overline{WAIT}$ pin is monitored only during execution of a read or write instruction to external peripherals (ED bus).

Analog to Digital Converter. The A/D Converter is a 4-channel, 8-bit half-flash converter. Two external reference voltages provide a scalable input range. The A/D sample rate is determined by a prescaler connected to the system clock. An interrupt is optionally generated at the end of a conversion. The four input channels can be programmed to operate on demand, continuously, or upon an event (timer or interrupt).

Counter/Timers (C/T0 and C/T1). These C/Ts are 16-bit with 8-bit prescalers. They also offer the option of being used as PWM generators and include both hardware and software Watch-Dog capabilities. Both C/Ts are identical and can be externally or internally clocked. Either C/T can drive TMO0 or TMO1. Either C/T can drive any of the three interrupt service requests (ISR0, ISR1, or ISR2).

Counter/Timer (C/T2). This C/T is 16-bits, externally or internally clocked, and can drive TMO2 and/or any of the three interrupt service requests (ISR0, ISR1, or ISR2).

Serial Peripheral Interface (SPI). The Serial Peripheral Interface provides a convenient means of inter-processor and processor-peripheral communication. It offers the capability to transmit and receive simultaneously. The SPI is designed to operate in either master or slave mode.