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Z89300 SERIES

DIGITAL TELEVISION CONTROLLERS

FEATURES AND BENEFITS

- Advanced TV controller IC with sophisticated On-Screen Display capability and integral VBI data decoding.
- 40-pin DIP, 42-pin shrink DIP and 52-pin shrink DIP versions with ROM sizes varying from 10K words to 24K words provide application diversity.
- 40-pin DIP, 42-pin SDIP and 52-pin SDIP OTP versions enable easy development and flexible small scale production.
- 16-bit single cycle RISC core provides very fast instruction throughput.
- I.R. (Infrared) remote capture register facilitates reliable capture of remote data even in high noise environments.
- 6-channel, 4-bit ADC (Analog to Digital Converter) supports multiple tuner AFT, analog keypad entry, audio level input and VBI (Vertical Blank Interval) data capture. Subsequent digital processing of VBI data results in excellent signal to noise ratio performance.
- Up to 10 PWM (Pulse Width Modulator) outputs allow low cost digital to analog conversion (with addition of external low pass filter circuits). Eight PWM's have 8-bit resolution for control of video and audio attributes. Two PWMs have 14-bit resolution to optionally control external VST (Voltage Synthesis Tuner).
- Master/slave I^2C (Inter Integrated Circuit) Philips Standard Serial Interface provides serial system interconnect to common peripheral functions.
- Bit programmable I/O ports provide flexibility for miscellaneous digital input/output functions.
- 24.0 MHz nominal PLL (Phase Lock Loop) controlled oscillators provide stable system and video clocks. Only one external capacitor is required for the loop filter function. A 32 kHz oscillator is used for reference.
- Hsync, Vsync and Composite sync generation circuits provide a video timebase (typically for VCR and set-top applications) in the absence of an available video signal.
- Micro-programmable OSD (On-Screen Display) generation logic provides ultimate flexibility to tailor OSD features and functions. In addition to normal OSD functions Closed-Captioning is supported in accordance with FCC Report and Order on GEN Docket No. 91-1, dated April 12. 1991. EDS and StarSight Telecast, Inc. on-screen TV program guide capability can be implemented as well with the 89300.
- High definition characters offer the ability to display complex characters.
- Program and character generator data contained in the one ROM space-simplifies mask ROM code submission and gives flexibility in size of character ROM. Up to 512 characters with 16x16, 16x18 or 16x20 programmable matrix
- ICEBOX™ Emulator provides in-circuit emulation for program debug.
- Zilog supplied ATB (Application Tool Box) software provides microcode support for VBI data capture, I.R. remote data capture, and OSD display including specific requirements of Starsight and Closed Captioning.

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DEVICE IDENTIFICATION AND SUMMARY

Zilog's Z893xx family of television controller products combine On-Screen Display and VBI data capture functions to provide a highly integrated solution for TV, VCR and set-top applications. Family members serve as either stand-alone controllers providing the most cost effective central processing facility or as add-on controllers where time-to-market is a key factor. Common to all devices is a high-speed 16-bit RISC controller that provides ultimate OSD flexibility and allows for digital VBI data capture. The power of the Z893xx family architecture is evident by it's ability to support a variety of OSD applications including Line 21 closed-caption, EDS and Starsight. Table 1 summarizes the features of the devices in the family.

In Circuit Emulation is facilitated by the Z89309 124-pin PGA device. The Z89332/6 are 24K/12K ROM variants in 42-pin SDIP package.

One Time Programmable versions of the parts Z89300/ Z89331, are offered for development and small scale production.

The Z89302, Z89303, Z89304, Z89305, Z89306 and Z89307/8/13/14 are mask ROM devices intended for high volume TV chassis production applications. They offer 40-pin, DIP and 52-pins DIP package configurations with 10K, 12K word, 16K word, and 24K word program memory sizes.

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Table 1. Zilog Z893xx Product Family

Device	Application	Feature Summary							
		ROM (word)	RAM (word)	Pkg.	I^2C	IR Capture	ADC	Bit I/O	PWM
Z89300	TV Receiver Controller OTP	24K OTP	640	40-DIP	Yes	Yes	3-ch	19	7
Z89301	TV Receiver Controller OTP	24K OTP	640	50-SDIP	Yes	Yes	4-ch	26	9
Z89309	TV Receiver Controller ICE device	Bond Out	640	124 PGA	Yes	Yes	6-ch	26	10
Z89302	TV Receiver Controller	24K Mask	640	40-DIP	Yes	Yes	3-ch	19	7
Z89303	TV Receiver Controller	24K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89313	TV Receiver Controller	24K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89304	TV Receiver Controller	16K Mask	640	40-DIP	Yes	Yes	3-ch	19	7
Z89305	TV Receiver Controller	16K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89306	TV Receiver Controller	12K Mask	640	40-DIP	Yes	Yes	3-ch	19	7
Z89307	TV Receiver Controller	12K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89331	One Time Programmable	24K OTP	640	42-SDIP	Yes	Yes	5-ch	20	7
Z89332	TV Receiver Controller	24K Mask	640	42-SDIP	Yes	Yes	5-ch	20	7
Z89336	TV Receiver Controller	12K Mask	640	42-SDIP	Yes	Yes	5-ch	20	7
Z89314	TV Receiver Controller	16K Mask	512	40-DIP	No	Yes	3-ch	19	7
Z89318	TV Receiver Controller	10K Mask	512	40-DIP	No	Yes	3-ch	19	7

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FUNCTIONAL DESCRIPTION

Capture Function

The capture function is intended for Infrared Remote data capture. It employs a capture register that holds the time value from one transition of I.R. data to the next.

The CPU can periodically check the capture status and read the value if a new capture has occurred. Subsequent decoding and command passing of the received I.R. signal is under program control.

Pulse Width Modulator Function

Pulse Width Modulation is used in conjunction with external low pass filters to perform digital to analog conversion. Eight PWM's of 8-bit resolution each find application in generating 0-12 volt signals for control of video and sound attributes. Two 14-bit resolution PWMs may be used with external circuits to generate the controlling voltage for voltage synthesis tuners. In the case of the chassis employing a frequency synthesis tuner, this PWM may also control video or sound attributes.

Each PWM circuit has a data register whose content are set under program control. The data in the register determines the ratio of PWM high to PWM low time.

Analog to Digital Converter Function

This function employs a 4-bit resolution, flash A to D converter. A six to one input multiplexor and conversion start circuits are controlled by the user program. The 4-bit conversion result is available to be read by the CPU at the end of each conversion.

One input channel (ADC0) is dedicated for quantizing VBI (vertical blank interval) data for subsequent digital signal processing. The other channel (ADC5) is typically used for V-SYNC separation from the composite TV signal. These channels have a special video clamp circuit that provides DC restoration of the composite video input signal. Typical VBI applications include Line 21 Closed-Caption, Electronic Data Services and Starsight Telecast. The range of ADC0 and ADC4 is 0.5V p-p from 1.5V to 2.0V.

The remaining four channels are general-purpose. They are typically used for implementation of tuner automatic frequency control and analog key entry. The range of ADC1/2/3/4 is from 0V to 5.0V.

Port Functions

Two input/output port blocks are available for general-purpose digital I/O application. Each port bit is programmable to be either input or output. To conserve device pin count, some port pins are mapped to provide I/0 to the A to D converter block and I^2C interface block.

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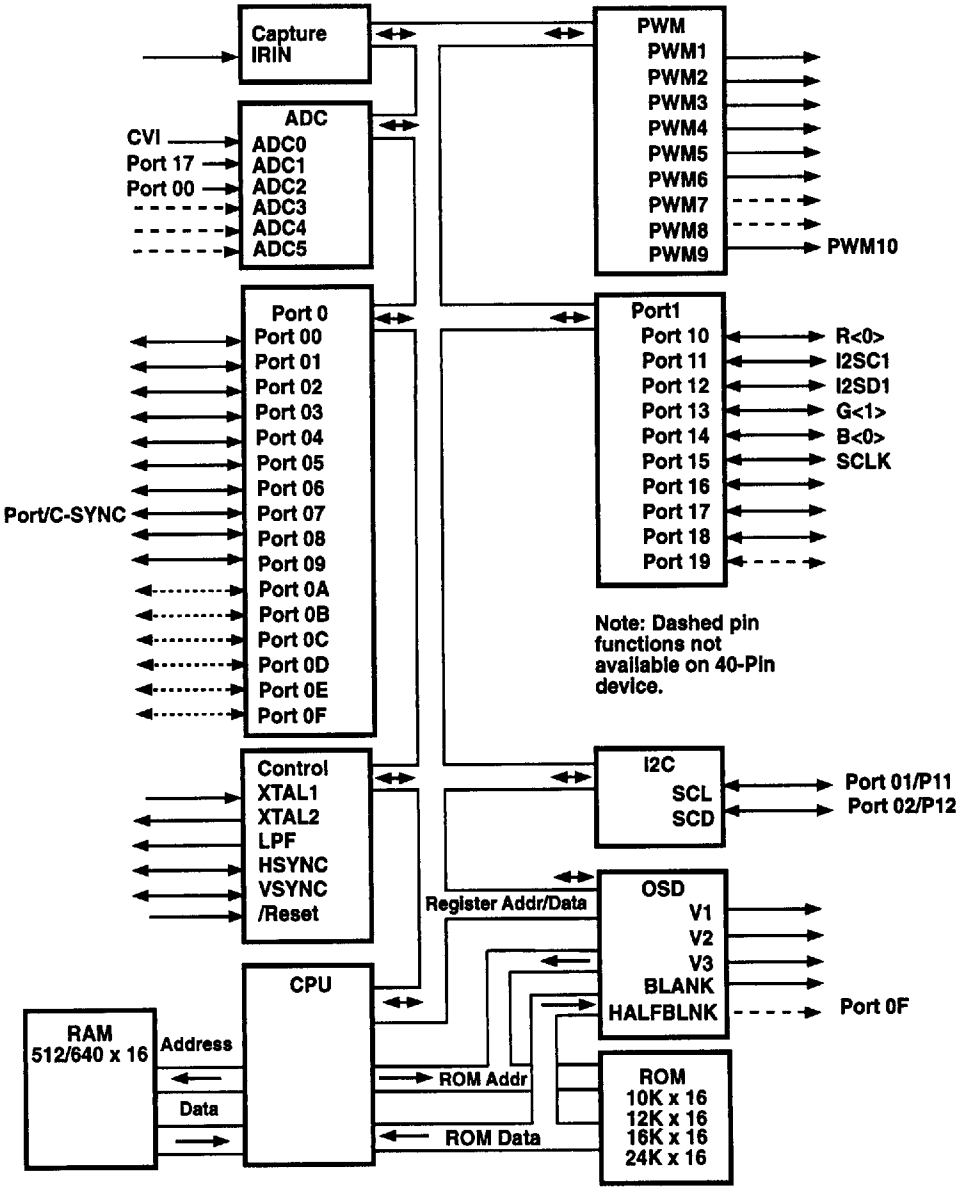

Figure 1. Z89300 Functional Block Diagram

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PIN DESCRIPTION

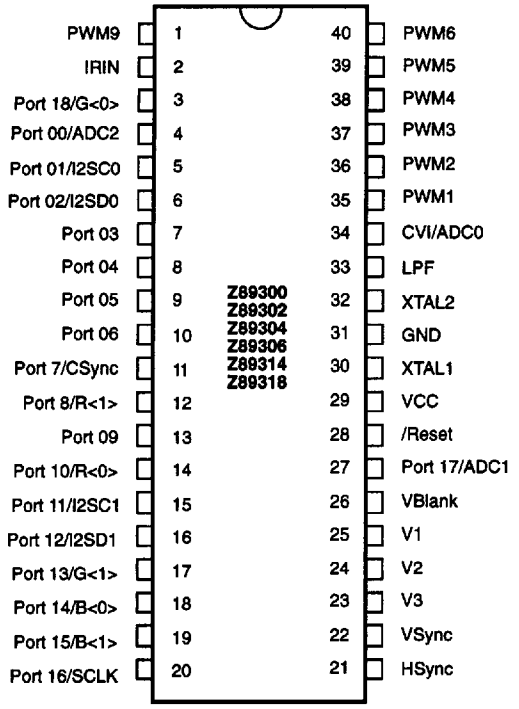

Figure 2. Z89300/02/06 40-Pin DIP

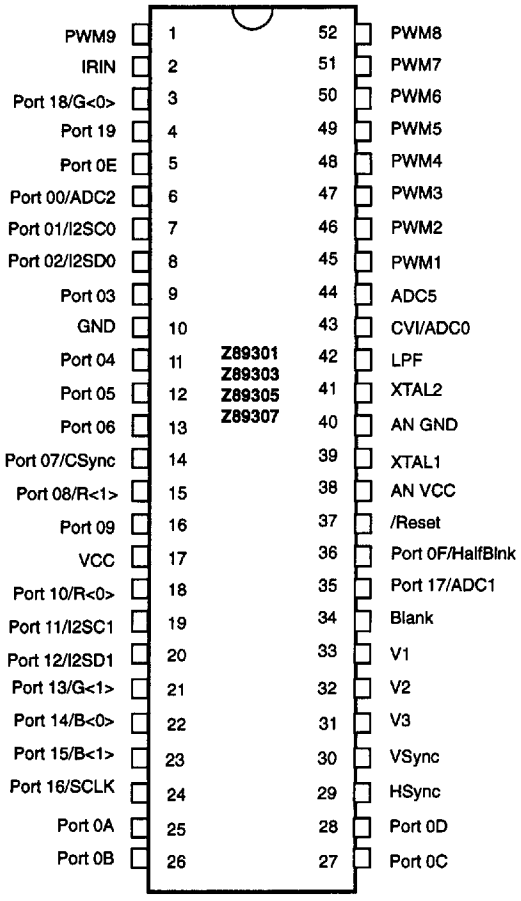

Figure 3. Z89301/03/07 52-Pin DIP

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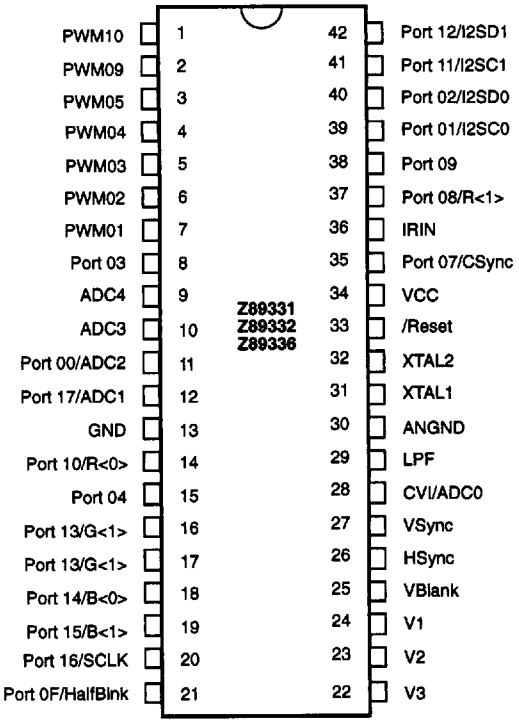

Figure 4. Z89332/336 42-Pin DIP

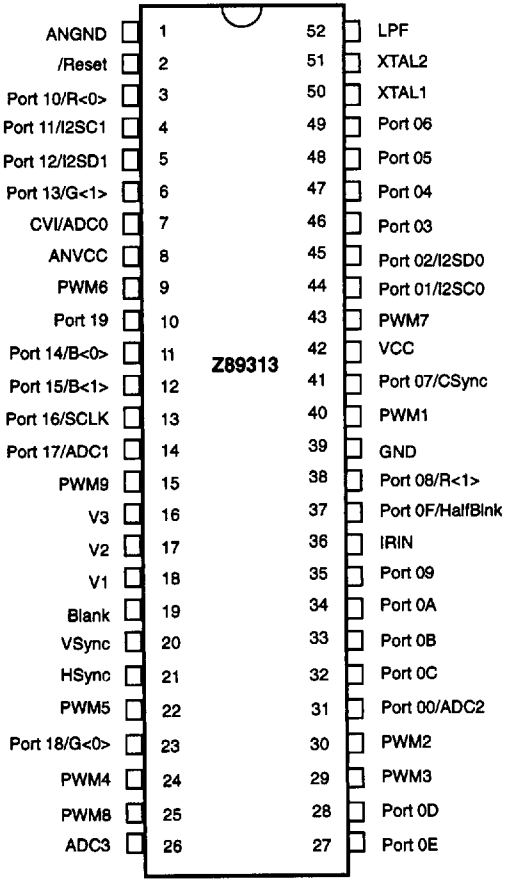

Figure 5. Z89313 52-Pin DIP

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PIN IDENTIFICATION

Table 2. Pin Identification

Pin		Package				Configuration	
Name	**Function**	**Z89301/3/5/7 52-pin SDIP**	**Z89313 52-pin SDIP**	**Z89300/02/4/6 14/18 40-pin DIP**	**Z89331/332 /336 42-pin DIP**	**Direction**	**Reset**
VCC	+5 Volts	17,38	8,42	29,–,	34	PWR	–
GND	0 Volts	10,40	1,39	31,–,	13,30	PWR	–
IRIN	Infrared Remote Capture Input	2	36	2	36	I	I
ADC [5:0][1]	4-Bit Analog to Digital Converter input[2].	44,–,–,6, 35,43	–,–,26,31 14,7	–,–, –, 4,27 34	–, 9,10, 11,12,28	AI	I
PWM10, PWM9	14-Bit Pulse Width Modulator Output	–,1	–,15	–,1	1,2	OD	0
PWM[8:1][3]	8-Bit Pulse Width Modulator Output	52,51,50,49, 48,47,46,45	25,43,9,22, 24,29,30,40	–,–.40,39. 38,37,36,35	–,–, –,3,4, 5,6,7	OD	0
Port0[F:0][4]	Bit Programmable Input/Output Ports	36,5,28,27, 26,25,16,15, 14,13,12,11, 9,8,7,6	37,27,28,32, 33,34,35,38, 41,49,48,47, 46,45,44,31,	–,–,–,–,–,–, 13,12,11, 10,9,8,7, 6,5,4	21,–,–,–, –,–,38,37, 35,–,–,15, 8,40,39,11	B	I
Port1[9:0][5]	Bit Programmable Input/Output Ports	4,3,35,24, 23,22,21, 20,19,18	10,23,14, 13,12,11, 6,5,4,3	–,3,27, 20,19,18, 17,16,15, 14	–,16,12, 20,19,18, 17,42,41, 14	B	I
SCL[6]	I^2C Clock I/O	7 or 19	44 or 4	5 or 15	39 or 41	BOD	
SCD[7]	I^2C Data I/O	8 or 20	45 or 5	6 or 16	40 or 42	BOD	
XTAL1	Crystal oscillator input	39	50	30	31	AI	I
XTAL2	Crystal oscillator output	41	51	32	32	AO	0
LPF	LOOP FILTER	42	52	33	29	AB	0
HSYNC	H_SYNC	29	21	21	26	B	I
VSYNC	V_SYNC	30	20	22	27	B	I
/Reset	Device Reset	37	2	28	33	I	I
V[3:1]	OSD Video Output. Typically Drive B, G and R Outputs.	31,32,33	16,17,18	23,24,25	22,23,24	0	0
Blank	OSD Blank Output	34	19	26	25	0	0
HalfBlank[8]	OSD Half Blank Output	36	37	–	21	0	
RGB digital outputs[9]	R[1:0], G[1:0] and B[1:0] Outputs of the RGB Matrix	23,22,21, 20,19,18	12,11,6,5, 4,3	19,18,17,[11] 16,15,14	37,14,17, 16,19,18	0	
SCLK [10,11]	Internal Processor SCLK	24	13	20	20	0	
SCLK [11]	Internal Processor SCLK	–	–	–	L1	0	0
/IE	Data Strobe	–	–	–	K1	0	0
R/W	Read/Write	–	–	–	J3	0	0
EA[2:0]	External Registers Address Bus	–	–	–	L2,K3,H1	0	0

Notes:

1 ADC1 input pin is shared with Port 17, ADC2 input pin is shared with Port 00. ADC3 and ADC4 are not available on 40-Pin DIP version.
2 ADC0 and ADC4 have a clamp circuit that facilitates Composite Video input
3. PWM[8,7] is not available on the 40-Pin DIP version.
4 Port 0 [F.A] is not available on the 40-Pin DIP version
5 Port 19 is not available on the 40-Pin DIP version
6 SCL I/O pin is shared with Port 01 or Port 11
7. SCD I/O pin is shared with Port 02 or Port 12
8 HalfBlank output is a function shared with Port 0F HalfBlank output is not available on the 40-Pin DIP version
9. Digital RGB outputs and the internal SCLK are shared with Port 1 [5:0]
10. Internal processor SCLK is shared with Port 16
11 Not available on Z89314

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GENERAL DESCRIPTION

The Z89300 Digital Television Controller is an application specific controller designed to provide compete audio and video control of television receivers and video recorders, and advanced on-screen display facilities.

System Description

Table 1 shows a typical application of the Z89300 Digital Television Controller as an embedded controller in a television receiver. It provides the ability to decode closed caption transmissions and display characters on the screen. Analog and digital control circuits can be manipulated. Keypad and infrared signals can be monitored directly. The Z89300 can also receive and provide vertical and horizontal synchronization signals.

In a typical system, normal transmission is received and demodulated, the CRT display is controlled by the signals received from the color decoder and deflection unit. In order to display characters generated by the Z89300, a video multiplexor must be provided which enables the CRT display's RGB signals and synchronization to be controlled by the video outputs from the processor. When the controller needs to display a character on the screen, the multiplexor is switched and the processor's video signals appear on the display.

The analog composite video signal is fed directly to the analog to digital converter on the chip, which is then decoded to extract the closed caption text embedded in the video signal. The characters received are generated as video signals and are then passed to the display.

When a detectable composite video signal is received the deflection unit extracts the horizontal and vertical synchronization signals and passes them to the CRT deflection plates as well as to the Z89300. The controller uses these signals to align its video signals with those of the normal display. In the case where the composite video signal is not present, video synchronization is able to be provided by the controller. In this case, the SYNC signal pins are set to be outputs and they are then fed to the deflection unit, which then controls the display. The SYNC generators can be configured to provide either H-SYNC and V-SYNC, or H-FLYBACK and V-FLYBACK.

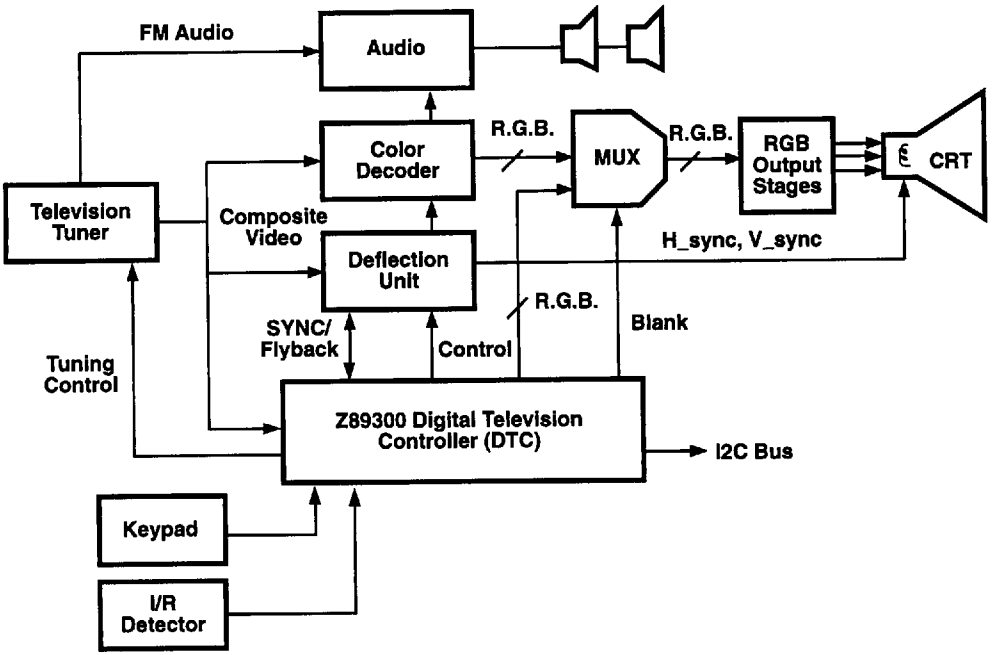

Figure 6. Z89300 Digital Television Controller System Application

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System Description (Continued)

Analog functions such as volume and color controls can be controlled by the pulse width modulated outputs from the Z89300. Other digital controls such as channel fine tuning can be controlled through the serial I²C bus.

An infrared remote control receiver can be directly decoded through the capture register, and keypad input can be scanned by directly controlling I/0 pins as keyscan ports.

The processor clock is provided by referencing an internal phase locked loop to an external 32.768 kHz crystal oscillator, which enables EMI emissions from the clock circuitry to be minimized. The internal system clock frequency can be software selected to be up to 12.059 MHz in normal operation or 32.768 kHz in low power mode. The Z89300 can also be placed in STOP mode, suspending processor clocking for power down suspension of operation.

Program, display and character graphics memories are on the chip, eliminating the need for any external memory components. Characters can be displayed as two or three times normal size. Smoothing and fringing circuits are provided to enhance display appearance.

The device is available in a one-time-programmable version as well as a 12K, 16K and 24K masked ROM sizes and is available in 40 and 52-pin DIP packages

FUNCTIONAL DESCRIPTION

Core Processor

The processor core is a high-performance RISC processor.

The powerful 12 MHz Z89C00 RISC processor core allows the user to control the on-board peripheral functions and registers using the standard processor instruction set.

The Z89300 controller processor core is a Z89C00 high performance 16-bit RISC processor optimized for data processing and transfer. 16-bit peripheral registers are programmed to control the operation of the peripheral devices. Two banks of 256 words each of RAM in the processor core can be used for video character sequence storage. Program and character graphics are stored in the PROM.

External Registers

The C00 module is capable of directly accessing up to eight external registers using only the three external register address signals that are normally available. In this implementation, two user signals are combined with the register address signals to provide the ability to address four banks of eight registers each. The most speed critical registers are located together in bank 3. In this document all external registers will be referred to as follows:

RX(Y)<Z>;
where - X is a register number within a register bank;
Y is a bank number;
Z is a bit field number

The user can select a register by setting the user bits to define the bank that the register is in and then specifying the address of the register on the external register address bus.

The external registers reside on the chip and are used to control the operation of all of the peripheral modules of the device. By reading or writing to the fields in the external registers the user can interact with the peripheral devices of the chip.

Interrupt Control

The Z89C00 core has three external interrupt signals that are used to provide interrupt signalling from the Z89300 peripheral modules to the core. In order to provide handling of all four of the device's interrupt sources, that is, horizontal sync (H-SYNC), vertical sync (V-SYNC) and the two timers (1s/CAP), the latter interrupt source is treated as a vectored interrupt where the vector is a bit in a register that selects one of the two timers. The more critical synchronization interrupts are non-vectored.

Interrupt priorities are programmable and each interrupt can be masked by setting fields in the external registers.

The timer interrupts are wire ORed to a single interrupt input. When a timer generates an interrupt it sets the condition of the interrupt vector flag depending on which timer initiated the interrupt request. When the processor is ready to service the interrupt request, it reads the vector bit and executes the appropriate service routine.

When the Z89300 receives an interrupt request from one of the non-vectored interrupt sources it directly executes the interrupt service routine for that source.

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Programmable Read Only Memory

The programmable ROM is designed to provide storage for both program memory PROGRAM and character set graphics pixel arrays (CGROM). The address boundaries between these applications is dependent on the storage required for character graphics.

The program ROM section can in theory be accessed anywhere in the addressable ROM space. However, since CGROM usually start at location 0000h, PROGRAM will reside in the higher address locations. The maximum available ROM space for program memory depends on the ROM reserved for CGROM for an application and the ROM size of the device selected. Memory accesses can be considered to be PROGRAM accesses when the ROM address is being provided by the processor ROM address bus.

The Z89300 ROM is either 10K, 12K, 16K or 24K words, depending on the part selected. The first byte of ROM is located at address 0000h, and is mapped as shown in Table 3.

Table 3. PROM Addressing

ROM Size (Words)	Low Address	High Address
12K	000h	2FFFh
16K	000h	3FFFh
24K	000h	5FFFh

The address multiplexor can be selected so that either the processor external address bus or the character registers provide the physical ROM address. For PROGRAM access the processor external address bus should be selected, otherwise the access is to CGROM space.

Clocks and Control

The Z89300 has two internal 12 MHz VCOs (PVCO - primary VCO &SVCO - Secondary - VCO) that are referenced to a 32 kHz internal oscillator to provide the system clock (SCLK). SCLK is generated internally by dividing the frequency of an appropriate oscillator (PVCO or SVCO) by 2. The frequency of the SCLK after POR is 12.058 MHz. In SLEEP mode the controller uses the 32 kHz clock for the system clock to reduce power consumption. The processor can be suspended by placing it into STOP mode when main power is not available for minimal power consumption.

An external crystal controls the internal 32 kHz oscillator, and is used as the clock source for the internal 24 MHz phase locked loop. The PLL provides the internal 12 MHz system clock for processor operation.

On-Screen Display

The extensive character attributes can be controlled in two modes by the on-screen display controller: character control mode for maximum display control flexibility and closed caption mode for optimum display of closed caption text.

Character control mode provides access to the full set of attribute controls. Each word of RAM specifies a single displayed character and basic character attributes, allowing the modification of attributes on a character-by-character basis. The insertion of control characters allows control of other character attributes.

The fully customizable 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes, including underlining, italics and blinking, eight foreground and background colors, character position offset delay, and background transparency. The 16-bit display character representation allows the modification of some key attributes on a character by character basis. A character's pixel array is stored as a 16,18 or 20 word representation in Character Graphics ROM (CGROM). The ROM contents are referenced by a 16-bit word stored in video RAM (VRAM) defining the character type and its key attributes.

Additional hardware provides the capability to display two and three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Fringing circuitry can be activated to improve the visibility of text by surrounding the character lines with a one pixel border.

RGB outputs provide the direct video signals, and a blanking output is provided to control the video multiplexor. Dot clock and vertical line synchronization is normally obtained from H_FLYBACK and V_FLYBACK, but can be generated by the Z89300 and driven to the external deflection unit through the bi-directional SYNC ports when external video synchronization signals are not present.

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Character Generation ROM

The required Character Graphics ROM size is dependent on the number of characters that are stored in memory. CGROM always begins at address 0000h, the first byte of ROM. The CGROM is configured in two banks selectable by setting a control bit. Each bank provides up to 256 characters with 16x16, 16x18 or 16x20 pixels matrix. Absolute maximum CGROM size is 9K words (9210 words).

Each character's pixel array is represented as 16 or 18 words of ROM storage,. Each word is 16 bits long. Pixel lines 1 to 16 are mapped sequentially to ROM addresses that are pointed to by the character pointer and a line number offset. In high resolution mode pixel lines 17 and 18 are offset to addresses beginning at the 4K boundary (1000h) for bank0 . Bank1 is mapped into ROM starting from address 1000h. Lines 17 and 18 of bank1 characters are mapped into ROM starting from address 2000h.

The first character in each bank should be a space character. In order to comply with the latter requirement it is recommended that bank0 character to be defined with 16x16 matrix. If the application requires bank0 characters to be in 16x18 pixel format, the first 32 characters of bank1 should be sacrificed and can't be used because line 17 and 18 of the bank0 characters will be mapped in their addresses and first eight characters of bank0 should not have any active dots in lines 17 and 18 in order to comply with the requirement that the first character in bank1 is a space character. For 16x20 format 32 characters need to be sacrificed.

In case, only bank0 of CGROM is used, there is no limitations on characters definition.

The CGROM data addressed by the contents of the character register is latched into the CGROM capture register. This contents of this register will contain a sequence of bits that represent whether the pixels on the pixel line currently being accessed for that character are on or off. This representation can be modified by the character multiplier to be two or three times normal character size by duplicating each bit in the word and expanding the representation to two or three of the character multiplier registers.

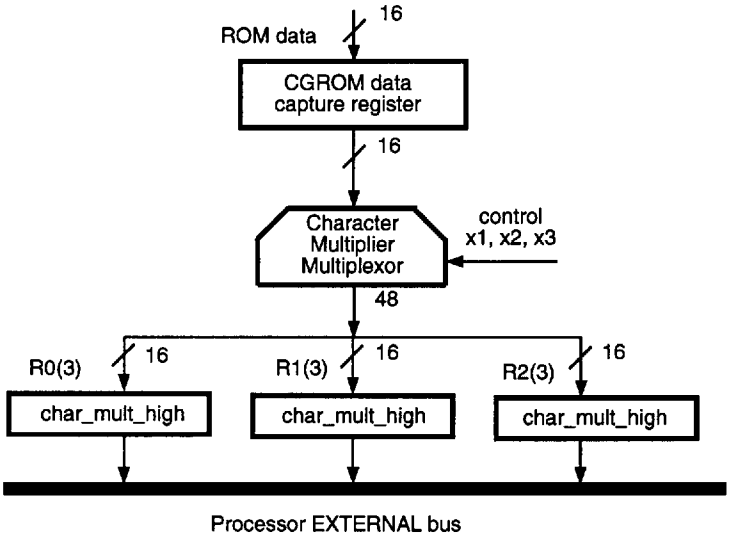

Figure 7. Character Multiplier

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Character Multiplier Multiplexor

The character multiplier multiplexor can be controlled to double or triple the size of the pixel line presented to it from the CGROM capture register. It does not perform a numerical multiplication. The bits of the word contained in the capture register are duplicated to enlarge the character as it would be displayed horizontally on the screen. A model of the operation of the character multiplier multiplexor is shown below:

Capture Register Contents	abcdefghijklmnop	abcdefghijklmnop	abcdefghijklmnop
	char_mult_high	char_mult_mid	char_mult_low
x1 operation			abcdefghijklmnop
x2 operation	aabbccddeeffgghh	iijjkkllmmnnoopp	
x3 operation	aaabbbcccdddeeef	ffgggghhhiiijjjkk	kllmmmnnnooopppp

Tuner Control

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices such as digital channel tuning adjustment may be accessed through the industry standard I^2C port.

Voltage synthesis tuning systems are supported by 14-bit PWM (PWM9/10).

Video and Sound Attribute Control

Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports and one 14-bit pulse width modulated port[1].

Two 14-bit and up to eight 8-bit pulse width modulated are available to provide PWM control of analog signal levels such as volume or color.

Vertical Blank Interval Data Capture

Closed caption text can be decoded directly from the composite video signal with the assistance of the processor's digital signal processing capabilities and displayed on the screen. The character representation in this mode allows for simple attribute control through the insertion of control characters, and each word of RAM specifies two displayed characters.

The 4-bit flash A/D converter provides the ability to directly receive the composite video signal and process the closed caption text embedded in the signal. Signal processing can be applied directly to the signal to improve decoder performance.

I/O Ports

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register.

Up to[2] 26 configurable I/O pins are general-purpose pins that can be utilized to provide functions such as serial data I/O, LED control, key scanning, power control and monitoring and I^2C serial data communications.

Notes:

1. All nine PWM ports are only available in the 52-pin package. In the 40-pin package only six 8-bit and one 14-bit PWM output pins are available
2. The 52-pin device has one 10-bit port and one 16-bit port. The 40-pin device has one 10-bit port and one 9-bit port.
3. The 42-pin device has two 14-bit PWMs and five 8-bit PWMs.

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REGISTERS

The register file of the Z893xx is organized in four banks selectable by writing bits 5 and 6 ("bank switch" bits) in Status Register of the Z89C00. All registers are mapped into an external register space of the Z89C00 RISC core and each bank consists of 8 registers. Status register is available for reading/writing any time. In order to access the register file, the appropriate bank of registers should be switched on. It is responsibility of the S/W to keep track on which register bank is accessible at any time.

Table 4. Bank Switching

Bank	Status Reg.	Bank Functionality
Bank 0	xxxx xxxx x00x xxxx b	I/O ports, I2C interface, PLL frequency, PWM9, PWM10- 14-bit
Bank 1	xxxx xxxx x01x xxxx b	Control registers
Bank 2	xxxx xxxx x10x xxxx b	PWM1..PWM8-8-bit
Bank 3	xxxx xxxx x11x xxxx b	OSD, palette control

Bank 0 (I/O Ports, I2C Interface, PLL Frequency, PWM9)

Table 5. Register0 - R0(0) PWM9 Data Register

Reg field	Bit position	R	W	Data	Description
Port/PWM	f---------------	R	W	1 0	Output port mode Output PWM mode (push-pull)
Port_data	-e--------------	R	W	x	Output data in Port mode
PWM_data	--dcba9876543210	R	W	xxx	Output data in PWM mode

Port/PWM bit defines the mode of the PWM9 output. When set to a "1" the PWM9 output monitors the data specified by the Port_data field. Otherwise the PWM_data field defines the waveform on the PWM9 pin.

Table 6. Register1 - R1(0) PWM10 Data Register

Reg field	Bit position	R	W	Data	Description
Port/PWM	f---------------	R	W	1 0	Output port mode Output PWM mode (push-pull)
Port_data	-e--------------	R	W	x	Output data in Port mode
PWM_data	--dcba9876543210	R	W	xxx	Output data in PWM mode

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Table 7. Register2 - R2(0) PLL Frequency Data Register

Reg field	Bit position	R	W	Data	Description
Port/PWM	fedcba98--------	R W			Return"0" No effect
PLL_data	--------76543210	R	W	xx	PLL divider = 256 + xx

The VCO, DOT and SCLK frequency are defined as

Fvco = Fdot = Fsclk = 32 kHz x (256 + PLLdata)

Upon POR the PLL frequency data register is preset to %70, which corresponds to the VCO frequency of 12.058 MHz.

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REGISTERS (Continued)

Table 8. Register3 - R3 (0) I2C Interface Register

Reg field	Bit position	R	W	Data	Description
Command	fedc----------	R			Return"0"
			W	%DD	See footnote below the Table
Reset	----b----------	R			Return "0"
			W	1	Reset the I2C interface
				0	No effect
HI/LO_ Speed	-----a----------	R	W	1	High speed (400 kHz) - implemented in Rev. BA
				0	Low Speed (100 kHz)
Slave_ mode	------9---------	R		1	Slave mode
			W	0	Master mode
					No effect
Busy	-------8--------	R		1	I2C interface is busy
			W	0	I2C interface is idle
					No effect
Data	--------76543210	R		xx	Received data
			W	xx	Data to be sent

Master Mode

0000 - Send start bit followed by address byte <Data>
0010 - Send data byte specified in <Data>
0100 - Send <7> as an Ack to Slave after Data byte was received **IN READ FRAME** and receive next Data byte.
0110 - Send <7> as an Ack to Slave, do nothing
1001 - Set Slave address defined in <Data> (BE PREPARED FOR SLAVE MODE)
1100 - Receive Ack from Slave after Address byte was transmitted IN READ FRAME If Ack=0, receive Data, else (Ack=1) do nothing.
1110 - Send stop bit
0011,0101,0111,10xx,1101,1111 - RESERVED COMBINATIONS (SHOULD NOT BE USED).

Slave Mode

0010 - Send <Data> **IN READ FRAME** then latch Master's Ack
0100 - Send <7> = 0 as an Ack **IN WRITE FRAME.**
1110 - Send <7> -1 as an Nak **IN WRITE FRAME** OR Send <7> as an Ack **IN READ FRAME** If <7>=0, "Send <Data>" **IN READ FRAME** command should be executed next, else (<7>!=0) release the bus.
1001 - Set Slave address defined in <Data>
ALL THE RESET COMBINATIONS ARE RESERVED AND SHOULD NOT BE USED.

The received data is available for reading only when the "busy" bit is reset to "0". Upon POR the speed of the I2C interface is set to "low".

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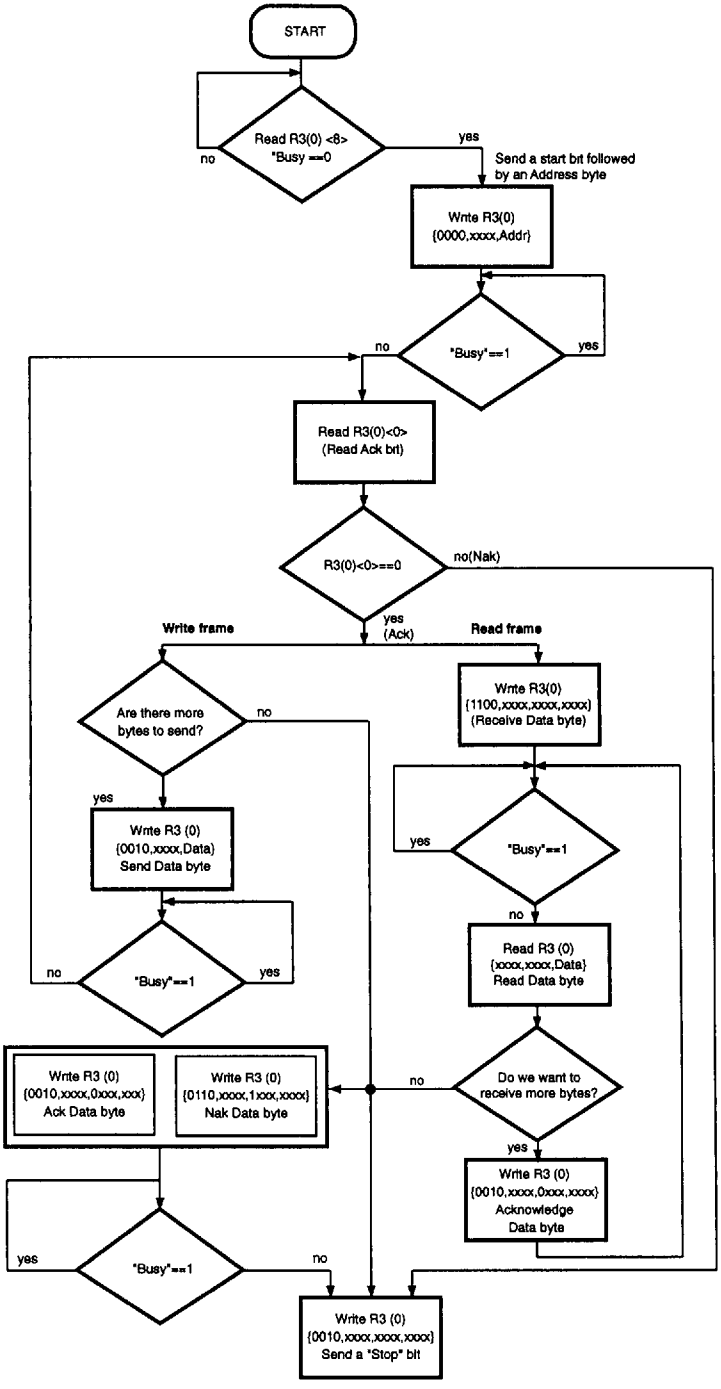

Figure 8. Master Mode

REGISTERS (Continued)

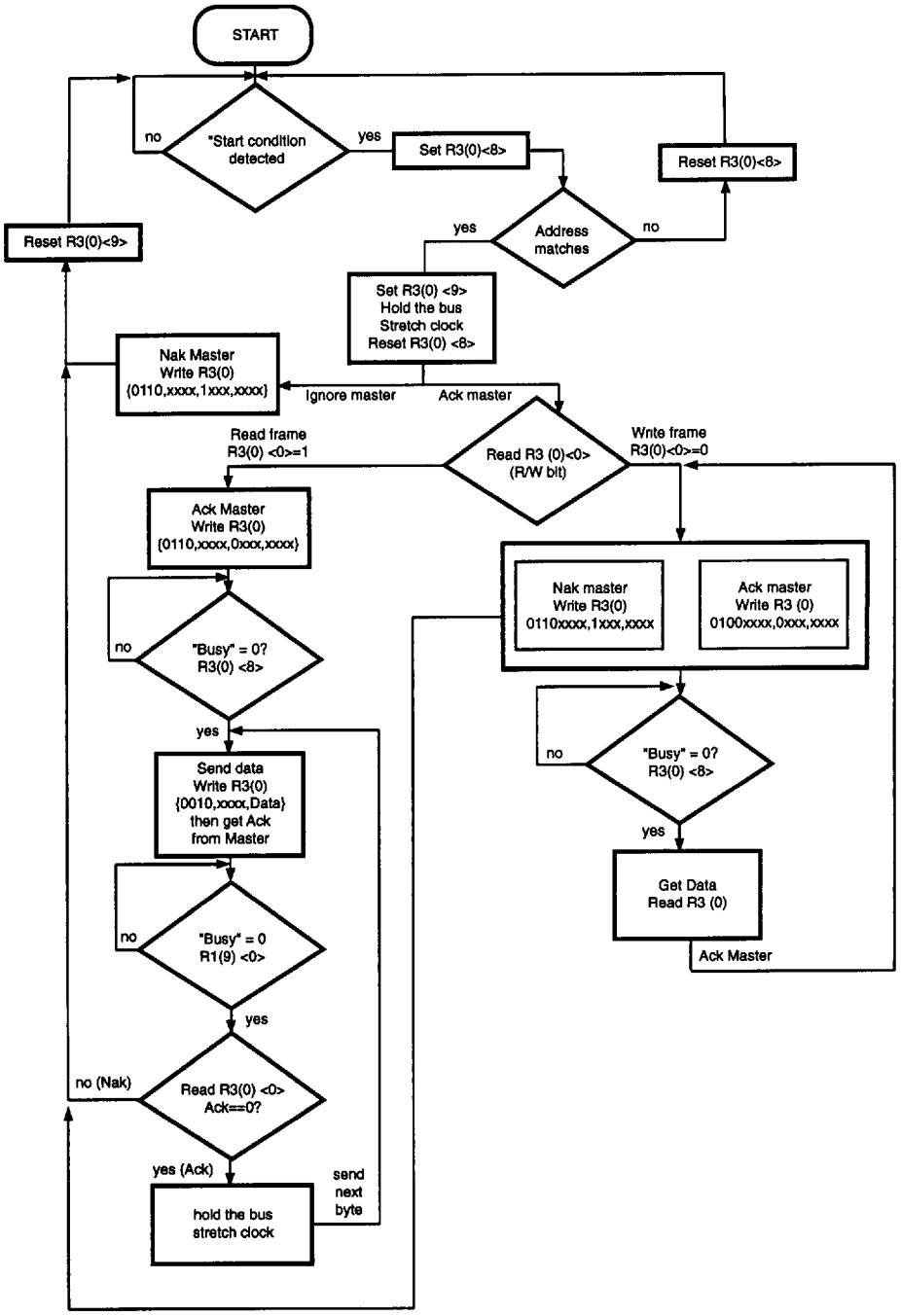

Figure 9. Slave Mode

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Table 9. Register4 - R4(0) Port 0 Data Register

Reg field	Bit position	R	W	Data	Description
Port_data	fedcba9876543210	R		xxxx	If port is configured in input mode - the input data on the port pins If Port is configured in Output mode - the data actually written to the port
			W	xxxx	Data

Table 10. Register5 - R5 (0) Port 1 Data Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba----------	R			Return "0"
			W		No effect
Port_data	------9876543210	R		xxxx	If port is configured in input mode - the input data on the prot pins If Port is configured in Output mode - the data actually written to the port
			W	xxxx	Data

Table 11. Register6 - R6(0) Port 0 Direction Register

Reg field	Bit position	R	W	Data	Description
Port_ direction	fedcba9876543210	R	W	xxxx	1 Input mode for corresponding bit 0 Output mode for corresponding bit

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REGISTERS (Continued)

Table 12. Register 7 - R7(0) Port 1 Direction Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba----------	R	W		Return "0" No effect
Port_ direction	------9876543210	R	W	xxxx	1 Input mode for corresponding bit 0 Output mode for corresponding bit

Bank 1 (Control Registers)

Table 13. Register0 - R0(1) Clamp Position Register

Reg field	Bit position	R	W	Data	Description
Disable_clamp_1	f---------------	R	W	1 0	ADC0 Clamp generation is disabled ADC0 Clamp generation is enabled
Disable_clamp_2	-e--------------	R	W	1 0	ADC5 Clamp generation is disabled ADC5 Clamp generation is enabled Implemented in Rev. BA
Reserved	--dcba987-------	R	W		Return "0" No effect
Position	---------6543210	R	W	xx	Position of clamp pulse (from leading edge of the H-FLYBACK)

Upon POR both disable_clamp bits are set to a "1".

The clamp pulse will be generated if it is Enabled bit (bit <f>) and the SCLK frequency was switched "back" to PVCO (SVCO/PVCO flag in R6 (1) should be reset to "0") before the current h-sync regardless whether the SVCO is enabled or disabled. Clamp position is defined by the "Position" field. The width of clamp pulse cannot be modified and is set to 1 µs. The value which can be assigned to the "Position" field should be >%10 and <%ff. The time interval between the leading edge of the H-FLY-BACK and the beginning of the clamp pulse can be calculated from:

$$Tdelay = Position \times \frac{1}{Tsclk} = Position \times 82\ ns$$

Table 14. Register 1 - R1(1) Speed Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba98765432--	R	W		Return"0" No effect
Fast_enable	--------------1-	R	W	1 0	PVCO,SVCO enabled PVCO,SVCO disabled
Fast/Slow	---------------0	R	W	1 0	SCLK is 12 MHz SCLK is 32 kHz

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Upon POR, SMR and WDT reset both of these bits are reset to "0", which corresponds to SCLK frequency of 32 kHz.

In order to switch from 32 kHz SCLK to 12 MHz, the following procedure is recommended:

- Setting Fast _enable bit to a "1":
- Waiting for 300 .. 400 ms for 12 MHz PLL to be stabilized (approximately 15000 clock cycles)
- Setting Fast/Slow bit to a "1":

In order to switch from 12 MHz SCLK to 32 kHz, the following procedure is recommended:

- Setting Fast/Slow bit to a "0":
- Waiting for 32 µs for SCLK to be switched (approximately 360 clock cycles);
- Setting Fast_enable bit to a "0".

Table 15. Register2 - R2(1) WDT/STOP Mode Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba98765432--	R	W		Return"0" No effect
WDT_instr	--------------1-	R	W	1 0	Return "0" WDT enable, WDT reset No effect
STOP_instr	---------------0	R	W	1 0	Return "0" STOP instruction No effect

Upon POR, SMR and WDT reset the WDT is disabled. The WDT can be re-enabled only after the PVCO and SVCO are enabled and the part is switched into a Fast mode (SCLK = 12 MHz). Upon switching the part into a Slow mode (SCLK = 32 MHz) the WDT will be suspended and the WDT counter will resume count when the Fast operation will be restored. In the latter case an additional re-initialization of the WDT is not necessary.

REGISTERS (Continued)

Table 16. Register3 - R3(1) Standard Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fe----------	R	W		Return"0" No effect
Mask HV-SYNC	--d----------	R	W	1 0	Enable HV output HV input only - POR
Char_Size 16_18/20	---c----------	R	W	1 0	16x20 Char. Matrix 16x16 or 16x18 Char. - POR
Bank0_128/ Bank0_256	----b----------	R	W	1 0 POR	Extended RAM - 128 words Basic Bank - 256 words - POR condition
P07/ ComSYNC	-----a----------	R	W	1 0 POR	Composite SYNC output P07 I/O - POR condition
RGBC/ Port1	------9---------	R	W	1 0 POR	SCLK, R<1:0>,G<1:0>,B<1:0> P16,P08,P10,P13,P18,P15,P14
I2C_port	-------8--------	R	W	1 0	I2C data - P12, I2C clock - P11 I2C data - P02, I2C clock - P01
CGROM blank	--------7-------	R	W	1 0	Bank1 is selected (starts @ % 1000) Bank0 is selected (starts @ % 0000)
HBLANK/ P0f	---------6------	R	W	1 0	HBLANK output P0f output
OSD_ on/off	----------5-----	R	W	1 0	OSD is enabled OSD is disabled
RGB_ polarity	----------4----	R	W	1 0	Negative Positive
Positive/ Negative	----------3---	R	W	1 0	Negative HV-SYNC in output mode Positive HV-SYNC in output mode
SYNC/BLANK	----------2--	R	W	1 0	HV-SYNC outputs HV-SYNC outputs
25/30_Hz and HV polarity	----------10	R	W	10 00 10 00	Internal mode ONLY (TV Standard) 50 Hz/625 lines support 60 Hz/525 lines support External mode ONLY (HV Polarity) Positive Negative
External/ Internal	----------0	R	W	1 0	External (HV-SYNC in input mode) Internal (HV-SYNC in output mode)

Upon POR the HV-SYNC pins are configured in input mode and OSD_on/off bit is reset to "0".

There are two different bits which define polarity of HV-SYNC signals. Bit <3> defines polarity of the output signals on the pads of the device (it does not effect the internal HV-SYNC signals). Bit <1> defines the polarity of the external HV-SYNC signals and effects the synchronization of the device.

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Table 17. Register4 - R4(1) A to D Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcb----------	R	W		Return"0" No effect
ADC_ select	-----a----------	R	W	1 0	ADC4,ADC5 select ADC0, ADC1, ADC2, ADC3 select-POR condition
Reserved	------98---------	R	W		Return"0" No effect
AtoDspeed	-------76--------	R	W	00 01 10 11	Single conversion - POR condition SCLK/4 SCLK/6 SCLK/8
AtoDsource	----------54----	R	W	00 01 10 11	ADC0 (Composite video input) /ADC4 ADC1 (P17) ADC5 ADC2 (P00) ADC3
AtoDdata	------------3210	R	W	%D	AtoD data No effect

There are four different source of A to D converter available in Z89300. Three of them are fixed: ADC0 has a range from 1.5 to 2.0V always connected to Composite Video Input pin of a device and can be clamped to a Ref - voltage (1.5V); ADC1 and ADC2 have a range from 0 to 5V, and are multiplexed with P17 and P00 port pins: ADC3 is available in 52 and 124-pin packages only and has a range from 0 to 5V; ADC4 has a range from 1.5 to 2.0V always connected to Composite Video Input signal and can be clamped to a Ref+ voltage (2.0V).

ADC3 and ADC4 are not available at the same time on 52-pin package. Either one of them can be bonded out according to the customer requirements. Bit <8>of the A to D control register defines the signal source (ADC3/ADC4).

Upon POR the input multiplexor is reset so to select A to D0.
Upon POR A to D control register is not initialized.

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REGISTERS (Continued)

Table 18. Register5 - R5(1) Timer Control Register

Reg field	Bit position	R	W	Data	Description
CAPint_r	f----------	R		1 0	Rising edge is captured No rising edge is captured
			W	1 0	Reset flag No effect
CAPint_f	-e----------	R		1 0	Falling edge is captured No falling edge is captured
			W	1 0	Reset flag No effect
Tout_1s	--d---------	R		1 0	Timeout of 1s timer No timeout of 1s timer
			W	1 0	Reset flag No effect
Tout_CAP	---c--------	R		1 0	Timeout of Capture timer No timeout of Capture timer
			W	1 0	Reset flag No effect
Reserved	----ba------	R			Return "0"
			W		No effect
Speed_1s	------98--------	R	W	00 01 10 11	1s 250 ms 62.5 ms 15.625 ms
1s/CAP_int	--------7-------	R	W	1 0	int2 source is 1s timer int2 source is Capture timer
CAP_halt	---------6------	R	W	1 0	Capture timer is halted Capture timer is running
CAP_edge	----------54----	R	W	00 01 10 11	No Capture Capture on rising edge only Capture on falling edge only Capture on both edges
CAP_glitch	------------32--	R	W	00 01 10 11	Glitch filter is disabled <8TSCLK is filtered out <32TSCLK is filtered out <128TSCLK is filtered out
CAP_speed	--------------10	R	W	00 01 10 11	SCLK/4 SCLK/8 SCLK/16 SCLK/32

When capture register is initialized together with a glitch filter, the CAP_speed field should specify the clock of the capture register with the period shorter than the glitch filter for setting defined by the CAP_glitch field.

For example, the following setting is invalid: CAP_glitch = 10b; CAP_speed = 10b;
The example of valid setting is CAP_glitch = 10b; CAP_speed = 11b

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Table 19. Register6 - R6(1) Clock Switch Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba9876------	R	W		Return "0" No effect
SVCO/PVCO	----------5-----	R	W	1 0 1 0	SCLK=SVCO (flag) SCLK=PVCO (flag) Switch SCLK to PVCO No effect
No_switch	----------4----	R	W	1 0	SCLK=PVCO, NO clock switching Clock switching is enabled
H_position	----------3210	R	W	%D	Defines delay of Hint by 4D SCLK cycles

The clock switch control register defines the source of SCLK fed into the Z89C00 core. The block diagram of the clock switch circuit is presented on figure below.

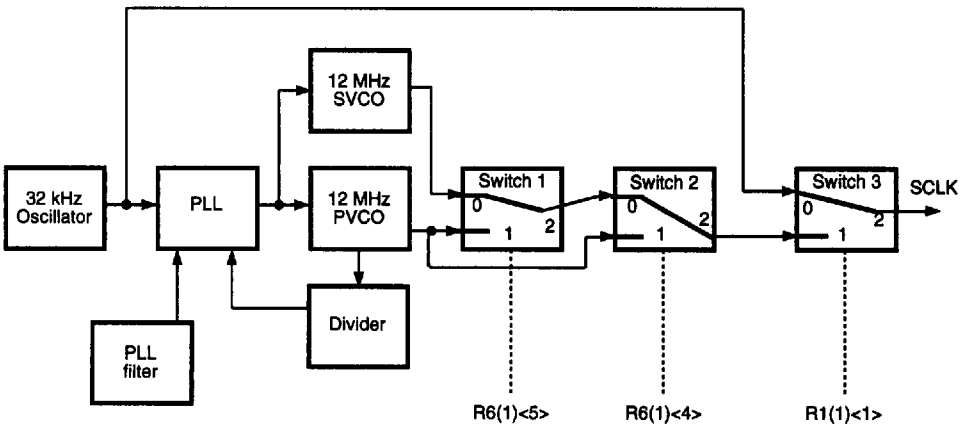

Figure 10. Clock Switch Control Register

Switch1 positioning defines the source of the signal on terminal 0 of switch2. Switch2 is used to override the frequency setting in "no_switch" mode. Whenever "no_switch" mode is set, switch1 continues to switch between PVCO and SVCO. Because of that it is not recommended to switch2 if it is not guaranteed that PVCO signal is fed to terminal0 of switch2. The recommended sequence is as follows:

1. Switch SCLK to PVCO
2. Wait for 2..3 SCLK cycles to ensure that the SCLK is switched
3. Switch R6 (1) <4> to enable/disable "no_switch" mode.

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