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High-Performance 8-Bit Microcontrollers

# Z8 Encore! XP® F0823 Series

## Product Specification

PS024314-0308

**Warning:** DO NOT USE IN LIFE SUPPORT

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# Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

| Date | Revision Level | Description | Page No |
|---|---|---|---|
| March 2008 | 14 | Changed title to Z8 Encore! XP F0823 Series and the contents to match the title. | All |
| December 2007 | 13 | Updated title from Z8 Encore! 8K and 4K Series to Z8 Encore! XP Z8F0823 Series. Updated Figure 3, Table 15, Table 35, Table 59 through Table 61, Table 119, and Part Number Suffix Designations section. | 8, 39, 59, 91, 196, and 226 |
| August 2007 | 12 | Updated Table 1, Table 16, and Program Memory section. | 2, 42, and 13 |
| June 2007 | 11 | Updated to combine Z8 Encore! 8K and Z8 Encore! 4K Series. | All |
| December 2006 | 10 | Updated Ordering Information chapter. | 217 |

# Table of Contents

# Overview

Zilog's Z8 Encore! XP® microcontroller unit (MCU) family of products are the first Zilog® microcontroller products based on the 8-bit eZ8 CPU core. Z8 Encore! XP F0823 Series products expand upon Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8 CPU is upward compatible with existing Z8® instructions. The rich peripheral set of Z8 Encore! XP F0823 Series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

## Features

The key features of Z8 Encore! XP F0823 Series include:

- 5 MHz eZ8 CPU
- 1 KB, 2 KB, 4 KB, or 8 KB Flash memory with in-circuit programming capability
- 256 B, 512 B, or 1 KB register RAM
- 6 to 24 I/O pins depending upon package
- Internal precision oscillator (IPO)
- Full-duplex UART
- The universal asynchronous receiver/transmitter (UART) baud rate generator (BRG) can be configured and used as a basic 16-bit timer
- Infrared data association (IrDA)-compliant infrared encoder/decoders, integrated with UART
- Two enhanced 16-bit timers with capture, compare, and PWM capability
- Watchdog Timer (WDT) with dedicated internal RC oscillator
- On-Chip Debugger (OCD)
- Optional 8-channel, 10-bit Analog-to-Digital Converter (ADC)
- On-Chip analog comparator
- Up to 20 vectored interrupts
- Direct LED drive with programmable drive strengths
- Voltage Brownout (VBO) protection
- Power-On Reset (POR)

- 2.7 V to 3.6 V operating voltage
- Up to thirteen 5 V-tolerant input pins
- 8-, 20-, and 28-pin packages
- 0 °C to +70 °C and -40 °C to +105 °C for operating temperature ranges

# Part Selection Guide

Table 1 lists the basic features and package styles available for each device within the Z8 Encore! XP® F0823 Series product line.

**Table 1. Z8 Encore! XP F0823 Series Family Part Selection Guide**

| Part Number | Flash (KB) | RAM (B) | I/O | ADC Inputs | Packages |
|---|---|---|---|---|---|
| Z8F0823 | 8 | 1024 | 6–22 | 4–8 | 8-, 20-, and 28-pins |
| Z8F0813 | 8 | 1024 | 6–24 | 0 | 8-, 20-, and 28-pins |
| Z8F0423 | 4 | 1024 | 6–22 | 4–8 | 8-, 20-, and 28-pins |
| Z8F0413 | 4 | 1024 | 6–24 | 0 | 8-, 20-, and 28-pins |
| Z8F0223 | 2 | 512 | 6–22 | 4–8 | 8-, 20-, and 28-pins |
| Z8F0213 | 2 | 512 | 6–24 | 0 | 8-, 20-, and 28-pins |
| Z8F0123 | 1 | 256 | 6–22 | 4–8 | 8-, 20-, and 28-pins |
| Z8F0113 | 1 | 256 | 6–24 | 0 | 8-, 20-, and 28-pins |

# Block Diagram

Figure 1 on page 3 displays the block diagram of the architecture of Z8 Encore! XP F0823 Series devices.

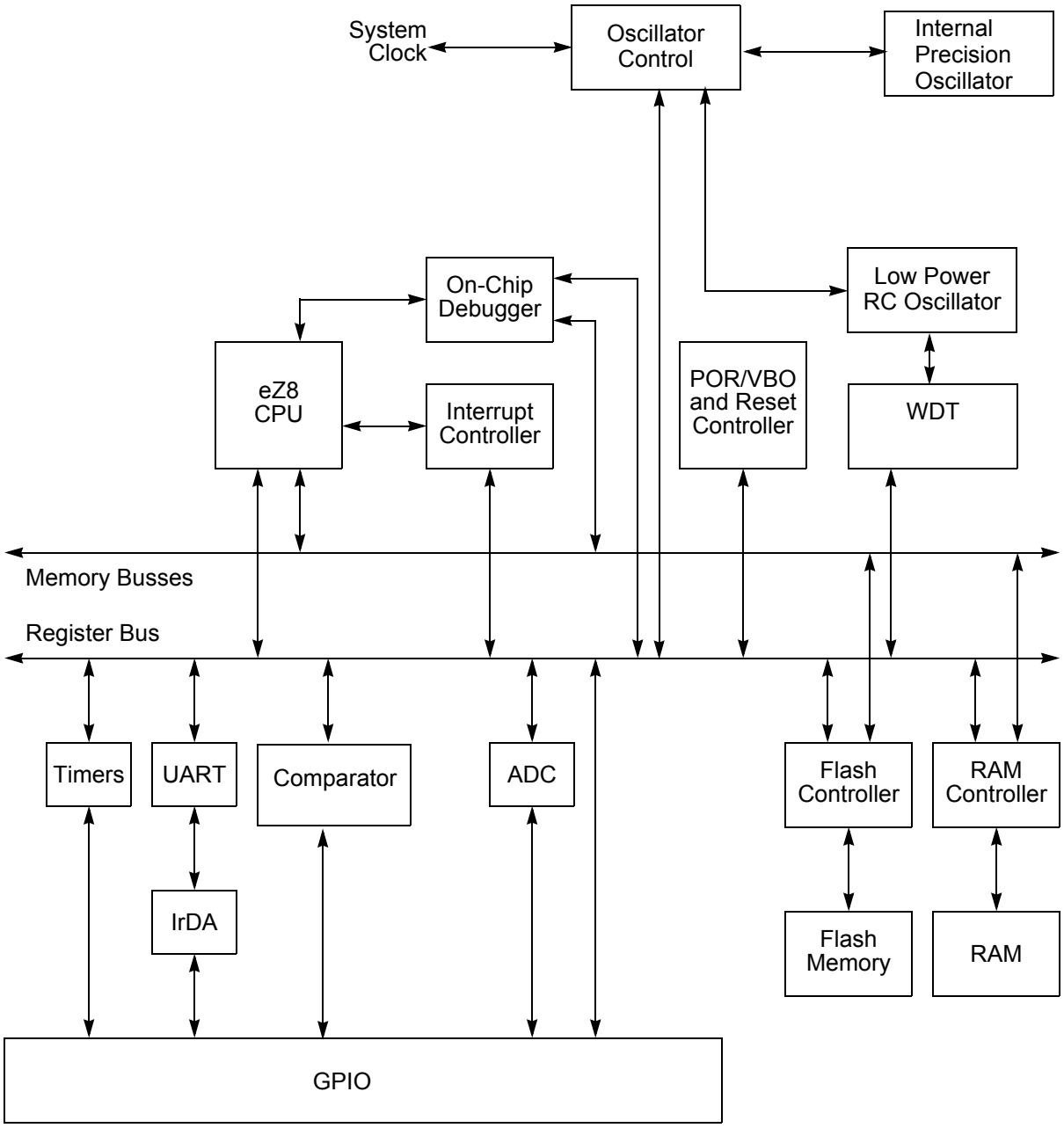


**Figure 1. Z8 Encore! XP® F0823 Series Block Diagram**

# CPU and Peripheral Overview

## eZ8 CPU Features

The eZ8 CPU, Zilog's latest 8-bit central processing unit (CPU), meets the continuing demand for faster and code-efficient microcontrollers. The eZ8 CPU executes a superset of the original Z8® instruction set. The eZ8 CPU features include:

- Direct register-to-register architecture allows each register to function as an accumulator, improving execution time and decreasing the required program memory.
- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks.
- Compatible with existing Z8 code.
- Expanded internal Register File allows access of up to 4 KB.
- New instructions improve execution efficiency for code developed using higher-level programming languages, including C.
- Pipelined instruction fetch and execution.
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT, and SRL.
- New instructions support 12-bit linear addressing of the Register file.
- Up to 10 MIPS operation.
- C-Compiler friendly.
- 2 to 9 clock cycles per instruction.

For more information on eZ8 CPU, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at www.zilog.com.

## General-Purpose I/O

Z8 Encore! XP F0823 Series features 6 to 24 port pins (Ports A–C) for general-purpose I/O (GPIO). The number of GPIO pins available is a function of package. Each pin is individually programmable. 5 V tolerant input pins are available on all I/Os on 8-pin devices, most I/Os on other package types.

## Flash Controller

The Flash Controller programs and erases Flash memory. The Flash Controller supports protection against accidental program and erasure, as well as factory serialization and read protection.

## Internal Precision Oscillator

The internal precision oscillator (IPO) is a trimmable clock source that requires no external components.

## 10-Bit Analog-to-Digital Converter

The optional analog-to-digital converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from eight different analog input pins in both single-ended and differential modes.

## Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable voltage reference or a second input pin. The comparator output can be used to drive either an output pin or to generate an interrupt.

## Universal Asynchronous Receiver/Transmitter

The UART is full-duplex and capable of handling asynchronous data transfers. The UART supports 8- and 9-bit data modes and selectable parity. The UART also supports multi-drop address processing in hardware. The UART baud rate generator can be configured and used as a basic 16-bit timer.

## Timers

Two enhanced 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in ONE-SHOT, CONTINUOUS, GATED, CAPTURE, CAPTURE RESTART, COMPARE, CAPTURE AND COMPARE, PWM SINGLE OUTPUT, and PWM DUAL OUTPUT modes.

## Interrupt Controller

Z8 Encore! XP® F0823 Series products support up to 20 interrupts. These interrupts consist of eight internal peripheral interrupts and 12 general-purpose I/O pin interrupt sources. The interrupts have three levels of programmable interrupt priority.

## Reset Controller

Z8 Encore! XP® F0823 Series products can be reset using the $\overline{\text{RESET}}$ pin, POR, WDT time-out, STOP mode exit, or Voltage Brownout warning signal. The $\overline{\text{RESET}}$ pin is bidirectional, that is, it functions as reset source as well as a reset indicator.

## On-Chip Debugger

Z8 Encore! XP F0823 Series products feature an integrated On-Chip Debugger. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints and executing code. A single-pin interface provides communication to the OCD.

# Pin Description

Z8 Encore! XP® F0823 Series products are available in a variety of package styles and pin configurations. This chapter describes the signals and pin configurations available for each of the package styles. For information on physical package specifications, see Packaging on page 209.

## Available Packages

Table 2 lists the package styles that are available for each device in the Z8 Encore! XP F0823 Series product line.

**Table 2. Z8 Encore! XP F0823 Series Package Options**

| Part Number | ADC | 8-pin PDIP | 8-pin SOIC | 20-pin PDIP | 20-pin SOIC | 20-pin SSOP | 28-pin PDIP | 28-pin SOIC | 28-pin SSOP | 8-pin QFN/ MLF-S |
|---|---|---|---|---|---|---|---|---|---|---|
| Z8F0823 | Yes | X | X | X | X | X | X | X | X | X |
| Z8F0813 | No | X | X | X | X | X | X | X | X | X |
| Z8F0423 | Yes | X | X | X | X | X | X | X | X | X |
| Z8F0413 | No | X | X | X | X | X | X | X | X | X |
| Z8F0223 | Yes | X | X | X | X | X | X | X | X | X |
| Z8F0213 | No | X | X | X | X | X | X | X | X | X |
| Z8F0123 | Yes | X | X | X | X | X | X | X | X | X |
| Z8F0113 | No | X | X | X | X | X | X | X | X | X |

## Pin Configurations

Figure 2 through Figure 4 displays the pin configurations for all packages available in the Z8 Encore! XP F0823 Series. For description of signals, see Table 3. The analog input alternate functions (ANA*x*) are not available on the Z8F0x13 devices. The analog supply pins ($AV_{DD}$ and $AV_{SS}$) are also not available on these parts, and are replaced by PB6 and PB7.

At reset, all pins of Ports A, B, and C default to an input state. In addition, any alternate functionality is not enabled, so the pins function as general-purpose input ports until programmed otherwise.

The pin configurations listed are preliminary and subject to change based on manufacturing limitations.

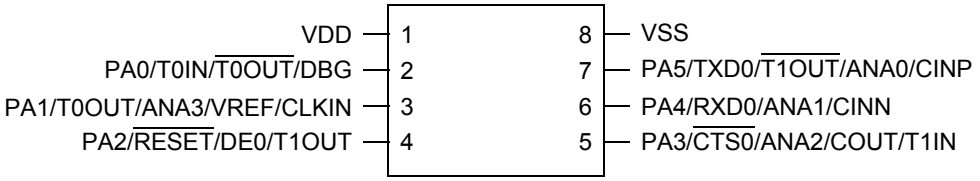


**Figure 2. Z8F08x3, Z8F04x3, F02x3 and Z8F01x3 in 8-Pin SOIC, QFN/MLF-S, or PDIP Package***

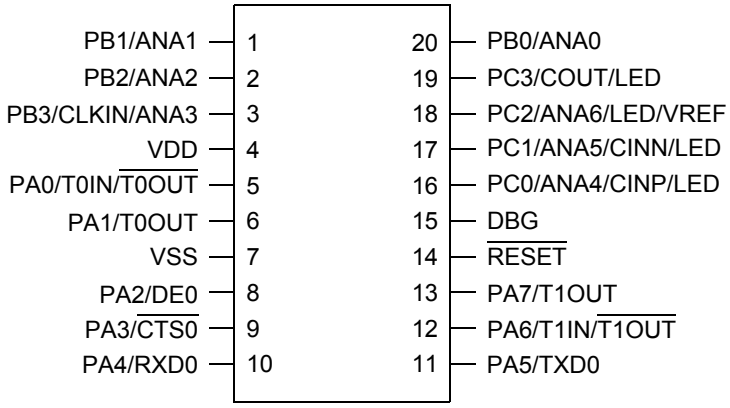


**Figure 3. Z8F08x3, Z8F04x3, F02x3 and Z8F01x3 in 20-Pin SOIC, SSOP or PDIP Package***

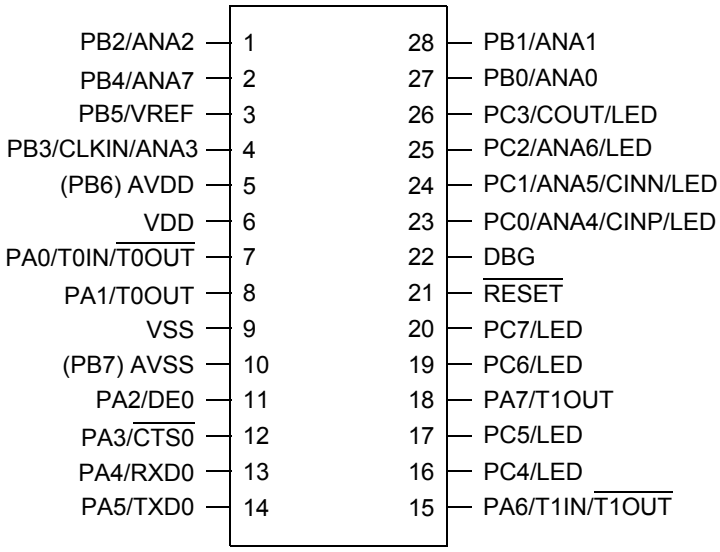


**Figure 4. Z8F08x3, Z8F04x3, F02x3 and Z8F01x3 in 28-Pin SOIC, SSOP or PDIP Package***

**Note:** *Analog input alternate functions (ANA) are not available on the Z8F0x13 devices.

# Signal Descriptions

Table 3 lists the Z8 Encore! XP® F0823 Series signals. To determine the signals available for the specific package styles, see Pin Configurations on page 7.

**Table 3. Signal Descriptions**

| Signal Mnemonic | I/O | Description |
|---|---|---|
| **General-Purpose I/O Ports A–D** | | |
| PA[7:0] | I/O | Port A. These pins are used for general-purpose I/O. |
| PB[7:0] | I/O | Port B. These pins are used for general-purpose I/O. PB6 and PB7 are available only in those devices without an ADC. |
| PC[7:0] | I/O | Port C. These pins are used for general-purpose I/O. |
| **Note:** PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by $AV_{DD}$ and $AV_{SS}$. | | |
| **UART Controllers** | | |
| TXD0 | O | Transmit Data. This signal is the transmit output from the UART and IrDA. |
| RXD0 | I | Receive Data. This signal is the receive input for the UART and IrDA. |
| $\overline{CTS0}$ | I | Clear To Send. This signal is the flow control input for the UART. |
| DE | O | Driver Enable. This signal allows automatic control of external RS-485 drivers. This signal is approximately the inverse of the TXE (Transmit Empty) bit in the UART Status 0 register. The DE signal can be used to ensure the external RS-485 driver is enabled when data is transmitted by the UART. |
| **Timers** | | |
| T0OUT/T1OUT | O | Timer Output 0–1. These signals are output from the timers. |
| $\overline{T0OUT}$/$\overline{T1OUT}$ | O | Timer Complement Output 0–1. These signals are output from the timers in PWM Dual Output mode. |
| T0IN/T1IN | I | Timer Input 0–1. These signals are used as the capture, gating and counter inputs. The T0IN signal is multiplexed $\overline{T0OUT}$ signals. |
| **Comparator** | | |
| CINP/CINN | I | Comparator Inputs. These signals are the positive and negative inputs to the comparator. |
| COUT | O | Comparator Output. This is the output of the comparator. |

**Table 3. Signal Descriptions (Continued)**

| Signal Mnemonic | I/O | Description |
|---|---|---|
| **Analog** | | |
| ANA[7:0] | I | Analog port. These signals are used as inputs to the ADC. The ANA0, ANA1, and ANA2 pins can also access the inputs and output of the integrated transimpedance amplifier. |
| VREF | I/O | Analog-to-Digital Converter reference voltage input. |
| **Clock Input** | | |
| CLKIN | I | Clock Input Signal. This pin can be used to input a TTL-level signal to be used as the system clock. |
| **LED Drivers** | | |
| LED | O | Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block. |
| **On-Chip Debugger** | | |
| DBG | I/O | Debug. This signal is the control and data input and output to and from the OCD.<br>**Caution:** *The DBG pin is open-drain and requires an external pull-up resistor to ensure proper operation.* |
| **Reset** | | |
| RESET | I/O | RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin Low when in reset. This pin is open-drain and features an enabled internal pull-up resistor. |
| **Power Supply** | | |
| $V_{DD}$ | I | Digital Power Supply. |
| $AV_{DD}$ | I | Analog Power Supply. |
| $V_{SS}$ | I | Digital Ground. |
| $AV_{SS}$ | I | Analog Ground. |

**Note:** The $AV_{DD}$ and $AV_{SS}$ signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

# Pin Characteristics

Table 4 provides detailed information about the characteristics for each pin available on Z8 Encore! XP F0823 Series 20- and 28-pin devices. Data in Table 4 is sorted alphabetically by the pin symbol mnemonic.

Table 5 provides detailed information about the characteristics for each pin available on Z8 Encore! XP® F0823 Series 8-pin devices.

**Note:** *All six I/O pins on the 8-pin packages are 5 V-tolerant (unless the pull-up devices are enabled). The column in Table 4 below describes 5 V-tolerance for the 20- and 28-pin packages only.*

**Table 4. Pin Characteristics (20- and 28-pin Devices)**

| Symbol Mnemonic | Direction | Reset Direction | Active Low or Active High | Tristate Output | Internal Pull-up or Pull-down | Schmitt-Trigger Input | Open Drain Output | 5 V Tolerance |
|---|---|---|---|---|---|---|---|---|
| AVDD | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| AVSS | N/A | N/A | N/A | N/A | N/A | N/A | N/A | NA |
| DBG | I/O | I | N/A | Yes | No | Yes | Yes | Yes |
| PA[7:0] | I/O | I | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | PA[7:2] only |
| PB[7:0] | I/O | I | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | PB[7:6] only |
| PC[7:0] | I/O | I | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | PC[7:3] only |
| RESET | I/O | I/O (defaults to $\overline{\text{RESET}}$) | Low (in Reset mode) | Yes (PD0 only) | Always on for $\overline{\text{RESET}}$ | Yes | Always on for $\overline{\text{RESET}}$ | Yes |
| VDD | N/A | N/A | N/A | N/A | | | N/A | N/A |
| VSS | N/A | N/A | N/A | N/A | | | N/A | N/A |

**Note:** *PB6 and PB7 are available only in the devices without ADC.*

**Table 5. Pin Characteristics (8-Pin Devices)**

| Symbol Mnemonic | Direction | Reset Direction | Active Low or Active High | Tristate Output | Internal Pull-up or Pull-down | Schmitt-Trigger Input | Open Drain Output | 5 V Tolerance |
|---|---|---|---|---|---|---|---|---|
| PA0/DBG | I/O | I (but can change during reset if key sequence detected) | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | Yes, unless pull-ups enabled |
| PA1 | I/O | I | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | Yes, unless pull-ups enabled |
| $\overline{\text{RESET}}$/ PA2 | I/O | I/O (defaults to $\overline{\text{RESET}}$) | N/A | Yes | Programmable for PA2; always on for $\overline{\text{RESET}}$ | Yes | Programmable for PA2; always on for $\overline{\text{RESET}}$ | Yes, unless pull-ups enabled |
| PA[5:3] | I/O | I | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | Yes, unless pull-ups enabled |
| VDD | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| VSS | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

# Address Space

The eZ8 CPU can access three distinct address spaces:

- The Register File contains addresses for the general-purpose registers and the eZ8 CPU, peripheral, and general-purpose I/O port control registers.
- The Program Memory contains addresses for all memory locations having executable code and/or data.
- The Data Memory contains addresses for all memory locations that contain data only.

These three address spaces are covered briefly in the following subsections. For more detailed information regarding the eZ8 CPU and its address space, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at www.zilog.com.

## Register File

The Register File address space in the Z8 Encore! XP® MCU is 4 KB (4096 bytes). The Register File is composed of two sections: control registers and general-purpose registers. When instructions are executed, registers defined as sources are read, and registers defined as destinations are written. The architecture of the eZ8 CPU allows all general-purpose registers to function as accumulators, address pointers, index registers, stack areas, or scratch pad memory.

The upper 256 bytes of the 4 KB Register File address space are reserved for control of the eZ8 CPU, the on-chip peripherals, and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256 B control register section are reserved (unavailable). Reading from a reserved Register File address returns an undefined value. Writing to reserved Register File addresses is not recommended and can produce unpredictable results.

The on-chip RAM always begins at address 000H in the Register File address space. Z8 Encore! XP F0823 Series devices contain 256 B-1 KB of on-chip RAM. Reading from Register File addresses outside the available RAM addresses (and not within the control register address space) returns an undefined value. Writing to these Register File addresses produces no effect.

## Program Memory

The eZ8 CPU supports 64 KB of Program Memory address space. Z8 Encore! XP F0823 Series devices contain 1 KB to 8 KB of on-chip Flash memory in the Program Memory address space. Reading from Program Memory addresses outside the available Flash

memory addresses returns FFH. Writing to these unimplemented Program Memory addresses produces no effect. Table 6 describes the Program Memory maps for the Z8 Encore! XP® F0823 Series products.

**Table 6. Z8 Encore! XP F0823 Series Program Memory Maps**

| Program Memory Address (Hex) | Function |
|---|---|
| **Z8F0823 and Z8F0813 Products** | |
| 0000–0001 | Flash Option Bits |
| 0002–0003 | Reset Vector |
| 0004–0005 | WDT Interrupt Vector |
| 0006–0007 | Illegal Instruction Trap |
| 0008–0037 | Interrupt Vectors* |
| 0038–003D | Oscillator Fail Traps* |
| 003E–0FFF | Program Memory |
| **Z8F0423 and Z8F0413 Products** | |
| 0000–0001 | Flash Option Bits |
| 0002–0003 | Reset Vector |
| 0004–0005 | WDT Interrupt Vector |
| 0006–0007 | Illegal Instruction Trap |
| 0008–0037 | Interrupt Vectors* |
| 0038–003D | Oscillator Fail Traps* |
| 003E–0FFF | Program Memory |
| **Z8F0223 and Z8F0213 Products** | |
| 0000–0001 | Flash Option Bits |
| 0002–0003 | Reset Vector |
| 0004–0005 | WDT Interrupt Vector |
| 0006–0007 | Illegal Instruction Trap |
| 0008–0037 | Interrupt Vectors* |
| 0038–003D | Oscillator Fail Traps* |
| 003E–07FF | Program Memory |
| **Z8F0123 and Z8F0113 Products** | |
| 0000–0001 | Flash Option Bits |

**Table 6. Z8 Encore! XP F0823 Series Program Memory Maps (Continued)**

| Program Memory Address (Hex) | Function |
|---|---|
| 0002–0003 | Reset Vector |
| 0004–0005 | WDT Interrupt Vector |
| 0006–0007 | Illegal Instruction Trap |
| 0008–0037 | Interrupt Vectors* |
| 0038–003D | Oscillator Fail Traps* |
| 003E–03FF | Program Memory |

*See Table 33 on page 54 for a list of the interrupt vectors and traps.

## Data Memory

Z8 Encore! XP® F0823 Series does not use the eZ8 CPU's 64 KB Data Memory address space.

## Flash Information Area

Table 7 lists the Z8 Encore! XP F0823 Series Flash Information Area. This 128 B Information Area is accessed by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash Information Area is mapped into the Program Memory and overlays the 128 bytes at addresses FE00H to FF7FH. When the Information Area access is enabled, all reads from these Program Memory addresses return the Information Area data rather than the Program Memory data. Access to the Flash Information Area is read-only.

**Table 7. Z8 Encore! XP F0823 Series Flash Memory Information Area Map**

| Program Memory Address (Hex) | Function |
|---|---|
| FE00–FE3F | Zilog Option Bits. |
| FE40–FE53 | Part Number.<br>20-character ASCII alphanumeric code<br>Left justified and filled with FH. |
| FE54–FE5F | Reserved. |
| FE60–FE7F | Zilog Calibration Data. |
| FE80–FFFF | Reserved. |