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High Performance 8-Bit Microcontrollers

Z8 Encore! XP® F0822 Series

Product Specification

PS022517-0508

Warning: DO NOT USE IN LIFE SUPPORT

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page Number
May 2008	17	Removed Flash Microcontrollers from the title throughout the document.	All
February 2008	16	Updated the flag status for BCLR, BIT, and BSET in Table 126.	219
December 2007	15	Updated Zilog logo, Zilog text, Disclaimer section, and implemented style guide. Updated Z8 Encore! 8K Series to Z8 Encore! XP F0822 Series Flash Microcontrollers throughout the document.	All
June 2007 and August 2007	13 and 14	No Changes.	All
December 2006	12	Updated Ordering Information and minor edits done.	All

Table of Contents

Introduction

This Product Specification provides detailed operating information for Z8 Encore! XP® F0822 Series devices within the Z8 Encore! XP Microcontroller (MCU) family of products. Within this document, Z8 Encore! XP® F0822 Series is referred as Z8 Encore! XP or the F0822 Series unless specifically stated otherwise.

About This Manual

Zilog recommends that you read and understand everything in this manual before setting up and using the product. We have designed this Product Specification to be used either as a *how to* procedural manual or a reference guide to important data.

Intended Audience

This document is written for Zilog customers who are experienced at working with microcontrollers, integrated circuits, or printed circuit assemblies.

Manual Conventions

The following assumptions and conventions are adopted to provide clarity and ease of use:

Courier Typeface

Commands, code lines and fragments, bits, equations, hexadecimal addresses, and various executable items are distinguished from general text by the use of the `Courier` typeface. Where the use of the font is not indicated, as in the Index, the name of the entity is presented in upper case.

- **Example:** FLAGS[1] is `smrf`.

Hexadecimal Values

Hexadecimal values are designated by uppercase *H* suffix and appear in the `Courier` typeface.

- **Example:** R1 is set to `F8H`.

Brackets

The square brackets [ ], indicate a register or bus.

- **Example:** For the register R1[7:0], R1 is an 8-bit register, R1[7] is the most significant bit, and R1[0] is the least significant bit.

Braces

The curly braces { }, indicate a single register or bus created by concatenating some combination of smaller registers, buses, or individual bits.

- **Example:** The 12-bit register address {0H, RP[7:4], R1[3:0]} is composed of a 4-bit hexadecimal value (0H) and two 4-bit register values taken from the Register Pointer (RP) and Working Register R1. 0H is the most significant nibble (4-bit value) of the 12-bit register, and R1[3:0] is the least significant nibble of the 12-bit register.

Parentheses

The parentheses ( ), indicate an indirect register address lookup.

- **Example:** (R1) is the memory location referenced by the address contained in the Working Register R1.

Parentheses/Bracket Combinations

The parentheses ( ), indicate an indirect register address lookup and the square brackets, [ ], indicate a register or bus.

- **Example:** Assume PC[15:0] contains the value 1234h. (PC [15:0]) then refers to the contents of the memory location at address 1234h.

Use of the Words *Set*, *Reset* and *Clear*

The word *set* implies that a register bit or a condition contains a logical 1. The words re*set* or *clear* imply that a register bit or a condition contains a logical 0. When either of these terms is followed by a number, the word *logical* cannot be included; however, it is implied.

Notation for Bits and Similar Registers

A field of bits within a register is designated as: Register[*n*:*n*].

- **Example:** ADDR[15:0] refers to bits 15 through bit 0 of the Address.

Use of the Terms *LSB*, *MSB*, *lsb*, and *msb*

In this document, the terms *LSB* and *MSB,* when appearing in upper case, mean *least significant byte* and *most significant byte*, respectively. The lowercase forms, *lsb* and *msb*, mean *least significant bit* and *most significant bit*, respectively.

Use of Initial Uppercase Letters

Initial uppercase letters designate settings and conditions in general text.

- **Example 1**: The receiver forces the SCL line to Low.
- **Example 2:** The Master generates a STOP condition to abort the transfer.

Use of All Uppercase Letters

The use of all uppercase letters designates the names of states, modes, and commands.

- **Example 1:** The bus is considered BUSY after the Start condition.
- **Example 2:** A START command triggers the processing of the initialization sequence.
- **Example 3:** STOP mode.

Bit Numbering

Bits are numbered from *0* to *n–1* where *n* indicates the total number of bits. For example, the 8 bits of a register are numbered from 0 to 7.

Safeguards

It is important that you understand the following safety terms, which are defined here.

Caution: *Indicates a procedure or file can become corrupted if you does not follow directions.*

Abbreviations/Acronyms

This document uses the following abbreviations or acronyms.

Abbreviations/ Acronyms	Expansion
ADC	Analog-to-Digital Converter
LPO	Low-Power Operational Amplifier
SPI	Serial Peripheral Interface
WDT	Watchdog Timer
GPIO	General-Purpose Input/Output
OCD	On-Chip Debugger
POR	Power-On Reset
LVD	Low-Voltage Detection
VBO	Voltage Brownout
ISR	Interrupt Service Routine
UART	Universal Asynchronous Receiver/Transmitter
IrDA	Infrared Data Association
I^2C	Inter-Integrated Circuit

Abbreviations/ Acronyms	Expansion
PDIP	Plastic Dual Inline Package
SOIC	Small Outline Integrated Circuit
SSOP	Small Shrink Outline Package
PC	Program Counter
IRQ	Interrupt Request

Introduction

Zilog's Z8 Encore! XP® MCU product family is a line of Zilog microcontrollers based on the 8-bit eZ8 CPU. Z8 Encore! XP® F0822 Series, hereafter referred as Z8 Encore! XP or the 8K Series adds Flash memory to Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming allows faster development time and program changes in the field. The new eZ8 CPU is upward-compatible with the existing Z8® instructions. The rich peripheral set of Z8 Encore! XP makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

Features

The features of Z8 Encore! XP MCU product family include:

- 20 MHz eZ8 CPU core
- Up to 8 KB Flash with in-circuit programming capability
- 1 KB Register RAM
- Optional 2- to 5-channel, 10-bit Analog-to-Digital Converter (ADC)
- Full-duplex 9-bit Universal Asynchronous Receiver/Transmitter (UART) with bus transceiver Driver Enable Control
- Inter-Integrated Circuit (I^2C)
- Serial Peripheral Interface (SPI)
- Infrared Data Association (IrDA)-compliant infrared encoder/decoders
- Two 16-bit timers with Capture, Compare, and PWM capability
- Watchdog Timer (WDT) with internal RC oscillator
- 11 to 19 Input/Output pins depending upon package
- Up to 19 interrupts with configurable priority
- On-Chip Debugger (OCD)
- Voltage Brownout (VBO) protection
- Power-On Reset (POR)
- Crystal oscillator with three power settings and RC oscillator option

- 2.7 V to 3.6 V operating voltage with 5 V-tolerant inputs
- 20-pin and 28-pin packages
- 0 °C to +70 °C standard temperature and -40 °C to +105 °C extended temperature operating ranges

Part Selection Guide

Table 1 identifies the basic features and package styles available for each device within the Z8 Encore! XP® F0822 Series product line.

Table 1. Z8 Encore! XP® F0822 Series Part Selection Guide

Part Number	Flash (KB)	RAM (KB)	I/O	16-bit Timers with PWM	ADC Inputs	UARTs with IrDA	I^2C	SPI	Package Pin Counts	
									20	28
Z8F0822	8	1	19	2	5	1	1	1		X
Z8F0821	8	1	11	2	2	1	1		X	
Z8F0812	8	1	19	2	0	1	1	1		X
Z8F0811	8	1	11	2	0	1	1		X	
Z8F0422	4	1	19	2	5	1	1	1		X
Z8F0421	4	1	11	2	2	1	1		X	
Z8F0412	4	1	19	2	0	1	1	1		X
Z8F0411	4	1	11	2	0	1	1		X	

Block Diagram

Figure 1 displays the block diagram of the architecture of Z8 Encore! XP® F0822 Series devices.

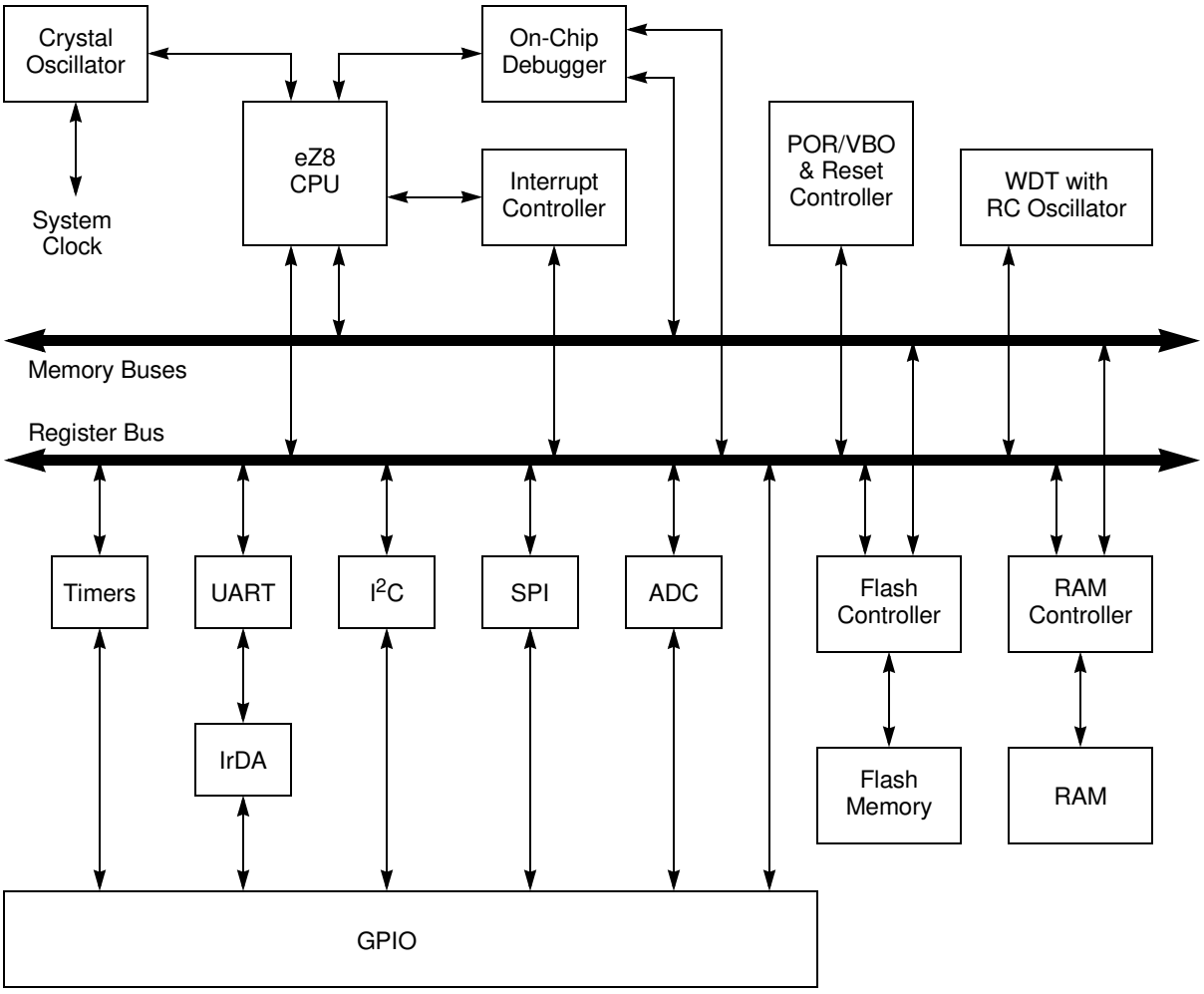

Figure 1. Z8 Encore! XP® F0822 Series Block Diagram

CPU and Peripheral Overview

eZ8 CPU Features

Zilog's latest eZ8 8-bit CPU, meets the continuing demand for faster and more code-efficient microcontrollers. The eZ8 CPU executes a superset of the original Z8® instruction set.

The eZ8 CPU features include:

- Direct register-to-register architecture allows each register to function as an accumulator, improving execution time and decreasing the required Program Memory.
- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks.
- Compatible with existing Z8® code.
- Expanded internal Register File allows access of up to 4 KB.
- New instructions improve execution efficiency for code developed using higher-level programming languages, including C.
- Pipelined instruction fetch and execution.
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT, and SRL.
- New instructions support 12-bit linear addressing of the Register File.
- Up to 10 MIPS operation.
- C-Compiler friendly.
- 2 to 9 clock cycles per instruction.

For more information regarding the eZ8 CPU, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at www.zilog.com.

General Purpose Input/Output

Z8 Encore! XP® F0822 Series features 11 to 19 port pins (Ports A–C) for General Purpose Input/Output (GPIO). The number of GPIO pins available is a function of package. Each pin is individually programmable. Ports A and C supports 5 V-tolerant inputs.

Flash Controller

The Flash Controller programs and erases the Flash memory.

10-Bit Analog-to-Digital Converter

The optional Analog-to-Digital Converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from 2 to 5 different analog input sources.

UART

The Universal Asynchronous Receiver/Transmitter (UART) is full-duplex and capable of handling asynchronous data transfers. The UART supports 8-bit and 9-bit data modes and selectable parity.

I²C

The Inter-Integrated Circuit (I^2C) controller makes the Z8 Encore! XP compatible with the I^2C protocol. The I^2C Controller consists of two bidirectional bus lines, a serial data (SDA) line, and a serial clock (SCL) line.

Serial Peripheral Interface

The Serial Peripheral Interface (SPI) allows the Z8 Encore! XP to exchange data between other peripheral devices such as EEPROMs, A/D converters, and ISDN devices. The SPI is a full-duplex, synchronous, and character-oriented channel that supports a four-wire interface.

Timers

Two 16-bit reloadable timers are used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in One-Shot, Continuous, Gated, Capture, Compare, Capture and Compare, and PWM modes.

Interrupt Controller

Z8 Encore! XP® F0822 Series products support up to 18 interrupts. These interrupts consist of 7 internal peripheral interrupts and 11 GPIO pin interrupt sources. The interrupts have 3 levels of programmable interrupt priority.

Reset Controller

Z8 Encore! XP F0822 Series products are reset using the $\overline{\text{RESET}}$ pin, POR, WDT, STOP mode exit, or VBO warning signal.

On-Chip Debugger

Z8 Encore! XP F0822 Series products feature an integrated On-Chip Debugger (OCD). The OCD provides a rich-set of debugging capabilities, such as, reading and writing registers, programming the Flash, setting breakpoints, and executing code. A single-pin interface provides communication to the OCD.

Signal and Pin Descriptions

Z8 Encore! XP® F0822 Series products are available in a variety of packages, styles, and pin configurations. This chapter describes the signals and available pin configurations for each of the package styles. For information regarding the physical package specifications, see Packaging on page 233.

Available Packages

Table 2 identifies the package styles available for each device within Z8 Encore! XP F0822 Series product line.

Table 2. Z8 Encore! XP F0822 Series Package Options

Part Number	10-Bit ADC	20-Pin SSOP and PDIP	28-Pin SOIC and PDIP
Z8F0822	Yes		X
Z8F0821	Yes	X	
Z8F0812	No		X
Z8F0811	No	X	
Z8F0422	Yes		X
Z8F0421	Yes	X	
Z8F0412	No		X
Z8F0411	No	X	

Pin Configurations

Figure 2 through Figure 5 display the pin configurations for all of the packages available in Z8 Encore! XP F0822 Series. See Table 4 for a description of the signals.

Note: *The analog input alternate functions (ANAx) are not available on Z8 Encore! XP® F0822 Series devices.*

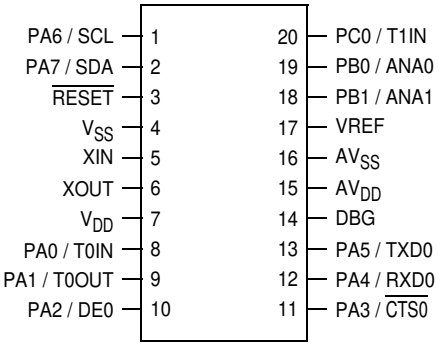

Figure 2. Z8F0821 and Z8F0421 in 20-Pin SSOP and PDIP Packages

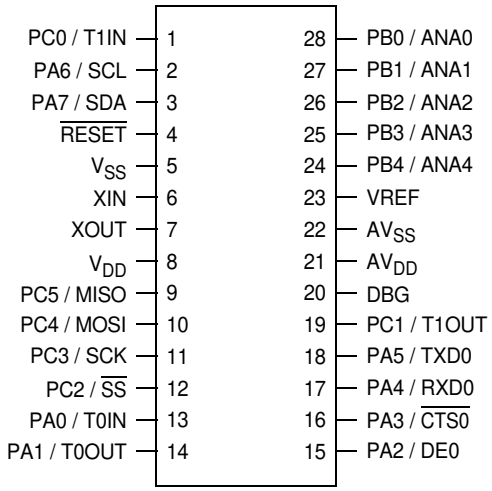

Figure 3. Z8F0822 and Z8F0422 in 28-Pin SOIC and PDIP Packages

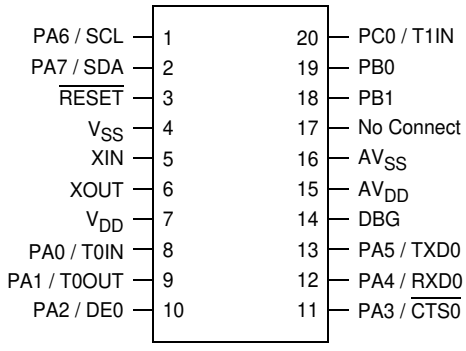

Figure 4. Z8F0811 and Z8F0411 in 20-Pin SSOP and PDIP Packages

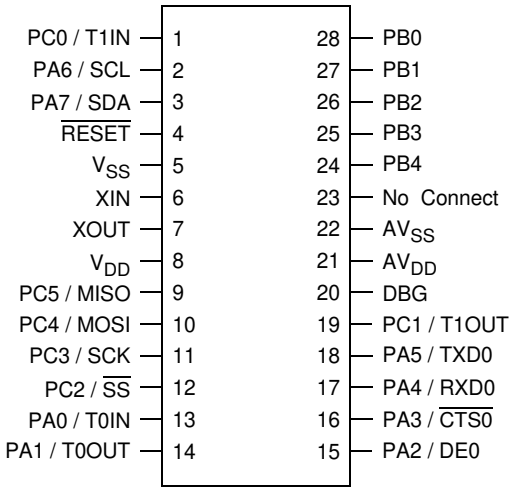

Figure 5. Z8F0812 and Z8F0412 in 28-Pin SOIC and PDIP Packages

Signal Descriptions

Table 3 describes Z8 Encore! XP® F0822 Series signals. See Pin Configurations on page 7 to determine the signals available for the specific package styles

.

Table 3. Signal Descriptions

Signal Mnemonic	I/O	Description
General-Purpose I/O Ports A-H		
PA[7:0]	I/O	**Port C**—These pins are used for general-purpose I/O and supports 5 V-tolerant inputs.
PB[4:0]	I/O	**Port B**—These pins are used for general-purpose I/O.
PC[5:0]	I/O	**Port C**—These pins are used for general-purpose I/O and support 5 V-tolerant inputs.
I²C Controller		
SCL	I/O	**Serial Clock**—This open-drain pin clocks data transfers in accordance with the I²C standard protocol. This pin is multiplexed with a GPIO pin. When the GPIO pin is configured for alternate function to enable the SCL function, this pin is open-drain.
SDA	I/O	**Serial Data**—This open-drain pin transfers data between the I²C and a slave. This pin is multiplexed with a GPIO pin. When the GPIO pin is configured for alternate function to enable the SDA function, this pin is open-drain.

Table 3. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
SPI Controller		
$\overline{SS}$	I/O	**Slave Select**—This signal can be an output or an input. If the Z8 Encore! XP® is the SPI Master, this pin can be configured as the Slave Select output. If the Z8 Encore! XP is the SPI Slave, this pin is the input slave select. It is multiplexed with a GPIO pin.
SCK	I/O	**SPI Serial Clock**—The SPI Master supplies this pin. If the Z8 Encore! XP is the SPI Master, this pin is the output. If the Z8 Encore! XP is the SPI Slave, this pin is the input. It is multiplexed with a GPIO pin.
MOSI	I/O	**Master-Out/Slave-In**—This signal is the data output from the SPI Master device and the data input to the SPI Slave device. It is multiplexed with a GPIO pin.
MISO	I/O	**Master-In/Slave-Out**—This pin is the data input to the SPI Master device and the data output from the SPI Slave device. It is multiplexed with a GPIO pin.
UART Controllers		
TXD0	O	**Transmit Data**—This signal is the transmit output from the UART and IrDA. The TXD signals are multiplexed with GPIO pins.
RXD0	I	**Receive Data**—This signal is the receiver input for the UART and IrDA. The RXD signals are multiplexed with GPIO pins.
$\overline{CTS0}$	I	**Clear To Send**—This signal is control inputs for the UART. The $\overline{CTS}$ signals are multiplexed with GPIO pins.
DE0	O	**Driver Enable**—This signal allows automatic control of external RS-485 drivers. This signal is approximately the inverse of the TXE (Transmit Empty) bit in the UART Status 0 Register. The DE signal can be used to ensure the external RS-485 driver is enabled when data is transmitted by the UART.
Timers		
T0OUT / T1OUT	O	**Timer Output 0–1**—These signals are output pins from the timers. The Timer Output signals are multiplexed with GPIO pins.
T0IN / T1IN	I	**Timer Input 0–1**—These signals are used as the Capture, Gating and Counter inputs. The Timer Input signals are multiplexed with GPIO pins.
Analog		
ANA[4:0]	I	**Analog Input**—These signals are inputs to the Analog-to-Digital Converter (ADC). The ADC analog inputs are multiplexed with GPIO pins.
VREF	I	**Analog-to-Digital Converter reference voltage input**—As an output, the VREF signal is not recommended for use as a reference voltage for external devices. If the ADC is configured to use the internal reference voltage generator, this pin should be left unconnected or capacitively coupled to analog ground (AVSS).

Table 3. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
Oscillators		
XIN	I	**External Crystal Input**—This is the input pin to the crystal oscillator. A crystal is connected between the external crystal input and the XOUT pin to form the oscillator. In addition, this pin is used with external RC networks or external clock drivers to provide the system clock to the system.
XOUT	O	**External Crystal Output**—This pin is the output of the crystal oscillator. A crystal is connected between external crystal output and the XIN pin to form the oscillator. When the system clock is referred in this manual, it refers to the frequency of the signal at this pin. This pin must be left unconnected when not using a crystal.
On-Chip Debugger		
DBG	I/O	**Debug**—This pin is the control and data input and output to and from the OCD. This pin is open-drain. **Caution:** *For operation of the OCD, all power pins (V_{DD} and AV_{DD}) must be supplied with power and all ground pins (V_{SS} and AV_{SS}) must be properly grounded. The DBG pin is open-drain and must have an external pull-up resistor to ensure proper operation.*
Reset		
$\overline{\text{RESET}}$	I	**RESET**—Generates a Reset when asserted (driven Low).
Power Supply		
V_{DD}	I	Digital Power Supply.
AV_{DD}	I	**Analog Power Supply**—Must be powered up and grounded to VDD, even if not using analog features.
V_{SS}	I	Digital Ground.
AV_{SS}	I	**Analog Ground**—Must be grounded and connected to VSS, even if not using analog features.

Pin Characteristics

Table 4 provides detailed information on the characteristics for each pin available on Z8 Encore! XP® F0822 Series products. Table 4 data is sorted alphabetically by the pin symbol mnemonic.

Table 4. Pin Characteristics

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tri-State Output	Internal Pull-up or Pull-down	Schmitt-Trigger Input	Open Drain Output
AV_{DD}	N/A	N/A	N/A	N/A	No	No	N/A
AV_{SS}	N/A	N/A	N/A	N/A	No	No	N/A
DBG	I/O	I	N/A	Yes	No	Yes	Yes
PA[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable
PB[4:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable
PC[5:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable
RESET	I	I	Low	N/A	Pull-up	Yes	N/A
V_{DD}	N/A	N/A	N/A	N/A	No	No	N/A
VREF	Analog	N/A	N/A	N/A	No	No	N/A
V_{SS}	N/A	N/A	N/A	N/A	No	No	N/A
XIN	I	I	N/A	N/A	No	No	N/A
XOUT	O	O	N/A	No	No	No	No