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High-Performance 8-Bit Microcontrollers

Z8 Encore! XP® F6482 Series

Product Specification

PS029412-0618

PRELIMINARY

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Revision History

Each instance in the following revision history table reflects a change to this document from its previous version. For more details, refer to the corresponding pages or appropriate links provided in the table.

Date	Revision Level	Description	Page
Jun 2018	12	Removed Z8F6481AT024XK2247 (80-pin LQFP) from the ZMOTION Library Series Ordering Information table.	633
Apr 2017	11	Corrected typos in pins 9 and 10 of the 32-pin QFN pinout. Corrected RTC_DOW, RTC_DOM, RTC_ADOW, RTC_ADOM addresses. Added information regarding IRQE in Stop Mode. Updated description of PWRCTL1[3:2] regarding control of the ADC and ADC voltage reference. Clarified SEEDSEL usage for DCO. Corrected R/W capability of the TxNFC registers. Corrected counter mode descriptions for RTC_DOW, RTC_DOM, RTC_ADOW, RTC_ADOM. Updated Event In power line selection Added I2C baud rate generator information for the case of the I2C configured as a general purpose timer Clarified stopping ADC conversions when SCAN, CONTCONV or AVE are set. Updated description of ADC wake-up Changed minimum ADC ST value from 1 clock to 2 clocks. Described the effect of setting Op Amp A or Op Amp B OPOWER bit. Clarified OCD block diagram. Removed VBO and LVD pulse rejection periods. Updated DCO resolution and DCO control word resolution. Add ZMOTION ordering part numbers	13 28-29 50 54 109, 121 186 211, 217, 226, 227 212, 228 334 445 446, 448 459 474, 480, 482 558 603, 616 623 633
May 2016	10	Added information about External Pad on the QFN package and clarification about AVDD and AVSS power supply in Table 4.	21, 22
Apr 2016	09	Corrected part number typos in Table 356.	630
Mar 2016	08	Added 44-pin QFN package information to Table 16, Table 356, and Table 358.	55, 630, 635
Jan 2016	07	Corrected Figure 6, 80-pin LQFP.	17
Dec 2015	06	Clarified the 64-pin package size (10mm x 10mm).	629

Nov 2015	05	Added 44-pin Quad Flat No Lead (QFN) packaging option. RTC. Changed LSB in counter mode to DOW. Clarified INPCAP functionality in Dual Input Triggered One-Shot Mode and Gated Mode. Updated 14-bit ADC conversion to be recommended for differential mode only. Indicated that the Op Amp B IRESSEL = 11 setting is not recommended for AV_{DD} < 3V. ADC electrical parameters. Added RESOLUT=1 (14-bit resolution) INL/DNL specs. Reduced maximum INMODE=0x ADC Clock frequency to 2MHz.Reduced maximum RESOLUT=1 ADC Clock frequency to 2MHz. Added ST and SST parameters for INMODE=1x at POWER=10 (low) Corrected typos.	12, 14, 629 211, 217, 218 155, 165, 180 440, 444, 605 477, 482, 605 various
Oct 2014	04	Corrected pin 10 to ESOUT1 from ESOUT0, Figure 2; corrected “P3” values for pins 32 and 33 to “PE”, Figure 3; corrected PB3 value for Pin 53 to PB4, Figure 6; modified description in System Clock Source Switching and PCLK Source Switching sections; clarified description for the ADCREF bit, Table 15; corrected subscripted terms in Frequency Locked Loop and Phase Locked Loop sections; corrected Figure 24 timer output values to T4CH0, T4CH1; clarified description in WDT Interrupt in Normal Operation, WDT Interrupt in Stop Mode, and WDT Reset in Stop Mode sections; clarified IEC definition, DALI Protocol Mode section; modified Bit 7 description, Table 204; corrected overline issue to depict active status of Timers 0, 1, and 2, Table 217; added note, Channel Scanning section; modified description, Starting and Stopping Conversions section and the Automatic and Manual Wake-Up subsections of the Starting and Stopping Conversions section; modified description, ADC Timing section; modified description, ADC Wake-up, Sampling, and Settling section; clarified description, Calibration and Compensation section; modified offset calibration description for bits 7:6, Table 235; modified GAIN values, bits 7:4, Table 253; modified VBIAS descriptions, Reference System Operation section; modified description of Bit 7, Table 257; corrected ADC Output (Hex) value for 0°C from BC1 to B1C, Table 262; modified T_{WAKE_AR} parameter description and T_{WAKE_ADC} conditions, Table 337; modified GAINTOL values and conditions, Table 342.	13, 14, 17, 54, 100, 102, 109, 112, 194, 207, 243, 399, 412, 443, 444, 446, 448, 450, 451, 480, 489, 492, 499, 605, 614
Dec 2013	03	Updated UART-LDD, USB, Option Bits, and Electrical Characteristics chapters.	230, 340, 540, 598
May 2013	02	Corrected to include PRELIMINARY in footer per Zilog style.	n/a
May 2013	01	Original issue.	n/a

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