



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





***Z8F640x, Z8F480x, Z8F320x,
Z8F240x, and Z8F160x***

***Z8 Encore![™] Microcontrollers
with Flash Memory and 10-Bit
A/D Converter***

Product Specification

PS017610-0404



This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters

532 Race Street
San Jose, CA 95126
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

ZiLOG is a registered trademark of ZiLOG Inc. in the United States and in other countries. All other products and/or service names mentioned herein may be trademarks of the companies with which they are associated.

©2004 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZiLOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Devices sold by ZiLOG, Inc. are covered by warranty and limitation of liability provisions appearing in the ZiLOG, Inc. Terms and Conditions of Sale. ZiLOG, Inc. makes no warranty of merchantability or fitness for any purpose Except with the express written approval of ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.



Table of Contents

Introduction	1
Features	1
Part Selection Guide	2
Block Diagram	3
CPU and Peripheral Overview	3
eZ8 CPU Features	3
General Purpose I/O	4
Flash Controller	4
10-Bit Analog-to-Digital Converter	4
UARTs	4
I ² C	4
Serial Peripheral Interface	5
Timers	5
Interrupt Controller	5
Reset Controller	5
On-Chip Debugger	5
DMA Controller	5
Signal and Pin Descriptions	6
Overview	6
Available Packages	6
Pin Configurations	7
Signal Descriptions	13
Pin Characteristics	15
Address Space	17
Overview	17
Register File	17
Program Memory	18
Data Memory	19
Register File Address Map	0
Reset and Stop Mode Recovery	25
Overview	25
Reset Types	25
System and Short Resets	26
Reset Sources	26
Power-On Reset	27
Voltage Brown-Out Reset	27
Watch-Dog Timer Reset	28



External Pin Reset	29
Stop Mode Recovery	29
Stop Mode Recovery Using Watch-Dog Timer Time-Out	29
Stop Mode Recovery Using a GPIO Port Pin Transition	30
Low-Power Modes	31
Overview	31
Stop Mode	31
Halt Mode	31
General-Purpose I/O	33
Overview	33
GPIO Port Availability By Device	33
Architecture	34
GPIO Alternate Functions	34
GPIO Interrupts	36
GPIO Control Register Definitions	36
Port A-H Address Registers	37
Port A-H Control Registers	38
Port A-H Input Data Registers	42
Port A-H Output Data Register	43
Interrupt Controller	44
Overview	44
Interrupt Vector Listing	44
Architecture	46
Operation	46
Master Interrupt Enable	46
Interrupt Vectors and Priority	47
Interrupt Assertion Types	47
Interrupt Control Register Definitions	48
Interrupt Request 0 Register	48
Interrupt Request 1 Register	49
Interrupt Request 2 Register	50
IRQ0 Enable High and Low Bit Registers	51
IRQ1 Enable High and Low Bit Registers	52
IRQ2 Enable High and Low Bit Registers	53
Interrupt Edge Select Register	54
Interrupt Port Select Register	55
Interrupt Control Register	56
Timers	57
Overview	57
Architecture	57
Operation	58



Timer Operating Modes	58
Reading the Timer Count Values	66
Timer Output Signal Operation	66
Timer Control Register Definitions	66
Timer 0-3 High and Low Byte Registers	66
Timer Reload High and Low Byte Registers	67
Timer 0-3 PWM High and Low Byte Registers	69
Timer 0-3 Control Registers	70
Watch-Dog Timer	72
Overview	72
Operation	72
Watch-Dog Timer Refresh	73
Watch-Dog Timer Time-Out Response	73
Watch-Dog Timer Reload Unlock Sequence	74
Watch-Dog Timer Control Register Definitions	75
Watch-Dog Timer Control Register	75
Watch-Dog Timer Reload Upper, High and Low Byte Registers	76
UART	78
Overview	78
Architecture	78
Operation	79
Data Format	79
Transmitting Data using the Polled Method	80
Transmitting Data using the Interrupt-Driven Method	81
Receiving Data using the Polled Method	82
Receiving Data using the Interrupt-Driven Method	82
Receiving Data using the Direct Memory Access Controller (DMA)	83
Multiprocessor (9-bit) Mode	84
UART Interrupts	85
UART Baud Rate Generator	85
UART Control Register Definitions	86
UARTx Transmit Data Register	86
UARTx Receive Data Register	87
UARTx Status 0 and Status 1 Registers	87
UARTx Control 0 and Control 1 Registers	89
UARTx Baud Rate High and Low Byte Registers	91
Infrared Encoder/Decoder	95
Overview	95
Architecture	95
Operation	96



Transmitting IrDA Data	96
Receiving IrDA Data	97
Jitter	98
Infrared Encoder/Decoder Control Register Definitions	98
Serial Peripheral Interface	99
Overview	99
Architecture	99
Operation	100
SPI Signals	101
SPI Clock Phase and Polarity Control	102
Multi-Master Operation	104
Error Detection	105
SPI Interrupts	105
SPI Baud Rate Generator	105
SPI Control Register Definitions	106
SPI Data Register	106
SPI Control Register	107
SPI Status Register	108
SPI Mode Register	109
SPI Baud Rate High and Low Byte Registers	110
I2C Controller	111
Overview	111
Operation	111
SDA and SCL Signals	111
I ² C Interrupts	112
Start and Stop Conditions	112
Writing a Transaction with a 7-Bit Address	112
Writing a Transaction with a 10-Bit Address	114
Reading a Transaction with a 7-Bit Address	115
Reading a Transaction with a 10-Bit Address	116
I2C Control Register Definitions	118
I2C Data Register	118
I2C Status Register	118
I2C Control Register	119
I2C Baud Rate High and Low Byte Registers	121
Direct Memory Access Controller	122
Overview	122
Operation	122
DMA0 and DMA1 Operation	122
Configuring DMA0 and DMA1 for Data Transfer	123



DMA_ADC Operation	123
Configuring DMA_ADC for Data Transfer	124
DMA Control Register Definitions	124
DMAx Control Register	124
DMAx I/O Address Register	125
DMAx Address High Nibble Register	126
DMAx Start/Current Address Low Byte Register	127
DMAx End Address Low Byte Register	128
DMA_ADC Address Register	128
DMA_ADC Control Register	130
DMA Status Register	131
Analog-to-Digital Converter	132
Overview	132
Architecture	132
Operation	133
Automatic Power-Down	133
Single-Shot Conversion	133
Continuous Conversion	134
DMA Control of the ADC	135
ADC Control Register Definitions	135
ADC Control Register	135
ADC Data High Byte Register	137
ADC Data Low Bits Register	137
Flash Memory	138
Overview	138
Operation	139
Flash Operation Timing Using the Flash Frequency Registers ..	141
Flash Code Protection Against External Access	141
Flash Code Protection Against Accidental Program and Erasure	141
Byte Programming	142
Page Erase	143
Mass Erase	143
Flash Controller Bypass	143
Flash Control Register Definitions	144
Flash Control Register	144
Flash Status Register	145
Flash Page Select Register	146
Flash Frequency High and Low Byte Registers	147



Option Bits	148
Overview	148
Operation	148
Option Bit Configuration By Reset	148
Option Bit Address Space	148
Program Memory Address 0000H	149
Program Memory Address 0001H	150
On-Chip Debugger	151
Overview	151
Architecture	151
Operation	152
OCD Interface	152
Debug Mode	153
OCD Data Format	154
OCD Auto-Baud Detector/Generator	154
OCD Serial Errors	155
Breakpoints	155
Watchpoints	155
Runtime Counter	156
On-Chip Debugger Commands	156
On-Chip Debugger Control Register Definitions	161
OCD Control Register	161
OCD Status Register	162
OCD Watchpoint Control Register	163
OCD Watchpoint Address Register	164
OCD Watchpoint Data Register	164
On-Chip Oscillator	165
20MHz Crystal Oscillator Operation	165
Electrical Characteristics	167
Absolute Maximum Ratings	167
DC Characteristics	169
AC Characteristics	172
On-Chip Peripheral AC and DC Electrical Characteristics	173
General Purpose I/O Port Input Data Sample Timing	176
General Purpose I/O Port Output Timing	177
On-Chip Debugger Timing	178
SPI Master Mode Timing	179
SPI Slave Mode Timing	180
I2C Timing	181
eZ8 CPU Instruction Set	182
Assembly Language Programming Introduction	182



Assembly Language Syntax	183
eZ8 CPU Instruction Notation	183
Condition Codes	186
eZ8 CPU Instruction Classes	187
eZ8 CPU Instruction Summary	191
Flags Register	201
Opcode Maps	202
Packaging	206
Ordering Information	211
Part Number Description	214
Precharacterization Product	215
Document Information	215
Document Number Description	215
Customer Feedback Form	216



List of Figures

Figure 1.	Z8 Encore! [®] Block Diagram	3
Figure 2.	Z8Fxx01 in 40-Pin Dual Inline Package (DIP)	7
Figure 3.	Z8Fxx01 in 44-Pin Plastic Leaded Chip Carrier (PLCC)	8
Figure 4.	Z8Fxx01 in 44-Pin Low-Profile Quad Flat Package (LQFP)	9
Figure 5.	Z8Fxx02 in 64-Pin Low-Profile Quad Flat Package (LQFP)	10
Figure 6.	Z8Fxx02 in 68-Pin Plastic Leaded Chip Carrier (PLCC)	11
Figure 7.	Z8Fxx03 in 80-Pin Quad Flat Package (QFP)	12
Figure 8.	Power-On Reset Operation	27
Figure 9.	Voltage Brown-Out Reset Operation	28
Figure 10.	GPIO Port Pin Block Diagram	34
Figure 11.	Interrupt Controller Block Diagram	46
Figure 12.	Timer Block Diagram	58
Figure 13.	UART Block Diagram	79
Figure 14.	UART Asynchronous Data Format without Parity	80
Figure 15.	UART Asynchronous Data Format with Parity	80
Figure 16.	UART Asynchronous Multiprocessor (9-bit) Mode Data Format	84
Figure 17.	Infrared Data Communication System Block Diagram	95
Figure 18.	Infrared Data Transmission	97
Figure 19.	Infrared Data Reception	98
Figure 20.	SPI Configured as a Master in a Single Master, Single Slave System	99
Figure 21.	SPI Configured as a Master in a Single Master, Multiple Slave System	100
Figure 22.	SPI Configured as a Slave	100
Figure 23.	SPI Timing When PHASE is 0	103
Figure 24.	SPI Timing When PHASE is 1	104
Figure 25.	7-Bit Addressed Slave Data Transfer Format	113
Figure 26.	10-Bit Addressed Slave Data Transfer Format	114
Figure 27.	Receive Data Transfer Format for a 7-Bit Addressed Slave	115
Figure 28.	Receive Data Format for a 10-Bit Addressed Slave	116
Figure 29.	Analog-to-Digital Converter Block Diagram	133
Figure 30.	Flash Memory Arrangement	139



Figure 31. Flash Controller Operation Flow Chart	140
Figure 32. On-Chip Debugger Block Diagram	151
Figure 33. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (1)	152
Figure 34. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (2)	153
Figure 35. OCD Data Format	154
Figure 36. Recommended Crystal Oscillator Configuration (20MHz operation)	166
Figure 37. Nominal ICC Versus System Clock Frequency	170
Figure 38. Nominal Halt Mode ICC Versus System Clock Frequency	171
Figure 39. Port Input Sample Timing	176
Figure 40. GPIO Port Output Timing	177
Figure 41. On-Chip Debugger Timing	178
Figure 42. SPI Master Mode Timing	179
Figure 43. SPI Slave Mode Timing	180
Figure 44. I ² C Timing	181
Figure 45. Flags Register	201
Figure 46. Opcode Map Cell Description	202
Figure 47. First Opcode Map	204
Figure 48. Second Opcode Map after 1FH	205
Figure 49. 40-Lead Plastic Dual-Inline Package (PDIP)	206
Figure 50. 44-Lead Low-Profile Quad Flat Package (LQFP)	207
Figure 51. 44-Lead Plastic Lead Chip Carrier Package (PLCC)	207
Figure 52. 64-Lead Low-Profile Quad Flat Package (LQFP)	208
Figure 53. 68-Lead Plastic Lead Chip Carrier Package (PLCC)	209
Figure 54. 80-Lead Quad-Flat Package (QFP)	210



List of Tables

Table 1.	Z8F640x Family Part Selection Guide	2
Table 2.	Z8F640x Family Package Options	6
Table 3.	Signal Descriptions	13
Table 4.	Pin Characteristics of the Z8F640x family	15
Table 5.	Z8F640x Family Program Memory Maps	18
Table 6.	Z8F640x Family Data Memory Maps	19
Table 7.	Register File Address Map	20
Table 8.	Reset and STOP Mode Recovery Characteristics and Latency	25
Table 9.	Reset Sources and Resulting Reset Type	26
Table 10.	STOP Mode Recovery Sources and Resulting Action	29
Table 11.	Port Availability by Device and Package Type	33
Table 12.	Port Alternate Function Mapping	35
Table 13.	Port A-H GPIO Address Registers (PxADDR)	37
Table 14.	GPIO Port Registers and Sub-Registers	37
Table 15.	Port A-H Control Registers (PxCTL)	38
Table 16.	Port A-H Data Direction Sub-Registers	39
Table 17.	Port A-H Alternate Function Sub-Registers	39
Table 18.	Port A-H Output Control Sub-Registers	40
Table 19.	Port A-H High Drive Enable Sub-Registers	41
Table 20.	Port A-H Input Data Registers (PxIN)	42
Table 21.	Port A-H STOP Mode Recovery Source Enable Sub-Registers	42
Table 22.	Port A-H Output Data Register (PxOUT)	43
Table 23.	Interrupt Vectors in Order of Priority	45
Table 24.	Interrupt Request 0 Register (IRQ0)	48
Table 25.	Interrupt Request 1 Register (IRQ1)	49
Table 26.	Interrupt Request 2 Register (IRQ2)	50
Table 27.	IRQ0 Enable and Priority Encoding	51
Table 28.	IRQ0 Enable High Bit Register (IRQ0ENH)	51
Table 29.	IRQ0 Enable Low Bit Register (IRQ0ENL)	52
Table 30.	IRQ1 Enable and Priority Encoding	52
Table 31.	IRQ1 Enable Low Bit Register (IRQ1ENL)	53



Table 32.	IRQ2 Enable and Priority Encoding	53
Table 33.	IRQ1 Enable High Bit Register (IRQ1ENH)	53
Table 34.	IRQ2 Enable Low Bit Register (IRQ2ENL)	54
Table 35.	IRQ2 Enable High Bit Register (IRQ2ENH)	54
Table 36.	Interrupt Edge Select Register (IRQES)	55
Table 37.	Interrupt Port Select Register (IRQPS)	55
Table 38.	Interrupt Control Register (IRQCTL)	56
Table 39.	Timer 0-3 High Byte Register (TxH)	67
Table 40.	Timer 0-3 Low Byte Register (TxL)	67
Table 41.	Timer 0-3 Reload High Byte Register (TxRH)	68
Table 42.	Timer 0-3 Reload Low Byte Register (TxRL)	68
Table 43.	Timer 0-3 PWM High Byte Register (TxPWHM)	69
Table 44.	Timer 0-3 PWM Low Byte Register (TxPWML)	69
Table 45.	Timer 0-3 Control Register (TxCTL)	70
Table 46.	Watch-Dog Timer Approximate Time-Out Delays	73
Table 47.	Watch-Dog Timer Control Register (WDTCTL)	75
Table 48.	Watch-Dog Timer Reload Upper Byte Register (WDTU)	76
Table 49.	Watch-Dog Timer Reload High Byte Register (WDTH)	76
Table 50.	Watch-Dog Timer Reload Low Byte Register (WDTL)	77
Table 51.	UARTx Transmit Data Register (UxTXD)	86
Table 52.	UARTx Receive Data Register (UxRXD)	87
Table 53.	UARTx Status 0 Register (UxSTAT0)	87
Table 54.	UARTx Control 0 Register (UxCTL0)	89
Table 55.	UARTx Status 1 Register (UxSTAT1)	89
Table 56.	UARTx Control 1 Register (UxCTL1)	90
Table 57.	UARTx Baud Rate High Byte Register (UxBRH)	91
Table 58.	UARTx Baud Rate Low Byte Register (UxBRL)	92
Table 59.	UART Baud Rates	93
Table 60.	SPI Clock Phase (PHASE) and Clock Polarity (CLKPOL) Operation	102
Table 61.	SPI Data Register (SPIDATA)	106
Table 62.	SPI Control Register (SPICTL)	107
Table 63.	SPI Status Register (SPISTAT)	108
Table 64.	SPI Mode Register (SPIMODE)	109
Table 65.	SPI Baud Rate High Byte Register (SPIBRH)	110
Table 66.	SPI Baud Rate Low Byte Register (SPIBRL)	110



Table 67.	I2C Data Register (I2CDATA)	118
Table 68.	I2C Status Register (I2CSTAT)	118
Table 69.	I2C Control Register (I2CCTL)	119
Table 70.	I2C Baud Rate High Byte Register (I2CBRH)	121
Table 71.	I2C Baud Rate Low Byte Register (I2CBRL)	121
Table 72.	DMAx Control Register (DMAxCTL)	124
Table 73.	DMAx I/O Address Register (DMAxIO)	126
Table 74.	DMAx Address High Nibble Register (DMAxH)	126
Table 75.	DMAx End Address Low Byte Register (DMAxEND)	128
Table 76.	DMAx Start/Current Address Low Byte Register (DMAxSTART)	128
Table 77.	DMA_ADC Register File Address Example	129
Table 78.	DMA_ADC Address Register (DMAA_ADDR)	129
Table 79.	DMA_ADC Control Register (DMAACTL)	130
Table 80.	DMA_ADC Status Register (DMAA_STAT)	131
Table 81.	ADC Control Register (ADCCTL)	135
Table 82.	ADC Data High Byte Register (ADCD_H)	137
Table 83.	ADC Data Low Bits Register (ADCD_L)	137
Table 84.	Z8F640x family Flash Memory Configurations	138
Table 85.	Flash Code Protection Using the Option Bits	142
Table 86.	Flash Control Register (FCTL)	144
Table 87.	Flash Status Register (FSTAT)	145
Table 88.	Flash Page Select Register (FPS)	146
Table 89.	Flash Frequency High Byte Register (FFREQH)	147
Table 90.	Flash Frequency Low Byte Register (FFREQL)	147
Table 91.	Option Bits At Program Memory Address 0000H	149
Table 92.	Options Bits at Program Memory Address 0001H	150
Table 93.	OCD Baud-Rate Limits	154
Table 94.	On-Chip Debugger Commands	156
Table 95.	OCD Control Register (OCDCTL)	161
Table 96.	OCD Status Register (OCDSTAT)	162
Table 97.	OCD Watchpoint Control/Address (WPTCTL)	163
Table 98.	OCD Watchpoint Address (WPTADDR)	164
Table 99.	OCD Watchpoint Data (WPTDATA)	164
Table 100.	Recommended Crystal Oscillator Specifications (20MHz Operation)	166



Table 101. Absolute Maximum Ratings	167
Table 102. DC Characteristics	169
Table 103. AC Characteristics	172
Table 104. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing	173
Table 105. Flash Memory Electrical Characteristics and Timing . . .	173
Table 106. Watch-Dog Timer Electrical Characteristics and Timing	174
Table 107. Analog-to-Digital Converter Electrical Characteristics and Timing	174
Table 108. GPIO Port Input Timing	176
Table 109. GPIO Port Output Timing	177
Table 110. On-Chip Debugger Timing	178
Table 111. SPI Master Mode Timing	179
Table 112. SPI Slave Mode Timing	180
Table 113. I2C Timing	181
Table 114. Assembly Language Syntax Example 1	183
Table 115. Assembly Language Syntax Example 2	183
Table 116. Notational Shorthand	184
Table 117. Additional Symbols	185
Table 118. Condition Codes	186
Table 119. Arithmetic Instructions	187
Table 120. Bit Manipulation Instructions	188
Table 121. Block Transfer Instructions	188
Table 122. CPU Control Instructions	189
Table 123. Load Instructions	189
Table 124. Logical Instructions	190
Table 125. Program Control Instructions	190
Table 126. Rotate and Shift Instructions	191
Table 127. eZ8 CPU Instruction Summary	191
Table 128. Opcode Map Abbreviations	203
Table 129. Ordering Information	211



Manual Objectives

This Product Specification provides detailed operating information for the Z8F640x, Z8F480x, Z8F320x, Z8F240x, and Z8F160x devices within the Z8 Encore![™] Microcontroller (MCU) family of products. Within this document, the Z8F640x, Z8F480x, Z8F320x, Z8F240x, and Z8F160x are referred to collectively as Z8 Encore![™] or the Z8F640x family unless specifically stated otherwise.

About This Manual

ZiLOG recommends that the user read and understand everything in this manual before setting up and using the product. However, we recognize that there are different styles of learning. Therefore, we have designed this Product Specification to be used either as a *how to* procedural manual or a reference guide to important data.

Intended Audience

This document is written for ZiLOG customers who are experienced at working with microcontrollers, integrated circuits, or printed circuit assemblies.

Manual Conventions

The following assumptions and conventions are adopted to provide clarity and ease of use:

Courier Typeface

Commands, code lines and fragments, bits, equations, hexadecimal addresses, and various executable items are distinguished from general text by the use of the `Courier` typeface. Where the use of the font is not indicated, as in the Index, the name of the entity is presented in upper case.

- Example: `FLAGS[1]` is `smrf`.

Hexadecimal Values

Hexadecimal values are designated by uppercase *H* suffix and appear in the `Courier` typeface.

- Example: R1 is set to `F8H`.

Brackets

The square brackets, `[]`, indicate a register or bus.

- Example: for the register `R1[7:0]`, R1 is an 8-bit register, `R1[7]` is the most significant bit, and `R1[0]` is the least significant bit.



Braces

The curly braces, { }, indicate a single register or bus created by concatenating some combination of smaller registers, buses, or individual bits.

- Example: the 12-bit register address {0H, RP[7:4], R1[3:0]} is composed of a 4-bit hexadecimal value (0H) and two 4-bit register values taken from the Register Pointer (RP) and Working Register R1. 0H is the most significant nibble (4-bit value) of the 12-bit register, and R1[3:0] is the least significant nibble of the 12-bit register.

Parentheses

The parentheses, (), indicate an indirect register address lookup.

- Example: (R1) is the memory location referenced by the address contained in the Working Register R1.

Parentheses/Bracket Combinations

The parentheses, (), indicate an indirect register address lookup and the square brackets, [], indicate a register or bus.

- *Example:* assume PC[15:0] contains the value 1234h. (PC[15:0]) then refers to the contents of the memory location at address 1234h.

Use of the Words *Set*, *Reset* and *Clear*

The word *set* implies that a register bit or a condition contains a logical 1. The words *reset* or *clear* imply that a register bit or a condition contains a logical 0. When either of these terms is followed by a number, the word *logical* may not be included; however, it is implied.

Notation for Bits and Similar Registers

A field of bits within a register is designated as: Register[n:n].

- Example: ADDR[15:0] refers to bits 15 through bit 0 of the Address.

Use of the Terms *LSB*, *MSB*, *lsb*, and *msb*

In this document, the terms *LSB* and *MSB*, when appearing in upper case, mean *least significant byte* and *most significant byte*, respectively. The lowercase forms, *lsb* and *msb*, mean *least significant bit* and *most significant bit*, respectively.

Use of Initial Uppercase Letters

Initial uppercase letters designate settings, modes, and conditions in general text.

- Example 1: Stop mode.
- Example 2: The receiver forces the SCL line to Low.
- The Master can generate a Stop condition to abort the transfer.



Use of All Uppercase Letters

The use of all uppercase letters designates the names of states and commands.

- Example 1: The bus is considered BUSY after the Start condition.
- Example 2: A START command triggers the processing of the initialization sequence.

Bit Numbering

Bits are numbered from 0 to $n-1$ where n indicates the total number of bits. For example, the 8 bits of a register are numbered from 0 to 7.

Safeguards

It is important that all users understand the following safety terms, which are defined here.



Caution: Indicates a procedure or file may become corrupted if the user does not follow directions.

Trademarks

ZiLOG, eZ8, Z8 Encore!, and Z8 are trademarks of [ZiLOG, Inc.](http://www.zilog.com) in the U.S.A. and other countries. All other trademarks are the property of their respective corporations.



Introduction

The Z8 Encore!® MCU family of products are the first in a line of ZiLOG microcontroller products based upon the new 8-bit eZ8 CPU. The Z8F640x/Z8F480x/Z8F320x/Z8F240x/Z8F160x products are referred to collectively as either Z8 Encore!® or the Z8F640x family. The Z8F640x family of products introduce Flash memory to ZiLOG's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8 CPU is upward compatible with existing Z8 instructions. The rich peripheral set of the Z8F640x family makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

Features

- eZ8 CPU, 20 MHz operation
- 12-channel, 10-bit analog-to-digital converter (ADC)
- 3-channel DMA
- Up to 64KB Flash memory with in-circuit programming capability
- Up to 4KB register RAM
- Serial communication protocols
 - Serial Peripheral Interface
 - I²C
- Two full-duplex 9-bit UARTs
- 24 interrupts with programmable priority
- Three or four 16-bit timers with capture, compare, and PWM capability
- Single-pin On-Chip Debugger
- Two Infrared Data Association (IrDA)-compliant infrared encoder/decoders integrated with the UARTs
- Watch-Dog Timer (WDT) with internal RC oscillator
- Up to 60 I/O pins
- Voltage Brown-out Protection (VBO)



- Power-On Reset (POR)
- 3.0-3.6V operating voltage with 5V-tolerant inputs
- 0° to +70°C standard temperature and -40° to +105°C extended temperature operating ranges

Part Selection Guide

Table 1 identifies the basic features and package styles available for each device within the Z8F640x family product line.

Table 1. Z8F640x Family Part Selection Guide

Part Number	Flash (KB)	RAM (KB)	I/O	16-bit Timers with PWM	ADC Inputs	UARTs with IrDA	I ² C	SPI	40/44-pin packages	64/68-pin packages	80-pin package
Z8F1601	16	2	31	3	8	2	1	1	X		
Z8F1602	16	2	46	4	12	2	1	1			X
Z8F2401	24	2	31	3	8	2	1	1	X		
Z8F2402	24	2	46	4	12	2	1	1			X
Z8F3201	32	2	31	3	8	2	1	1	X		
Z8F3202	32	2	46	4	12	2	1	1			X
Z8F4801	48	4	31	3	8	2	1	1	X		
Z8F4802	48	4	46	4	12	2	1	1			X
Z8F4803	48	4	60	4	12	2	1	1			X
Z8F6401	64	4	31	3	8	2	1	1	X		
Z8F6402	64	4	46	4	12	2	1	1			X
Z8F6403	64	4	60	4	12	2	1	1			X

Block Diagram

Figure 55 illustrates the block diagram of the architecture of the Z8 Encore![™].

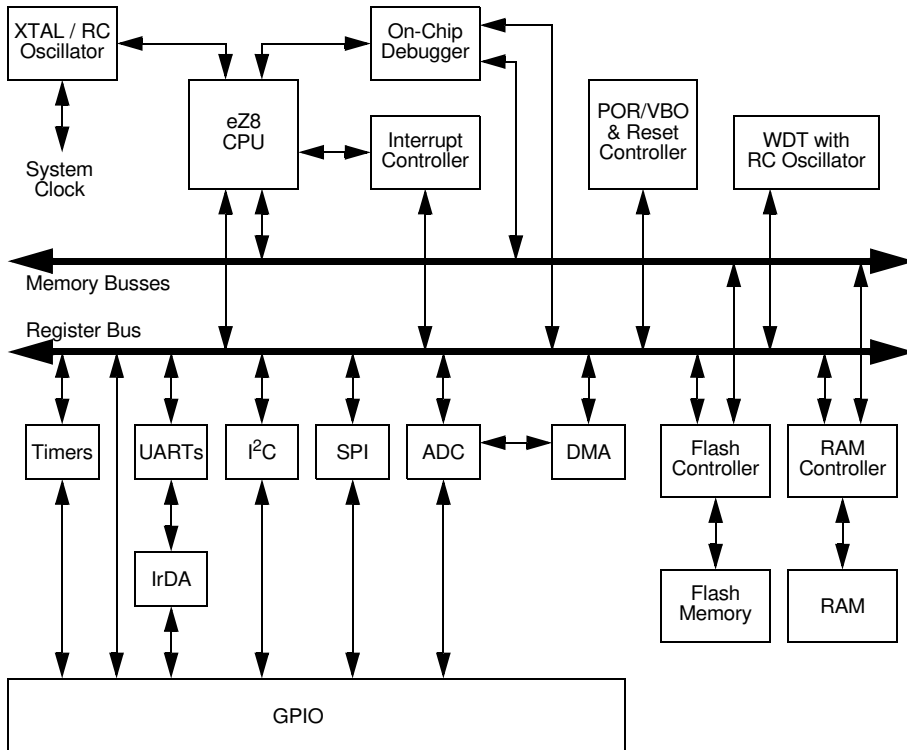


Figure 55. Z8 Encore![®] Block Diagram

CPU and Peripheral Overview

eZ8 CPU Features

The eZ8, ZiLOG's latest 8-bit Central Processing Unit (CPU), meets the continuing demand for faster and more code-efficient microcontrollers. The eZ8 CPU executes a superset of the original Z8 instruction set. The eZ8 CPU features include:

- Direct register-to-register architecture allows each register to function as an accumulator, improving execution time and decreasing the required program memory



- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks
- Compatible with existing Z8 code
- Expanded internal Register File allows access of up to 4KB
- New instructions improve execution efficiency for code developed using higher-level programming languages, including C
- Pipelined instruction fetch and execution
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT, and SRL
- New instructions support 12-bit linear addressing of the Register File
- Up to 10 MIPS operation
- C-Compiler friendly
- 2-9 clock cycles per instruction

For more information regarding the eZ8 CPU, refer to the *eZ8 CPU User Manual* available for download at www.zilog.com.

General Purpose I/O

The Z8 Encore!® features seven 8-bit ports (Ports A-G) and one 4-bit port (Port H) for general purpose I/O (GPIO). Each pin is individually programmable.

Flash Controller

The Flash Controller programs and erases the Flash memory.

10-Bit Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from up to 12 different analog input sources.

UARTs

Each UART is full-duplex and capable of handling asynchronous data transfers. The UARTs support 8- and 9-bit data modes and selectable parity.

I²C

The inter-integrated circuit (I²C®) controller makes the Z8 Encore!® compatible with the I²C protocol. The I²C controller consists of two bidirectional bus lines, a serial data (SDA) line and a serial clock (SCL) line.



Serial Peripheral Interface

The serial peripheral interface (SPI) allows the Z8 Encore!® to exchange data between other peripheral devices such as EEPROMs, A/D converters and ISDN devices. The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface.

Timers

Up to four 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in One-Shot, Continuous, Gated, Capture, Compare, Capture and Compare, and PWM modes. Only 3 timers (Timers 0-2) are available in the 40- and 44-pin packages.

Interrupt Controller

The Z8F640x family products support up to 24 interrupts. These interrupts consist of 12 internal and 12 general-purpose I/O pins. The interrupts have 3 levels of programmable interrupt priority.

Reset Controller

The Z8F640x family can be reset using the $\overline{\text{RESET}}$ pin, power-on reset, Watch-Dog Timer (WDT), Stop mode exit, or Voltage Brown-Out (VBO) warning signal.

On-Chip Debugger

The Z8 Encore!® features an integrated On-Chip Debugger (OCD). The OCD provides a rich set of debugging capabilities, such as reading and writing registers, programming the Flash, setting breakpoints and executing code. A single-pin interface provides communication to the OCD.

DMA Controller

The Z8F640x family features three channels of DMA. Two of the channels are for register RAM to and from I/O operations. The third channel automatically controls the transfer of data from the ADC to the memory.



Signal and Pin Descriptions

Overview

The Z8F640x family products are available in a variety of packages styles and pin configurations. This chapter describes the signals and available pin configurations for each of the package styles. For information regarding the physical package specifications, please refer to the chapter Packaging on page 206.

Available Packages

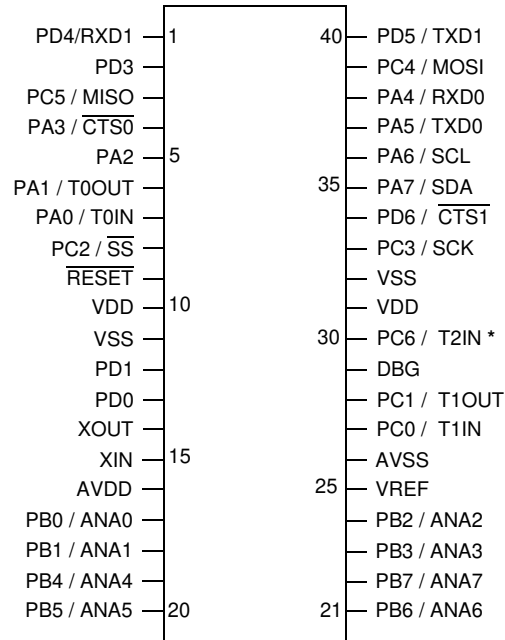
Table 2 identifies the package styles that are available for each device within the Z8F640x family product line.

Table 2. Z8F640x family Package Options

Part Number	40-pin PDIP	44-pin LQFP	44-pin PLCC	64-pin LQFP	68-pin PLCC	80-pin QFP
Z8F1601	X	X	X			
Z8F1602				X	X	
Z8F2401	X	X	X			
Z8F2402				X	X	
Z8F3201	X	X	X			
Z8F3202				X	X	
Z8F4801	X	X	X			
Z8F4802				X	X	
Z8F4803						X
Z8F6401	X	X	X			
Z8F6402				X	X	
Z8F6403						X

Pin Configurations

Figures 56 through 61 illustrate the pin configurations for all of the packages available in the Z8 Encore!® MCU family. Refer to Table 2 for a description of the signals.



Note: Timer 3 is not supported.

* T2OUT is not supported.

Figure 56. Z8Fxx01 in 40-Pin Dual Inline Package (DIP)