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Z8F640x, Z8F480x, Z8F320x, Z8F240x, and Z8F160x

Z8 Encore!™ Microcontrollers with Flash Memory and 10-Bit A/D Converter

Product Specification

PS017610-0404

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Document Disclaimer

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Manual Objectives

This Product Specification provides detailed operating information for the Z8F640x, Z8F480x, Z8F320x, Z8F240x, and Z8F160x devices within the Z8 Encore!™ Microcontroller (MCU) family of products. Within this document, the Z8F640x, Z8F480x, Z8F320x, Z8F240x, and Z8F160x are referred to collectively as Z8 Encore!™ or the Z8F640x family unless specifically stated otherwise.

About This Manual

ZiLOG recommends that the user read and understand everything in this manual before setting up and using the product. However, we recognize that there are different styles of learning. Therefore, we have designed this Product Specification to be used either as a *how to* procedural manual or a reference guide to important data.

Intended Audience

This document is written for ZiLOG customers who are experienced at working with microcontrollers, integrated circuits, or printed circuit assemblies.

Manual Conventions

The following assumptions and conventions are adopted to provide clarity and ease of use:

Courier Typeface

Commands, code lines and fragments, bits, equations, hexadecimal addresses, and various executable items are distinguished from general text by the use of the `Courier` typeface. Where the use of the font is not indicated, as in the Index, the name of the entity is presented in upper case.

- Example: FLAGS[1] is `smrf`.

Hexadecimal Values

Hexadecimal values are designated by uppercase *H* suffix and appear in the `Courier` typeface.

- Example: R1 is set to `F8H`.

Brackets

The square brackets, [ ], indicate a register or bus.

- Example: for the register R1[7:0], R1 is an 8-bit register, R1[7] is the most significant bit, and R1[0] is the least significant bit.

Braces

The curly braces, { }, indicate a single register or bus created by concatenating some combination of smaller registers, buses, or individual bits.

- Example: the 12-bit register address {0H, RP[7:4], R1[3:0]} is composed of a 4-bit hexadecimal value (0H) and two 4-bit register values taken from the Register Pointer (RP) and Working Register R1. 0H is the most significant nibble (4-bit value) of the 12-bit register, and R1[3:0] is the least significant nibble of the 12-bit register.

Parentheses

The parentheses, ( ), indicate an indirect register address lookup.

- Example: (R1) is the memory location referenced by the address contained in the Working Register R1.

Parentheses/Bracket Combinations

The parentheses, ( ), indicate an indirect register address lookup and the square brackets, [ ], indicate a register or bus.

- *Example:* assume PC[15:0] contains the value 1234h. (PC[15:0]) then refers to the contents of the memory location at address 1234h.

Use of the Words *Set*, *Reset* and *Clear*

The word *set* implies that a register bit or a condition contains a logical 1. The words re*set* or *clear* imply that a register bit or a condition contains a logical 0. When either of these terms is followed by a number, the word *logical* may not be included; however, it is implied.

Notation for Bits and Similar Registers

A field of bits within a register is designated as: Register[*n*:*n*].

- Example: ADDR[15:0] refers to bits 15 through bit 0 of the Address.

Use of the Terms *LSB*, *MSB*, *lsb*, and *msb*

In this document, the terms *LSB* and *MSB,* when appearing in upper case, mean *least significant byte* and *most significant byte*, respectively. The lowercase forms, *lsb* and *msb*, mean *least significant bit* and *most significant bit*, respectively.

Use of Initial Uppercase Letters

Initial uppercase letters designate settings, modes, and conditions in general text.

- Example 1: Stop mode.
- Example 2: The receiver forces the SCL line to Low.
- The Master can generate a Stop condition to abort the transfer.

Use of All Uppercase Letters

The use of all uppercase letters designates the names of states and commands.

- Example 1: The bus is considered BUSY after the Start condition.
- Example 2: A START command triggers the processing of the initialization sequence.

Bit Numbering

Bits are numbered from *0* to *n–1* where *n* indicates the total number of bits. For example, the 8 bits of a register are numbered from 0 to 7.

Safeguards

It is important that all users understand the following safety terms, which are defined here.

Caution: Indicates a procedure or file may become corrupted if the user does not follow directions.

Trademarks

Introduction

The Z8 Encore!® MCU family of products are the first in a line of ZiLOG microcontroller products based upon the new 8-bit eZ8 CPU. The Z8F640x/Z8F480x/Z8F320x/Z8F240x/Z8F160x products are referred to collectively as either Z8 Encore!® or the Z8F640x family. The Z8F640x family of products introduce Flash memory to ZiLOG's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8 CPU is upward compatible with existing Z8 instructions. The rich peripheral set of the Z8F640x family makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

Features

- eZ8 CPU, 20 MHz operation
- 12-channel, 10-bit analog-to-digital converter (ADC)
- 3-channel DMA
- Up to 64KB Flash memory with in-circuit programming capability
- Up to 4KB register RAM
- Serial communication protocols
  - Serial Peripheral Interface
  - I^2C
- Two full-duplex 9-bit UARTs
- 24 interrupts with programmable priority
- Three or four 16-bit timers with capture, compare, and PWM capability
- Single-pin On-Chip Debugger
- Two Infrared Data Association (IrDA)-compliant infrared encoder/decoders integrated with the UARTs
- Watch-Dog Timer (WDT) with internal RC oscillator
- Up to 60 I/O pins
- Voltage Brown-out Protection (VBO)

- Power-On Reset (POR)
- 3.0-3.6V operating voltage with 5V-tolerant inputs
- 0° to +70°C standard temperature and -40° to +105°C extended temperature operating ranges

Part Selection Guide

Table 1 identifies the basic features and package styles available for each device within the Z8F640x family product line.

Table 1. Z8F640x Family Part Selection Guide

Part Number	Flash (KB)	RAM (KB)	I/O	16-bit Timers with PWM	ADC Inputs	UARTs with IrDA	I^2C	SPI	40/44-pin packages	64/68-pin packages	80-pin package
Z8F1601	16	2	31	3	8	2	1	1	X		
Z8F1602	16	2	46	4	12	2	1	1		X	
Z8F2401	24	2	31	3	8	2	1	1	X		
Z8F2402	24	2	46	4	12	2	1	1		X	
Z8F3201	32	2	31	3	8	2	1	1	X		
Z8F3202	32	2	46	4	12	2	1	1		X	
Z8F4801	48	4	31	3	8	2	1	1	X		
Z8F4802	48	4	46	4	12	2	1	1		X	
Z8F4803	48	4	60	4	12	2	1	1			X
Z8F6401	64	4	31	3	8	2	1	1	X		
Z8F6402	64	4	46	4	12	2	1	1		X	
Z8F6403	64	4	60	4	12	2	1	1			X

Block Diagram

Figure 55 illustrates the block diagram of the architecture of the Z8 Encore!™.

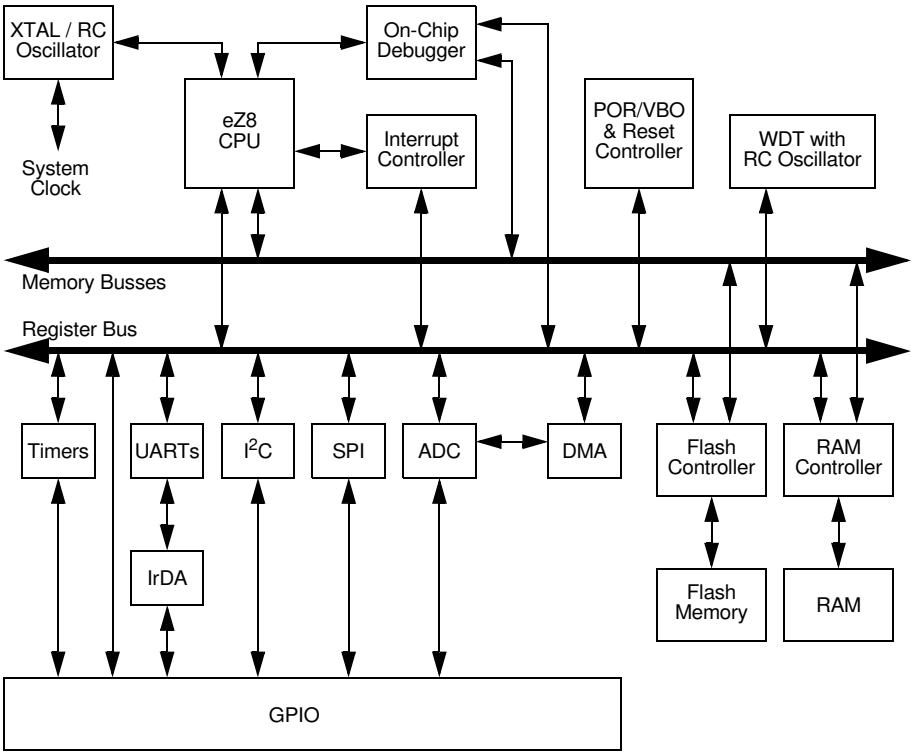


Figure 55. Z8 Encore!® Block Diagram

CPU and Peripheral Overview

eZ8 CPU Features

The eZ8, ZiLOG's latest 8-bit Central Processing Unit (CPU), meets the continuing demand for faster and more code-efficient microcontrollers. The eZ8 CPU executes a superset of the original Z8 instruction set. The eZ8 CPU features include:

- Direct register-to-register architecture allows each register to function as an accumulator, improving execution time and decreasing the required program memory

- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks
- Compatible with existing Z8 code
- Expanded internal Register File allows access of up to 4KB
- New instructions improve execution efficiency for code developed using higher-level programming languages, including C
- Pipelined instruction fetch and execution
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT, and SRL
- New instructions support 12-bit linear addressing of the Register File
- Up to 10 MIPS operation
- C-Compiler friendly
- 2-9 clock cycles per instruction

For more information regarding the eZ8 CPU, refer to the *eZ8 CPU User Manual* available for download at www.zilog.com.

General Purpose I/O

The Z8 Encore!® features seven 8-bit ports (Ports A-G) and one 4-bit port (Port H) for general purpose I/O (GPIO). Each pin is individually programmable.

Flash Controller

The Flash Controller programs and erases the Flash memory.

10-Bit Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from up to 12 different analog input sources.

UARTs

Each UART is full-duplex and capable of handling asynchronous data transfers. The UARTs support 8- and 9-bit data modes and selectable parity.

I^2C

The inter-integrated circuit (I^2C®) controller makes the Z8 Encore!® compatible with the I^2C protocol. The I^2C controller consists of two bidirectional bus lines, a serial data (SDA) line and a serial clock (SCL) line.

Serial Peripheral Interface

The serial peripheral interface (SPI) allows the Z8 Encore!® to exchange data between other peripheral devices such as EEPROMs, A/D converters and ISDN devices. The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface.

Timers

Up to four 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in One-Shot, Continuous, Gated, Capture, Compare, Capture and Compare, and PWM modes. Only 3 timers (Timers 0-2) are available in the 40- and 44-pin packages.

Interrupt Controller

The Z8F640x family products support up to 24 interrupts. These interrupts consist of 12 internal and 12 general-purpose I/O pins. The interrupts have 3 levels of programmable interrupt priority.

Reset Controller

The Z8F640x family can be reset using the $\overline{\text{RESET}}$ pin, power-on reset, Watch-Dog Timer (WDT), Stop mode exit, or Voltage Brown-Out (VBO) warning signal.

On-Chip Debugger

The Z8 Encore!® features an integrated On-Chip Debugger (OCD). The OCD provides a rich set of debugging capabilities, such as reading and writing registers, programming the Flash, setting breakpoints and executing code. A single-pin interface provides communication to the OCD.

DMA Controller

The Z8F640x family features three channels of DMA. Two of the channels are for register RAM to and from I/O operations. The third channel automatically controls the transfer of data from the ADC to the memory.

Signal and Pin Descriptions

Overview

The Z8F640x family products are available in a variety of packages styles and pin configurations. This chapter describes the signals and available pin configurations for each of the package styles. For information regarding the physical package specifications, please refer to the chapter Packaging on page 206.

Available Packages

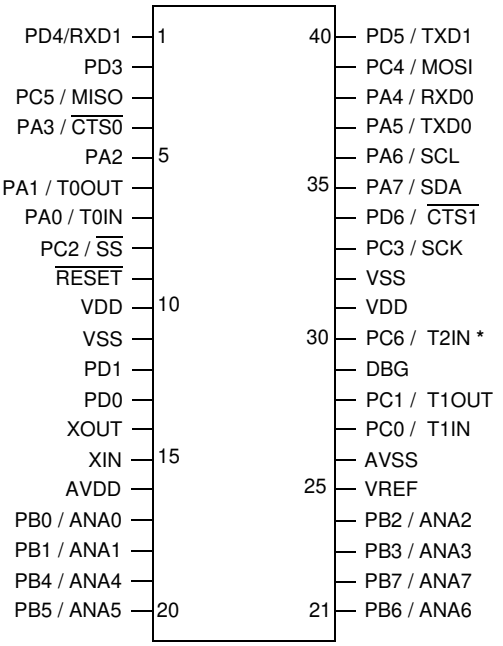
Table 2 identifies the package styles that are available for each device within the Z8F640x family product line.

Table 2. Z8F640x family Package Options

Part Number	40-pin PDIP	44-pin LQFP	44-pin PLCC	64-pin LQFP	68-pin PLCC	80-pin QFP
Z8F1601	X	X	X			
Z8F1602				X	X	
Z8F2401	X	X	X			
Z8F2402				X	X	
Z8F3201	X	X	X			
Z8F3202				X	X	
Z8F4801	X	X	X			
Z8F4802				X	X	
Z8F4803						X
Z8F6401	X	X	X			
Z8F6402				X	X	
Z8F6403						X

Pin Configurations

Figures 56 through 61 illustrate the pin configurations for all of the packages available in the Z8 Encore!® MCU family. Refer to Table 2 for a description of the signals.



Note: Timer 3 is not supported.

* T2OUT is not supported.

Figure 56. Z8Fxx01 in 40-Pin Dual Inline Package (DIP)