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**High Performance 8-Bit Microcontrollers**

**Z8 Encore! XP<sup>®</sup> 64K Series  
Flash Microcontrollers**

**Product Specification**

PS019919-1207



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## Revision History

Each instance in the Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages or appropriate links given in the table below.

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# Manual Objectives

This Product Specification provides detailed operating information for the Flash devices within Zilog's Z8 Encore! XP<sup>®</sup> 64K Series Flash Microcontrollers Microcontroller (MCU) products. Within this document, the Z8F642x, Z8F482x, Z8F322x, Z8F242x, and Z8F162x devices are referred to collectively as the Z8 Encore! XP<sup>®</sup> 64K Series Flash Microcontrollers unless specifically stated otherwise.

## About This Manual

Zilog<sup>®</sup> recommends that you read and understand everything in this manual before setting up and using the product. However, we recognize that there are different styles of learning. Therefore, we have designed this Product Specification to be used either as a *how to* procedural manual or a reference guide to important data.

## Intended Audience

This document is written for Zilog customers who are experienced at working with microcontrollers, integrated circuits, or printed circuit assemblies.

## Manual Conventions

The following assumptions and conventions are adopted to provide clarity and ease of use:

### Courier Typeface

Commands, code lines and fragments, bits, equations, hexadecimal addresses, and various executable items are distinguished from general text by the use of the `Courier` typeface. Where the use of the font is not indicated, as in the Index, the name of the entity is presented in upper case.

- Example: `FLAGS[1]` is `smrf`.

### Hexadecimal Values

Hexadecimal values are designated by uppercase *H* suffix and appear in the `Courier` typeface.

- Example: R1 is set to `F8H`.

### Brackets

The square brackets, `[ ]`, indicate a register or bus.

- Example: For the register `R1[7:0]`, R1 is an 8-bit register, `R1[7]` is the most significant bit, and `R1[0]` is the least significant bit.

## Braces

The curly braces, { }, indicate a single register or bus created by concatenating some combination of smaller registers, buses, or individual bits.

- Example: The 12-bit register address {0H, RP[7:4], R1[3:0]} is composed of a 4-bit hexadecimal value (0H) and two 4-bit register values taken from the Register Pointer (RP) and Working Register R1. 0H is the most-significant nibble (4-bit value) of the 12-bit register, and R1[3:0] is the least significant nibble of the 12-bit register.

## Parentheses

The parentheses, ( ), indicate an indirect register address lookup.

- Example: (R1) is the memory location referenced by the address contained in the Working Register R1.

## Parentheses/Bracket Combinations

The parentheses, ( ), indicate an indirect register address lookup and the square brackets, [ ], indicate a register or bus.

- Example: Assume PC[15:0] contains the value 1234h. (PC[15:0]) then refers to the contents of the memory location at address 1234h.

## Use of the Words *Set*, *Reset* and *Clear*

The word *set* implies that a register bit or a condition contains a logical 1. The words *reset* or *clear* imply that a register bit or a condition contains a logical 0. When either of these terms is followed by a number, the word *logical* may not be included; however, it is implied.

## Notation for Bits and Similar Registers

A field of bits within a register is designated as: Register[n:n].

- Example: ADDR[15:0] refers to bits 15 through bit 0 of the Address.

## Use of the Terms *LSB*, *MSB*, *lsb*, and *msb*

In this document, the terms *LSB* and *MSB*, when appearing in upper case, mean *least significant byte* and *most significant byte*, respectively. The lowercase forms, *lsb* and *msb*, mean *least significant bit* and *most significant bit*, respectively.

## Use of Initial Uppercase Letters

Initial uppercase letters designate settings and conditions in general text.

- Example 1: The receiver forces the SCL line to Low.
- Example 2: The Master can generate a Stop condition to abort the transfer.



### Use of All Uppercase Letters

The use of all uppercase letters designates the names of states, modes, and commands.

- Example 1: The bus is considered BUSY after the Start condition.
- Example 2: A START command triggers the processing of the initialization sequence.
- Example 3: STOP mode.

### Bit Numbering

Bits are numbered from 0 to  $n-1$  where  $n$  indicates the total number of bits. For example, the 8 bits of a register are numbered from 0 to 7.

### Safeguards

It is important that you understand the following safety terms, which are defined here.



**Caution:**

*Indicates a procedure or file may become corrupted if you do not follow directions.*

# Introduction

Zilog's Z8 Encore! XP MCU family of products are a line of Zilog<sup>®</sup> microcontroller products based upon the 8-bit eZ8 CPU. The Z8 Encore! XP<sup>®</sup> 64K Series Flash Microcontrollers, hereafter referred to collectively as the Z8 Encore! XP or the 64K Series adds Flash memory to Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8<sup>™</sup> CPU is upward compatible with existing Z8<sup>®</sup> instructions. The rich-peripheral set of the Z8 Encore! XP makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

## Features

The features of Z8 Encore! XP 64K Series Flash Microcontrollers include:

- 20 MHz eZ8 CPU
- Up to 64 KB Flash with in-circuit programming capability
- Up to 4 KB register RAM
- 12-channel, 10-bit Analog-to-Digital Converter (ADC)
- Two full-duplex 9-bit UARTs with bus transceiver Driver Enable control
- Inter-integrated circuit (I<sup>2</sup>C)
- Serial Peripheral Interface (SPI)
- Two Infrared Data Association (IrDA)-compliant infrared encoder/decoders
- Up to four 16-bit timers with capture, compare, and PWM capability
- Watchdog Timer (WDT) with internal RC oscillator
- Three-channel DMA
- Up to 60 input/output (I/O) pins
- 24 interrupts with configurable priority
- On-Chip Debugger
- Voltage Brownout (VBO) Protection
- Power-On Reset (POR)
- Operating voltage of 3.0 V to 3.6 V with 5 V-tolerant inputs
- 0 °C to +70 °C, -40 °C to +105 °C, and -40 °C to +125 °C operating temperature ranges

## Part Selection Guide

Table 1 identifies the basic features and package styles available for each device within the Z8 Encore! XP product line.

**Table 1. Z8 Encore! XP 64K Series Flash Microcontrollers Part Selection Guide**

Part Number	Flash (KB)	RAM (KB)	I/O	16-bit Timers with PWM	ADC Inputs	UARTs with IrDA	I <sup>2</sup> C	SPI	40/44-pin packages	64/68-pin packages	80-pin package
Z8F1621	16	2	31	3	8	2	1	1	X		
Z8F1622	16	2	46	4	12	2	1	1		X	
Z8F2421	24	2	31	3	8	2	1	1	X		
Z8F2422	24	2	46	4	12	2	1	1		X	
Z8F3221	32	2	31	3	8	2	1	1	X		
Z8F3222	32	2	46	4	12	2	1	1		X	
Z8F4821	48	4	31	3	8	2	1	1	X		
Z8F4822	48	4	46	4	12	2	1	1		X	
Z8F4823	48	4	60	4	12	2	1	1			X
Z8F6421	64	4	31	3	8	2	1	1	X		
Z8F6422	64	4	46	4	12	2	1	1		X	
Z8F6423	64	4	60	4	12	2	1	1			X

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## Block Diagram

Figure 1 displays the block diagram of the architecture of the Z8 Encore! XP 64K Series Flash Microcontrollers.

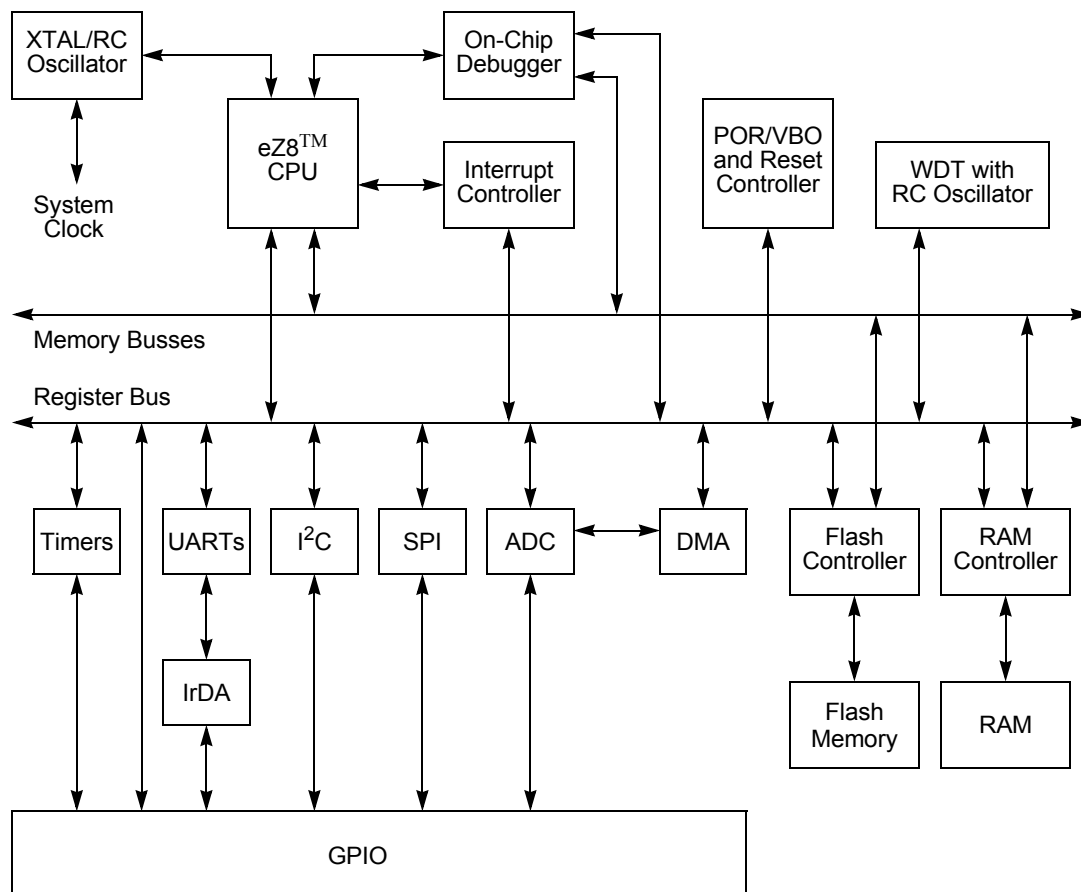


Figure 1. Z8 Encore! XP 64K Series Flash Microcontrollers Block Diagram

## CPU and Peripheral Overview

### eZ8™ CPU Features

The latest 8-bit eZ8 CPU meets the continuing demand for faster and more code-efficient microcontrollers. The eZ8 CPU executes a superset of the original Z8<sup>®</sup> instruction set.

The eZ8 CPU features include:

- Direct register-to-register architecture allows each register to function as an accumulator, improving execution time and decreasing the required Program Memory
- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks
- Compatible with existing Z8 code
- Expanded internal Register File allows access of up to 4 KB
- New instructions improve execution efficiency for code developed using higher-level programming languages, including C
- Pipelined instruction fetch and execution
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT, and SRL
- New instructions support 12-bit linear addressing of the Register File
- Up to 10 MIPS operation
- C-Compiler friendly
- 2 to 9 clock cycles per instruction

For more information on the eZ8 CPU, refer to *eZ8<sup>™</sup> CPU Core User Manual (UM0128)* available for download at [www.zilog.com](http://www.zilog.com).

## General-Purpose Input/Output

The 64K Series features seven 8-bit ports (Ports A-G) and one 4-bit port (Port H) for general-purpose input/output (GPIO). Each pin is individually programmable. All ports (except B and H) support 5 V-tolerant inputs.

## Flash Controller

The Flash Controller programs and erases the Flash memory.

## 10-Bit Analog-to-Digital Converter

The Analog-to-Digital Converter converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from up to 12 different analog input sources.

## UARTs

Each UART is full-duplex and capable of handling asynchronous data transfers. The UARTs support 8- and 9-bit data modes, selectable parity, and an efficient bus transceiver Driver Enable signal for controlling a multi-transceiver bus, such as RS-485.

## I<sup>2</sup>C

The I<sup>2</sup>C controller makes the Z8 Encore! XP compatible with the I<sup>2</sup>C protocol. The I<sup>2</sup>C controller consists of two bidirectional bus lines, a serial data (SDA) line and a serial clock (SCL) line.

## Serial Peripheral Interface

The serial peripheral interface allows the Z8 Encore! XP to exchange data between other peripheral devices such as EEPROMs, A/D converters and ISDN devices. The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface.

## Timers

Up to four 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in One-Shot, Continuous, Gated, Capture, Compare, Capture and Compare, and PWM modes. Only 3 timers (Timers 0-2) are available in the 44-pin packages.

## Interrupt Controller

The 64K Series products support up to 24 interrupts. These interrupts consist of 12 internal and 12 GPIO pins. The interrupts have 3 levels of programmable interrupt priority.

## Reset Controller

The Z8 Encore! can be reset using the  $\overline{\text{RESET}}$  pin, Power-On Reset, Watchdog Timer, STOP mode exit, or Voltage Brownout (VBO) warning signal.

## On-Chip Debugger

The Z8 Encore! XP features an integrated On-Chip Debugger. The OCD provides a rich set of debugging capabilities, such as reading and writing registers, programming the Flash, setting breakpoints and executing code. A single-pin interface provides communication to the OCD.

## DMA Controller

The 64K Series features three channels of DMA. Two of the channels are for register RAM to and from I/O operations. The third channel automatically controls the transfer of data from the ADC to the memory.





# Signal and Pin Descriptions

## Overview

The Z8 Encore! XP 64K Series Flash Microcontrollers product are available in a variety of packages styles and pin configurations. This chapter describes the signals and available pin configurations for each of the package styles. For information on physical package specifications, see [Packaging](#) on page 265.

## Available Packages

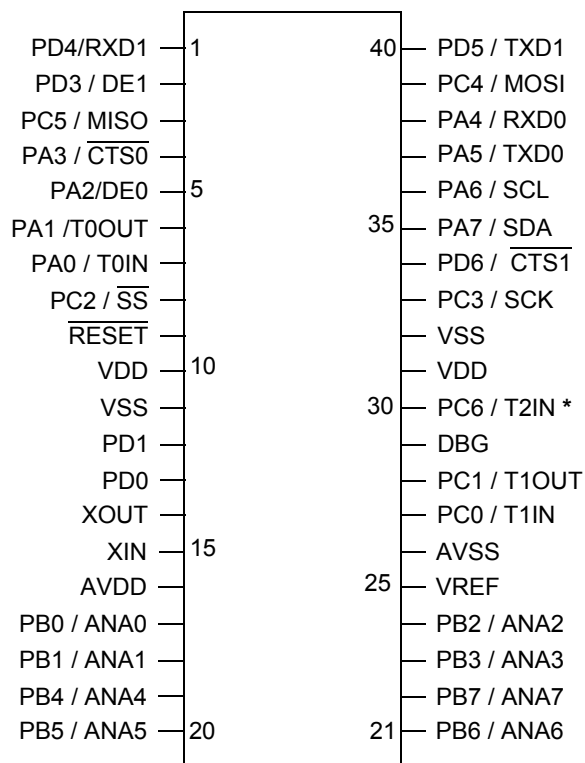
[Table 2](#) identifies the package styles that are available for each device within the Z8 Encore! XP 64K Series Flash Microcontrollers product line.

**Table 2. Z8 Encore! XP 64K Series Flash Microcontrollers Package Options**

Part Number	40-Pin PDIP	44-pin LQFP	44-pin PLCC	64-pin LQFP	68-pin PLCC	80-pin QFP
Z8F1621	X	X	X			
Z8F1622				X	X	
Z8F2421	X	X	X			
Z8F2422				X	X	
Z8F3221	X	X	X			
Z8F3222				X	X	
Z8F4821	X	X	X			
Z8F4822				X	X	
Z8F4823						X
Z8F6421	X	X	X			
Z8F6422				X	X	
Z8F6423						X

## Pin Configurations

Figure 2 through Figure 7 on page 13 display the pin configurations for all of the packages available in the Z8 Encore! XP 64K Series Flash Microcontrollers. For description of the signals, see Table 3 on page 14. Timer 3 is not available in the 40-pin and 44-pin packages.



**Note:** Timer 3 is not supported.

\* T2OUT is not supported.

**Figure 2. Z8 Encore! XP 64K Series Flash Microcontrollers in 40-Pin Dual Inline Package (PDIP)**

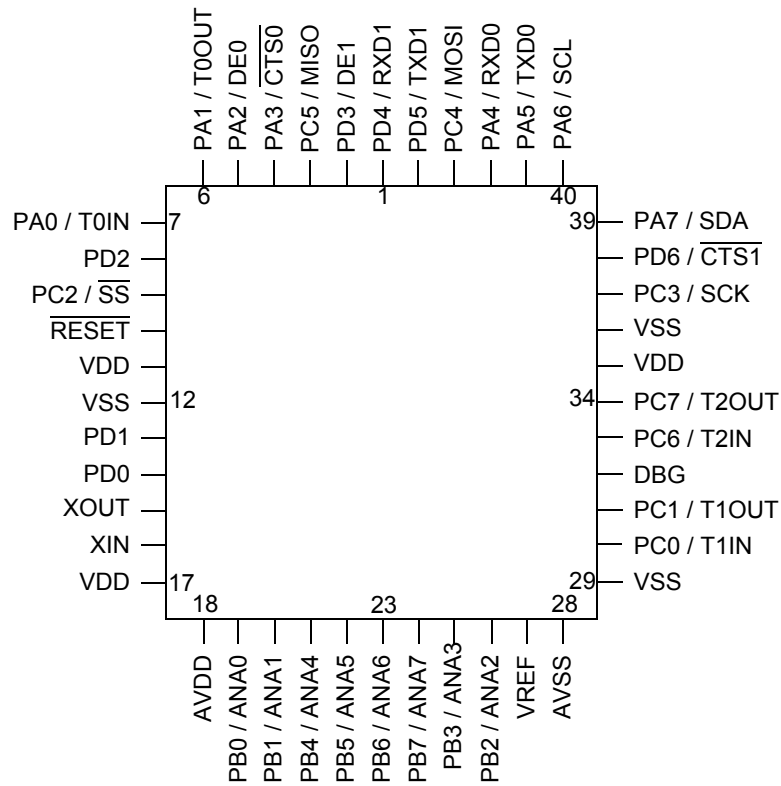


Figure 3. Z8 Encore! XP 64K Series Flash Microcontrollers in 44-Pin Plastic Leaded Chip Carrier (PLCC)

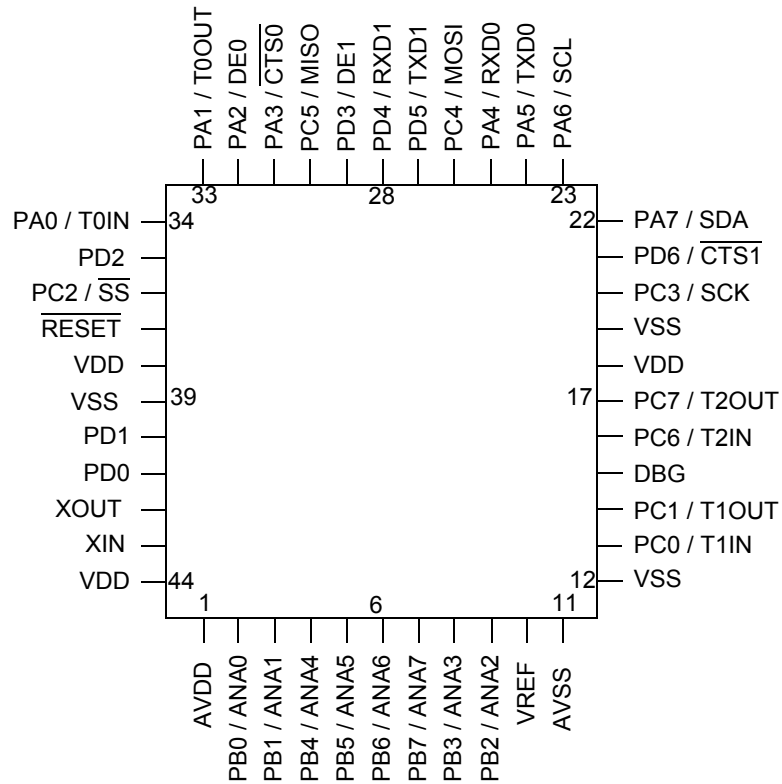


Figure 4. Z8 Encore! XP 64K Series Flash Microcontrollers in 44-Pin Low-Profile Quad Flat Package (LQFP)

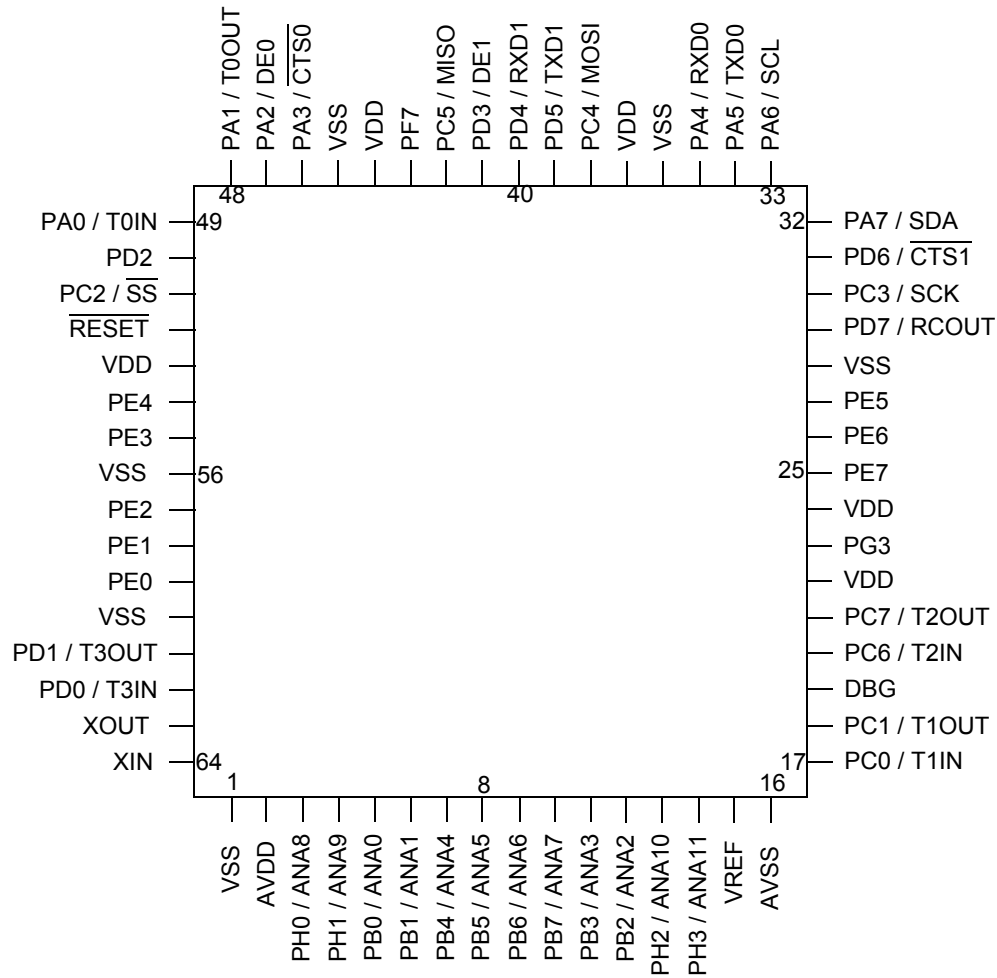


Figure 5. Z8 Encore! XP 64K Series Flash Microcontrollers in 64-Pin Low-Profile Quad Flat Package (LQFP)