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Z8S180/Z8L180

ENHANCED Z180 MICROPROCESSOR
OFFERS FASTER EXECUTION,
POWER-SAVER MODE, LOW EMI

FEATURES

- Code Compatible with ZiLOG Z80[®] CPU
- Extended Instructions
- Two Chain-Linked DMA Channels
- Low Power-Down Modes
- On-Chip Interrupt Controllers
- Three On-Chip Wait-State Generators
- On-Chip Oscillator/Generator
- Expanded MMU Addressing (Up to 1 MB)
- Clocked Serial I/O Port
- Two 16-Bit Counter/Timers
- Two Enhanced UARTs (up to 512 Kbps)
- Clock Speeds: 10, 20, 33 MHz
- Operating Range: 5V (3.3V @ 20 MHz)
- Operating Temperature Range: 0°C to +70°C
- -40°C to +85°C Extended Temperature Range
- Three Packaging Styles
 - 68-Pin PLCC
 - 64-Pin DIP
 - 80-Pin QFP

GENERAL DESCRIPTION

The enhanced Z8S180/Z8L180[™] significantly improves on previous Z80180 models, while still providing full backward compatibility with existing ZiLOG Z80 devices. The Z8S180/Z8L180 now offers faster execution speeds, power-saving modes, and EMI noise reduction.

This enhanced Z180[™] design also incorporates additional feature enhancements to the ASCIs, DMAs, and STANDBY mode power consumption. With the addition of ESCC-like Baud Rate Generators (BRGs), the two ASCIs offer the flexibility and capability to transfer data asynchronously at rates of up to 512 Kbps. In addition, the ASCI receiver features a 4-byte first in/first out (FIFO) buffer which reduces the likelihood of overrun errors. The DMAs have been modified to allow for chain-linking of the two DMA channels when set to take their DMA requests from the same peripherals device. This feature allows for nonstop DMA operation between the two DMA channels.

Not only does the Z8S180/Z8L180 consume less power during normal operations than the previous model, it offers

three modes intended to further reduce power consumption. Power consumption during STANDBY Mode is reduced to 10 μ A by stopping the external oscillators and internal clock. The SLEEP mode reduces power by placing the CPU into a stopped state, consuming less current while the on-chip I/O devices still operate. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a stopped mode, reducing power consumption even further.

A new clock-doubler feature in the Z8S180/Z8L180 allows the internal clock speed to be twice the external clock speed. As a result, system cost is reduced by allowing the use of lower-cost, lower-frequency crystals.

The Enhanced Z180 is housed in 80-pin QFP, 68-pin PLCC, and 64-pin DIP packages.

Note: All Signals with an overline are active Low. For example: B/W, in which WORD is active Low; or B/W, in which BYTE is active Low.

GENERAL DESCRIPTION (Continued)

Power connections follow the conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

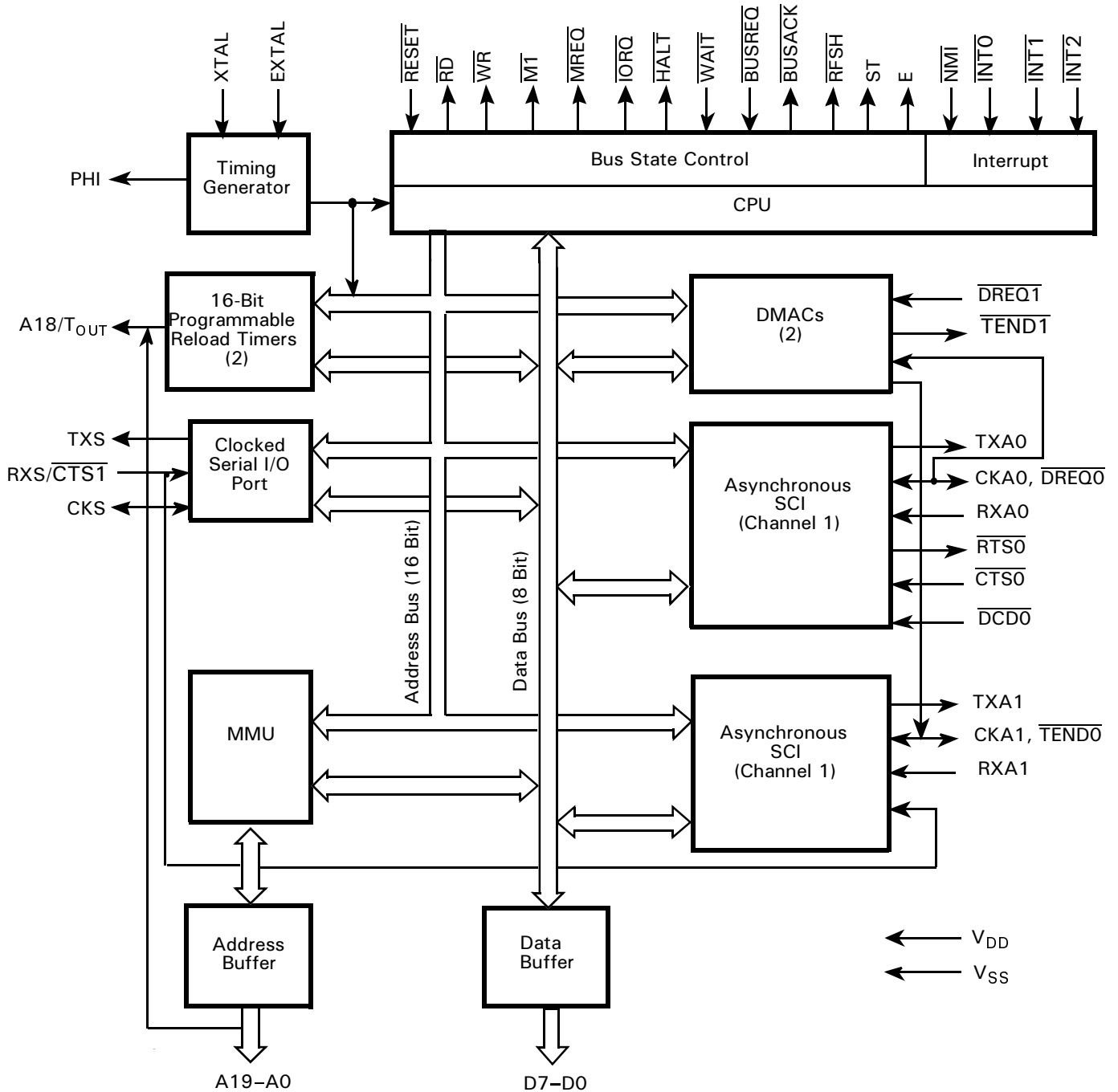


Figure 1. Z8S180/Z8L180 Functional Block Diagram

PIN IDENTIFICATION

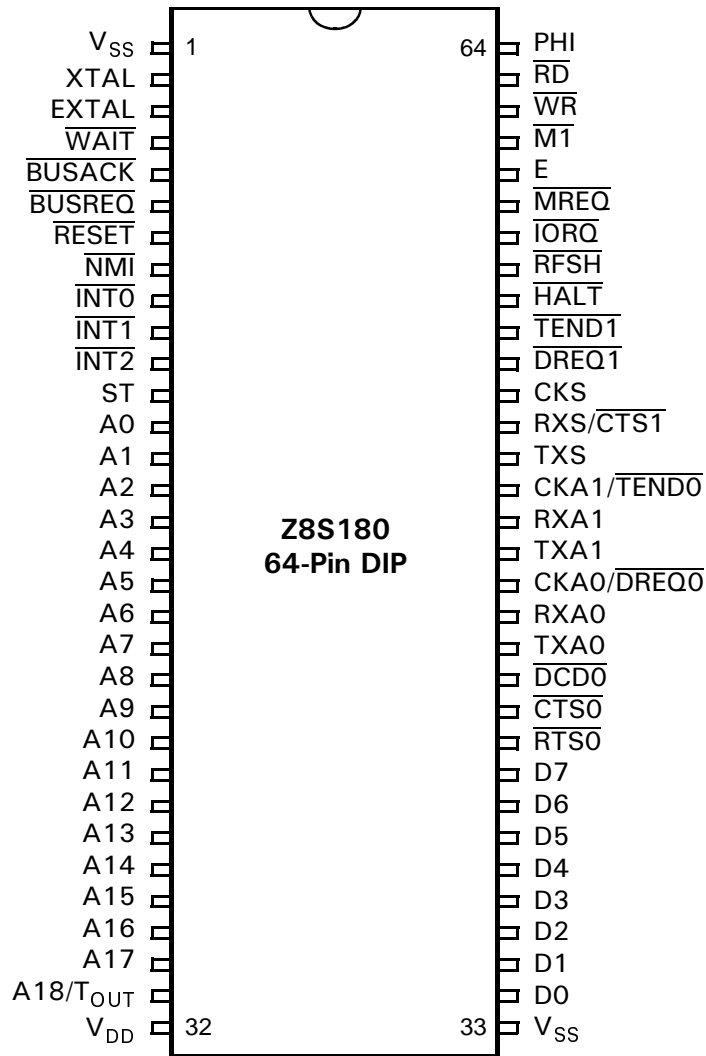


Figure 2. Z8S180 64-Pin DIP Pin Configuration

PIN IDENTIFICATION (Continued)

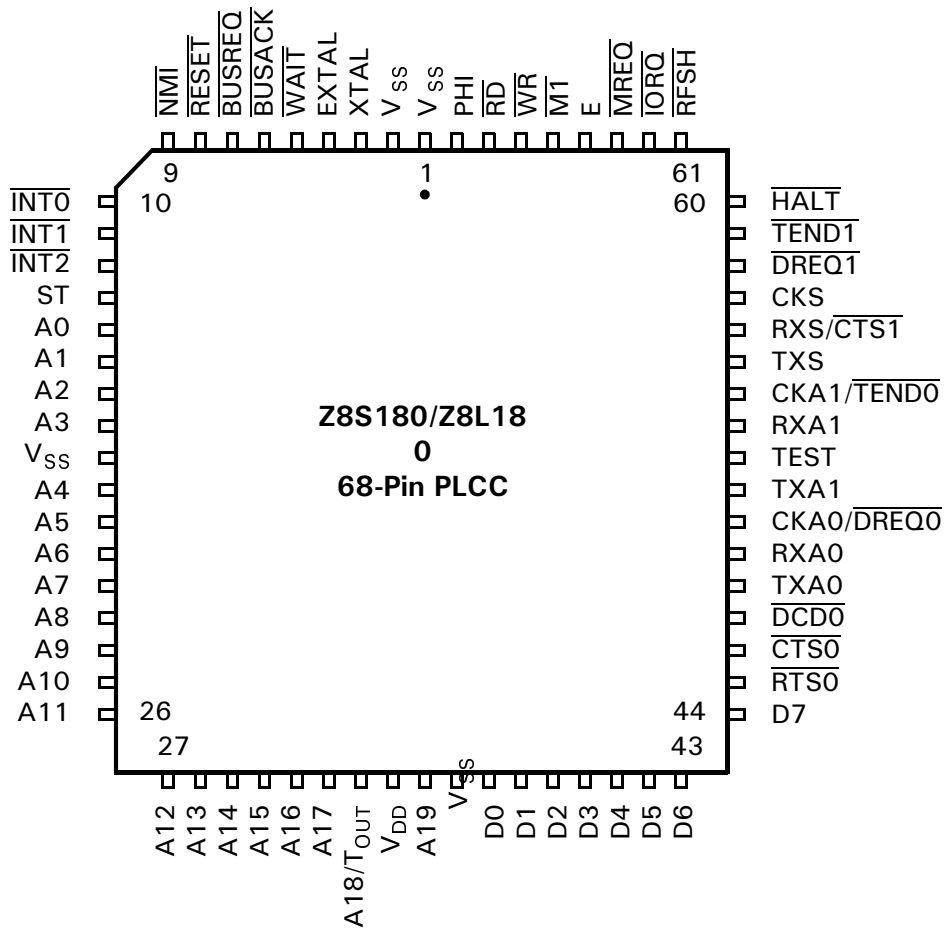


Figure 3. Z8S180/Z8L180 68-Pin PLCC Pin Configuration

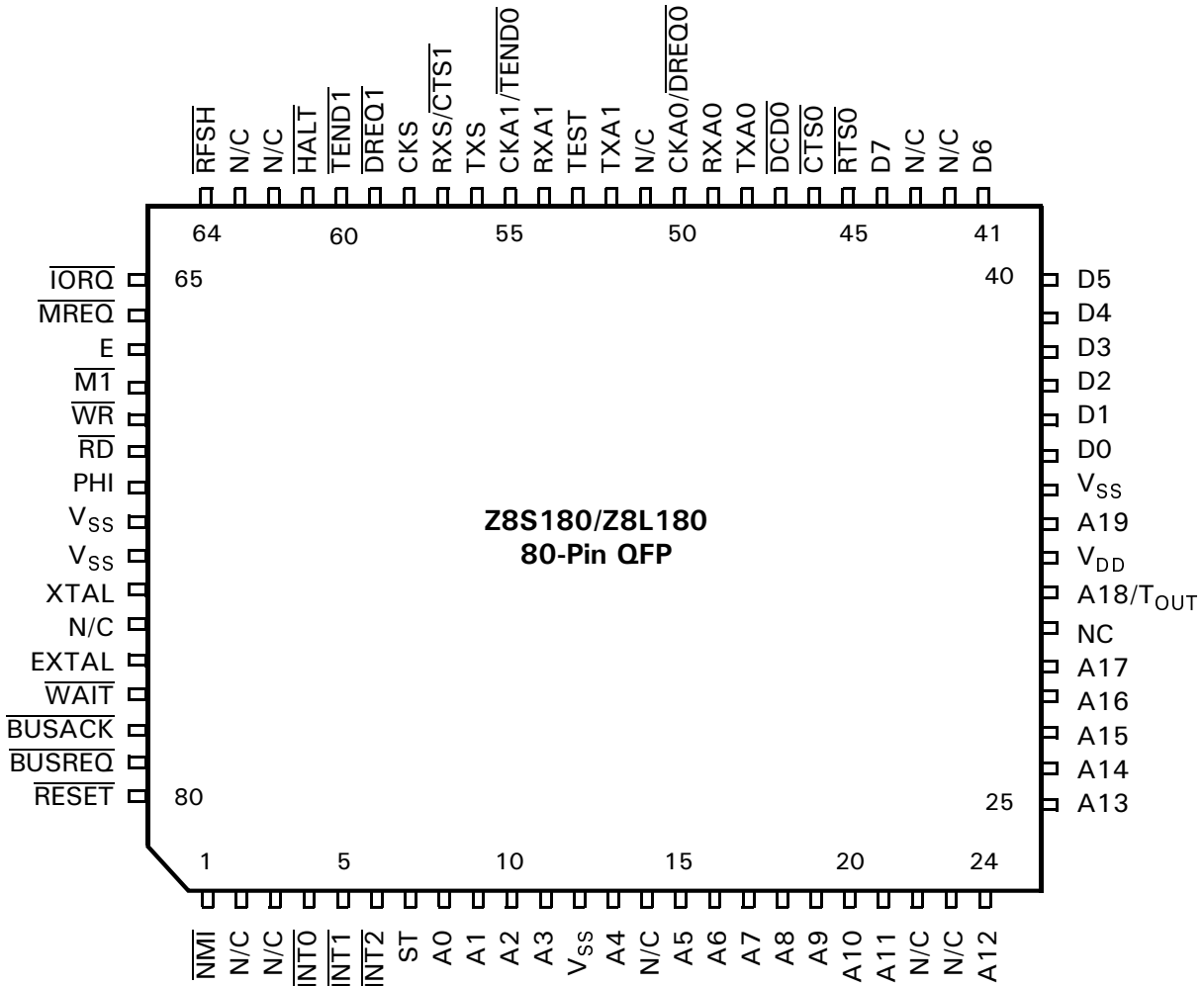


Figure 4. Z8S180/Z8L180 80-Pin QFP Pin Configuration

Table 1. Z8S180/Z8L180 Pin Identification

Pin Number and Package Type			Default Function	Secondary Function	Control
QFP	PLCC	DIP			
1	9	8	$\overline{\text{NMI}}$		
2			NC		
3			NC		
4	10	9	$\overline{\text{INT0}}$		
5	11	10	$\overline{\text{INT1}}$		
6	12	11	$\overline{\text{INT2}}$		
7	13	12	ST		
8	14	13	A0		
9	15	14	A1		
10	16	15	A2		
11	17	16	A3		
12	18		V _{SS}		

PIN IDENTIFICATION (Continued)

Table 1. Z8S180/Z8L180 Pin Identification (Continued)

Pin Number and Package Type			Default Function	Secondary Function	Control
QFP	PLCC	DIP			
13	19	17	A4		
14			NC		
15	20	18	A5		
16	21	19	A6		
17	22	20	A7		
18	23	21	A8		
19	24	22	A9		
20	25	23	A10		
21	26	24	A11		
22			NC		
23			NC		
24	27	25	A12		
25	28	26	A13		
26	29	27	A14		
27	30	28	A15		
28	31	29	A16		
29	32	30	A17		
30			NC		
31	33	31	A18	T _{OUT}	Bit 2 or Bit 3 of TCR
32	34	32	V _{DD}		
33	35		A19		
34	36	33	V _{SS}		
35	37	34	D0		
36	38	35	D1		
37	39	36	D2		
38	40	37	D3		
39	41	38	D4		
40	42	39	D5		
41	43	40	D6		
42			NC		
43			NC		
44	44	41	D7		
45	45	42	$\overline{\text{RTS0}}$		
46	46	43	$\overline{\text{CTS0}}$		
47	47	44	$\overline{\text{DCD0}}$		
48	48	45	TXA0		
49	49	46	RXA0		
50	50	47	CKA0	$\overline{\text{DREQ0}}$	Bit 3 or Bit 5 of DMODE
51			NC		
52	51	48	TXA1		

Table 1. Z8S180/Z8L180 Pin Identification (Continued)

Pin Number and Package Type			Default Function	Secondary Function	Control
QFP	PLCC	DIP			
53	52		TEST		
54	53	49	RXA1		
55	54	50	CKA1	$\overline{\text{TEND0}}$	Bit 4 of CNTLA1
56	55	51	TXS		
57	56	52	RXS	$\overline{\text{CTS1}}$	Bit 2 of STAT1
58	57	53	CKS		
59	58	54	$\overline{\text{DREQ1}}$		
60	59	55	$\overline{\text{TEND1}}$		
61	60	56	$\overline{\text{HALT}}$		
62			NC		
63			NC		
64	61	57	$\overline{\text{RFSH}}$		
65	62	58	$\overline{\text{IORQ}}$		
66	63	59	$\overline{\text{MREQ}}$		
67	64	60	E		
68	65	61	$\overline{\text{M1}}$		
69	66	62	$\overline{\text{WR}}$		
70	67	63	$\overline{\text{RD}}$		
71	68	64	PHI		
72	1	1	V _{SS}		
73	2		V _{SS}		
74	3	2	XTAL		
75			NC		
76	4	3	EXTAL		
77	5	4	$\overline{\text{WAIT}}$		
78	6	5	$\overline{\text{BUSACK}}$		
79	7	6	$\overline{\text{BUSREQ}}$		
80	8	7	$\overline{\text{RESET}}$		

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
1	9	8	$\overline{\text{NMI}}$		IN	IN	IN
2			NC				
3			NC				
4	10	9	$\overline{\text{INT0}}$		IN	IN	IN
5	11	10	$\overline{\text{INT1}}$		IN	IN	IN
6	12	11	$\overline{\text{INT2}}$		IN	IN	IN
7	13	12	ST		High	High	High
8	14	13	A0		3T	3T	High
9	15	14	A1		3T	3T	High
10	16	15	A2		3T	3T	High
11	17	16	A3		3T	3T	High
12	18		V _{SS}		V _{SS}	V _{SS}	V _{SS}
13	19	17	A4		3T	3T	High
14			NC				
15	20	18	A5		3T	3T	High
16	21	19	A6		3T	3T	High
17	22	20	A7		3T	3T	High
18	23	21	A8		3T	3T	High
19	24	22	A9		3T	3T	High
20	25	23	A10		3T	3T	High
21	26	24	A11		3T	3T	High
22			NC				
23			NC				
24	27	25	A12		3T	3T	High
25	28	26	A13		3T	3T	High
26	29	27	A14		3T	3T	High
27	30	28	A15		3T	3T	High
28	31	29	A16		3T	3T	High
29	32	30	A17		3T	3T	High
30			NC				
31	33	31	A18		3T	3T	High
			T _{OUT}		N/A	OUT	OUT
32	34	32	V _{DD}		V _{DD}	V _{DD}	V _{DD}
33	35		A19		3T	3T	High
34	36	33	V _{SS}		V _{SS}	V _{SS}	V _{SS}
35	37	34	D0		3T	3T	3T
36	38	35	D1		3T	3T	3T
37	39	36	D2		3T	3T	3T
38	40	37	D3		3T	3T	3T

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type			Pin Status				
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{\text{RTS0}}$		High	OUT	High
46	46	43	$\overline{\text{CTS0}}$		IN	OUT	IN
47	47	44	$\overline{\text{DCD0}}$		IN	IN	IN
48	48	45	TXA0		High	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0		3T	I/O	I/O
			$\overline{\text{DREQ0}}$		N/A	IN	IN
51			NC				
52	51	48	TXA1		High	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1		3T	I/O	I/O
			$\overline{\text{TEND0}}$		N/A	High	High
56	55	51	TXS		High	OUT	OUT
57	56	52	RXS		IN	IN	IN
			$\overline{\text{CTS1}}$		N/A	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{\text{DREQ1}}$		IN	3T	IN
60	59	55	$\overline{\text{TEND1}}$		High	OUT	High
61	60	56	$\overline{\text{HALT}}$		High	High	Low
62			NC				
63			NC				
64	61	57	$\overline{\text{RFSH}}$		High	OUT	High
65	62	58	$\overline{\text{IORQ}}$		High	3T	High
66	63	59	$\overline{\text{MREQ}}$		High	3T	High
67	64	60	E		Low	OUT	OUT
68	65	61	$\overline{\text{M1}}$		High	High	High
69	66	62	$\overline{\text{WR}}$		High	3T	High
70	67	63	$\overline{\text{RD}}$		High	3T	High
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V _{SS}		GND	GND	GND
73	2		V _{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
76	4	3	EXTAL		IN	IN	IN
77	5	4	$\overline{\text{WAIT}}$		IN	IN	IN
78	6	5	$\overline{\text{BUSACK}}$		High	OUT	OUT
79	7	6	$\overline{\text{BUSREQ}}$		IN	IN	IN
80	8	7	$\overline{\text{RESET}}$		IN	IN	IN

PIN DESCRIPTIONS

A0–A19. Address Bus (Output, 3-state). A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 1 MB) and I/O data bus exchanges (up to 64 KB). The address bus enters a high-impedance state during reset and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT} , selected as address output on reset), and address line A19 is not available in DIP versions of the Z8S180.

BUSACK. Bus Acknowledge (Output, active Low). \overline{BUSACK} indicates that the requesting device, the MPU address and data bus, and some control signals enter their high-impedance state.

BUSREQ. Bus Request (Input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request demands a higher priority than \overline{NMI} and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions, places addresses, data buses, and other control signals into the high-impedance state.

CKA0, CKA1. Asynchronous Clock 0 and 1 (bidirectional). When in output mode, these pins are the transmit and receive clock outputs from the ASCII baud rate generators. When in input mode, these pins serve as the external clock inputs for the ASCII baud rate generators. CKA0 is multiplexed with $\overline{DREQ0}$, and CKA1 is multiplexed with $\overline{TEND0}$.

CKS. Serial Clock (bidirectional). This line is the clock for the CSI/O channel.

CTS0–CTS1. Clear to send 0 and 1 (Inputs, active Low). These lines are modem control signals for the ASCII channels. $\overline{CTS1}$ is multiplexed with RXS.

D0–D7. Data Bus = (bidirectional, 3-state). D0–D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high-impedance state during reset and external bus acknowledge cycles.

DCD0. Data Carrier Detect 0 (Input, active Low); a programmable modem control signal for ASCII channel 0.

DREQ0, DREQ1. DMA Request 0 and 1 (Input, active Low). \overline{DREQ} is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a READ or WRITE operation. These inputs can be programmed to be either level or edge sensed. $\overline{DREQ0}$ is multiplexed with CKA0.

E. Enable Clock (Output). This pin functions as a synchronous, machine-cycle clock output during bus transactions.

EXTAL. External Clock Crystal (Input). Crystal oscillator connections. An external clock can be input to the Z8S180/Z8L180 on this pin when a crystal is not used. This input is Schmitt triggered.

HALT. HALT/SLEEP (Output, active Low). This output is asserted after the CPU executes either the HALT or SLEEP instruction and is waiting for either a nonmaskable or a maskable interrupt before operation can resume. It is also used with the $\overline{M1}$ and ST signals to decode the status of the CPU machine cycle.

INT0. Maskable Interrupt Request 0 (Input, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the \overline{NMI} and \overline{BUSREQ} signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{M1}$ and \overline{IORQ} signals become active.

INT1, INT2. Maskable Interrupt Request 1 and 2 (Inputs, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the \overline{NMI} , \overline{BUSREQ} , and $\overline{INT0}$ signals are inactive. The CPU acknowledges these requests with an interrupt acknowledge cycle. Unlike the acknowledgment for $\overline{INT0}$, neither the $\overline{M1}$ or \overline{IORQ} signals become active during this cycle.

IORQ. I/O Request (Output, active Low, 3-state). \overline{IORQ} indicates that the address bus contains a valid I/O address for an I/O READ or I/O WRITE operation. \overline{IORQ} is also generated, along with $\overline{M1}$, during the acknowledgment of the $\overline{INT0}$ input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the \overline{IOE} signal of the Z64180.

M1. Machine Cycle 1 (Output, active Low). Together with \overline{MREQ} , $\overline{M1}$ indicates that the current cycle is the opcode-fetch cycle of instruction execution. Together with \overline{IORQ} , $\overline{M1}$ indicates that the current cycle is for interrupt acknowledgment. It is also used with the \overline{HALT} and ST signal to decode the status of the CPU machine cycle. This signal is analogous to the \overline{LIR} signal of the Z64180.

MREQ. Memory Request (Output, active Low, 3-state). \overline{MREQ} indicates that the address bus holds a valid address for a memory READ or memory WRITE operation. This signal is analogous to the \overline{ME} signal of Z64180.

NMI. Nonmaskable Interrupt (Input, negative edge triggered). \overline{NMI} demands a higher priority than \overline{INT} and is al-

PIN DESCRIPTIONS (Continued)

ways recognized at the end of an instruction, regardless of the state of the interrupt-enable flip-flops. This signal forces CPU execution to continue at location 0066H.

PHI. System Clock (Output). The output is used as a reference clock for the MPU and the external system. The frequency of this output may be one-half, equal to, or twice the crystal or input clock frequency.

\overline{RD} . Read (Output, active Low, 3-state). \overline{RD} indicates that the CPU wants to read data from either memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

\overline{RFSH} . Refresh (Output, active Low). Together with \overline{MREQ} , \overline{RFSH} indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low-order 8 bits of the address bus (A7–A0) contain the refresh address. *This signal is analogous to the \overline{REF} signal of the Z64180.*

$\overline{RTS0}$. Request to Send 0 (Output, active Low); a programmable MODEM control signal for ASCII channel 0.

$\overline{RXA0}$, $\overline{RXA1}$. Receive Data 0 and 1 (Input). These signals are the receive data for the ASCII channels.

\overline{RXS} . Clocked Serial Receive Data (Input). This line is the receive data for the CSI/O channel. \overline{RXS} is multiplexed with the $\overline{CTS1}$ signal for ASCII channel 1.

\overline{ST} . Status (Output). This signal is used with the $\overline{M1}$ and \overline{HALT} output to decode the status of the CPU machine cycle. See Table 3.

Table 3. Status Summary

ST	\overline{HALT}	$\overline{M1}$	Operation
0	1	0	CPU Operation (1st Opcode Fetch)
1	1	0	CPU Operation (2nd Opcode and 3rd Opcode Fetch)
1	1	1	CPU Operation (MC Except Opcode Fetch)
0	X	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (Including SYSTEM STOP Mode)

Notes:

X = Do not care.

MC = Machine Cycle.

$\overline{TEND0}$, $\overline{TEND1}$. Transfer End 0 and 1 (Outputs, active Low). This output is asserted active during the most recent WRITE cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{TEND0}$ is multiplexed with CKA1.

\overline{TEST} . Test (Output, not in DIP version). This pin is for test and should be left open.

T_{OUT} . Timer Out (Output). T_{OUT} is the output from PRT channel 1. This line is multiplexed with A18 of the address bus.

$\overline{TXA0}$, $\overline{TXA1}$. Transmit Data 0 and 1 (Outputs). These signals are the transmitted data from the ASCII channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

\overline{TXS} . Clocked Serial Transmit Data (Output). This line is the transmitted data from the CSI/O channel.

\overline{WAIT} . Wait (Input, active Low). \overline{WAIT} indicates to the MPU that the addressed memory or I/O devices are not ready for data transfer. This input is sampled on the falling edge of T2 (and subsequent WAIT states). If the input is sampled Low, then the additional WAIT states are inserted until the \overline{WAIT} input is sampled High, at which time execution continues.

\overline{WR} . WRITE (Output, active Low, 3-state). \overline{WR} indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

\overline{XTAL} . Crystal Oscillator Connection (Input). This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see [DC Characteristics](#)).

Several pins are used for different conditions, depending on the circumstance.

Table 4. Multiplexed Pin Descriptions

A18/TOUT	During RESET, this pin is initialized as A18. If either the TOC1 or the TOC0 bit of the Timer Control register (TCR) is set to 1, the T _{OUT} function is selected. If TOC1 and TOC0 are cleared to 0, the A18 function is selected.
CKA0/ $\overline{\text{DREQ0}}$	During RESET, this pin is initialized as CKA0. If either DM1 or SM1 in the DMA Mode register (DMODE) is set to 1, the $\overline{\text{DREQ0}}$ function is selected.
CKA1/ $\overline{\text{TEND0}}$	During RESET, this pin is initialized as CKA1. If the CKA1D bit in ASCI control register ch1 (CNTLA1) is set to 1, the $\overline{\text{TEND0}}$ function is selected. If the CKA1D bit is set to 0, the CKA1 function is selected.
RXS/ $\overline{\text{CTS1}}$	During RESET, this pin is initialized as RXS. If the CTS1E bit in the ASCI status register ch1 (STAT1) is set to 1, the $\overline{\text{CTS1}}$ function is selected. If the CTS1E bit is set to 0, the RXS function is selected.

ARCHITECTURE

The Z180 combines a high-performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller, Interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks: direct memory access (DMA) control (2 channels), asynchronous serial communication interface (ASCI, 2 channels) programmable reload timers (PRT, 2 channels), and a clock serial I/O (CSI/O) channel.

Clock Generator. This logic generates a system clock from an external crystal or clock input. The external clock is divided by 2 or 1 and provides the timing for both internal and external devices.

Bus State Controller. This logic performs all of the status and bus-control activity associated with the CPU and some on-chip peripherals. Also includes wait-state timing, reset cycles, DRAM refresh, and DMA bus exchanges.

Interrupt Controller. This logic monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To maintain compatibility with the Z80 CPU, three different interrupts modes are supported.

Memory Management Unit. The MMU allows the user to map the memory used by the CPU (logically only 64KB) into the 1-MB addressing range supported by the Z8S180/Z8L180. The organization of the MMU object

code maintains compatibility with the Z80 CPU, while offering access to an extended memory space. Accomplished by using an effective common-area/banked-area scheme.

Central Processing Unit. The CPU is microcoded to provide a core that is object-code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiplication. The core is modified to allow many of the instructions to execute in fewer clock cycles.

DMA Controller. The DMA controller provides high-speed transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory to/from I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. DMA transfers can access the full 1-MB address range with a block length up to 64 KB, and can cross over 64K boundaries.

Asynchronous Serial Communication Interface (ASCI).

The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communication format as well as break detection and generation

Programmable Reload Timers (PRT). This logic consists of two separate channels, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.

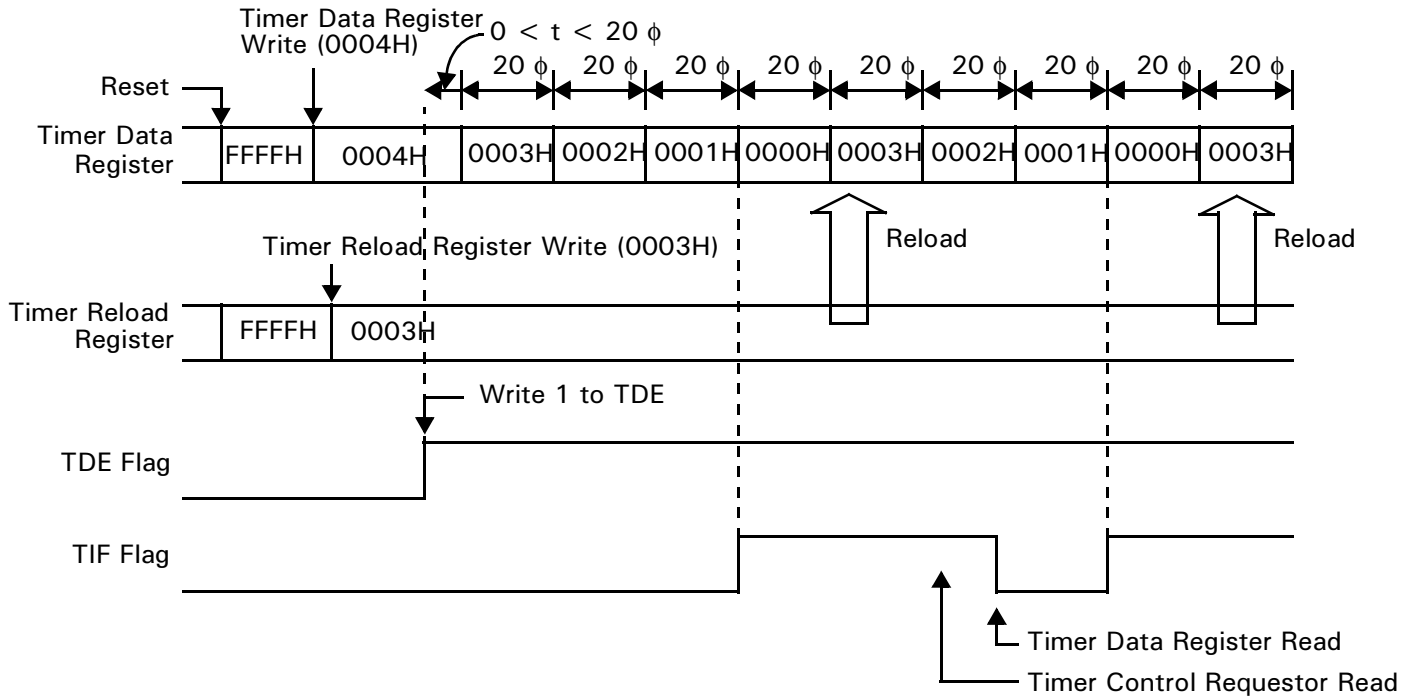


Figure 5. Timer Initialization, Count Down, and Reload Timing

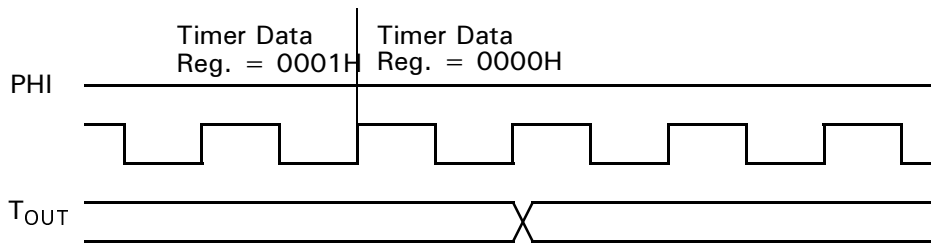


Figure 6. Timer Output Timing

Clocked Serial I/O (CSI/O). The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer. TRDR is used for both CSI/O transmission and reception. Thus, the system design must ensure that the constraints of half-duplex operation are met (Transmit and Receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O does not work.

Note: TRDR is not buffered. Performing a CSI/O transmit while the previous transmission is still in progress causes the data to be immediately updated and corrupts the transmit operation. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.

ARCHITECTURE (Continued)

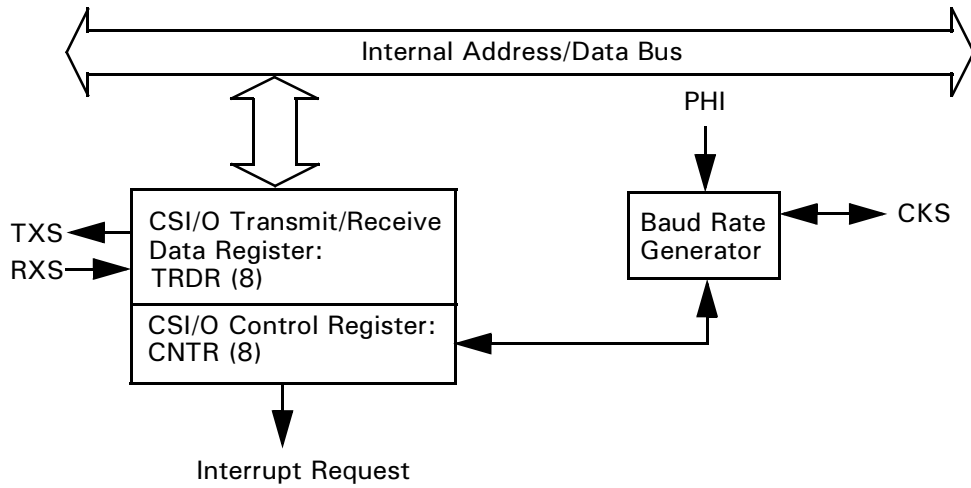


Figure 7. CSI/O Block Diagram

OPERATION MODES

Z80 versus 64180 Compatibility. The Z8S180/Z8L180 is descended from two different “ancestor” processors, ZiLOG’s original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR), illustrated in Figure 8, can be programmed to select between certain Z80 and 64180 differences.

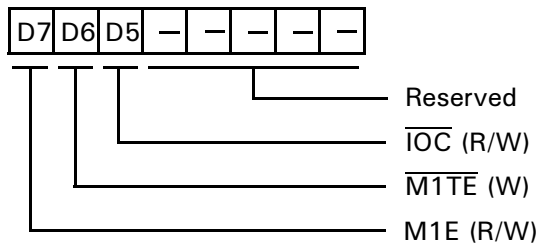


Figure 8. Operating Control Register (OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during RESET.

When $M1E = 1$, the $\overline{M1}$ output is asserted Low during opcode fetch cycles, Interrupt Acknowledge cycles, and the first machine cycle of an NMI acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch a RETI instruction one time. When fetching a RETI from a zero-wait-state memory location, the processor uses three clock bus cycles. These bus cycles are not fully Z80-timing compatible.

When $M1E = 0$, the processor does not drive $\overline{M1}$ Low during the instruction fetch cycles. After fetching a RETI instruction with normal timing, the processor goes back and refetches the instruction using fully Z80-compatible cycles that include driving $\overline{M1}$ Low. This option may be required by some external Z80 peripherals to properly decode the RETI instruction. Figure 9 and Table 5 show the RETI sequence when $M1E$ is 0.

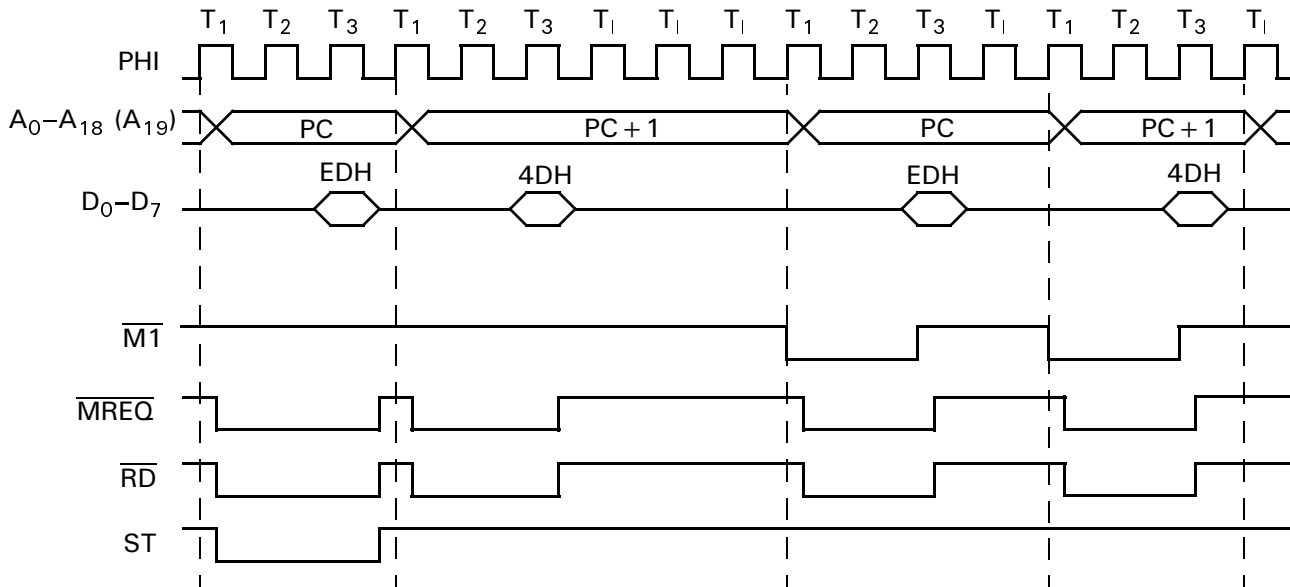


Figure 9. RETI Instruction Sequence with $M1E = 0$

OPERATION MODES (Continued)

Table 5. RETI Control Signal States

Machine Cycle	States	Address	Data	\overline{RD}	\overline{WR}	\overline{MREQ}	\overline{IORQ}	$\overline{M1}$	$\overline{M1}$	\overline{HALT}	ST
								M1E = 1	M1E = 0		
1	T1-T3	1st Opcode	EDH	0	1	0	1	0	1	1	0
2	T1-T3	2nd Opcode	4DH	0	1	0	1	0	1	1	0
	Ti	NA	3-state	1	1	1	1	1	1	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
3	T1-T3	1st Opcode	EDH	0	1	0	1	0	0	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
4	T1-T3	2nd Opcode	4DH	0	1	0	1	0	1	1	1
5	T1-T3	SP	Data	0	1	0	1	1	1	1	1
6	T1-T3	SP + 1	Data	0	1	0	1	1	1	1	1

$\overline{M1TE}$ ($\overline{M1}$ Temporary Enable). This bit controls the temporary assertion of the $\overline{M1}$ signal. It is always read back as a 1 and is set to 1 during RESET.

When M1E is set to 0 to accommodate certain external Z80 peripheral(s), those same device(s) may require a pulse on $\overline{M1}$ after programming certain of their registers to complete the function being programmed.

For example, when a control word is written to the Z80 PIO to enable interrupts, no enable actually takes place until the PIO sees an active $\overline{M1}$ signal. When $\overline{M1TE} = 1$, there is no change in the operation of the $\overline{M1}$ signal, and M1E controls its function. When $\overline{M1TE} = 0$, the $\overline{M1}$ output is asserted during the next opcode fetch cycle regardless of the state programmed into the M1E bit. This condition is only momentary (one time) and it is not necessary to preprogram a 1 to disable the function (see Figure 10).

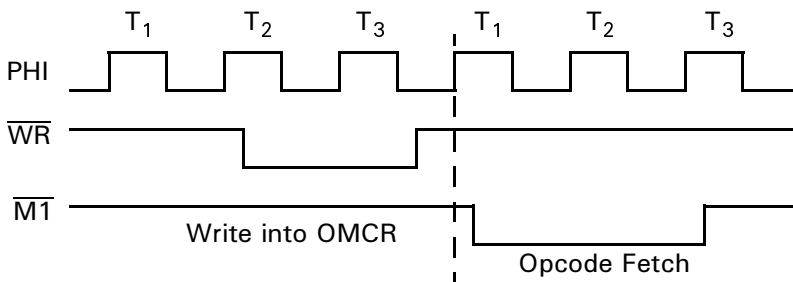
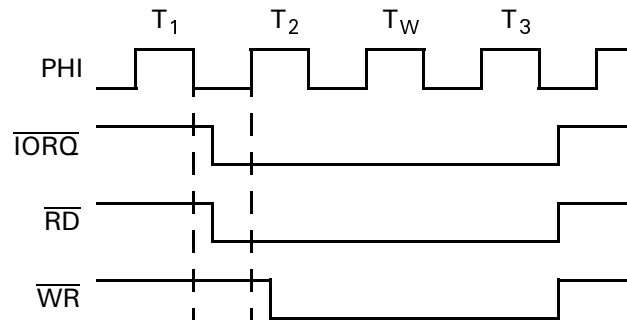


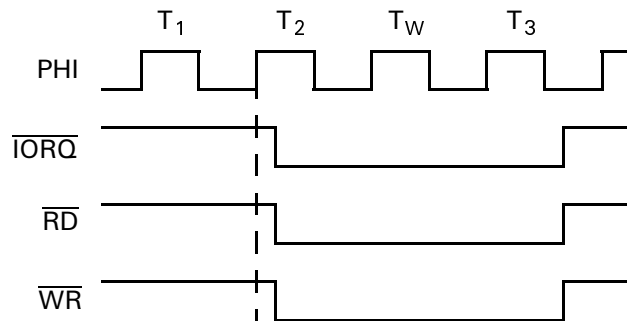
Figure 10. M1 Temporary Enable Timing

IOC (I/O Compatibility). This bit controls the timing of the \overline{IORQ} and \overline{RD} signals. The bit is set to 1 by RESET.

When $\overline{IOC} = 1$, the \overline{IORQ} and \overline{RD} signals function the same as the Z64180 (Figure 11).

Figure 11. I/O Read and Write Cycles with $\overline{\text{IOC}} = 1$

When $\overline{\text{IOC}} = 0$, the timing of the $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ signals match the timing of the Z80. The $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ signals go active as a result of the rising edge of T2. (Figure 12.)

Figure 12. I/O Read and Write Cycles with $\overline{\text{IOC}} = 0$

HALT and Low-Power Operating Modes. The Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOVERY)

Normal Operation. In this state, the Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the $\overline{\text{HALT}}$ pin is High.

HALT Mode. This mode is entered by the HALT instruction. Thereafter, the Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it and drives the $\overline{\text{HALT}}$, $\overline{\text{ST}}$ and $\overline{\text{M1}}$ pins all Low. The oscillator and PHI pin remain Active. Interrupts and bus granting to external Masters, and DRAM refresh can occur, and all on-chip I/O devices continue to operate including the DMA channels.

OPERATION MODES (Continued)

The Z8S180/Z8L180 leaves HALT mode in response to:

- Low on $\overline{\text{RESET}}$
- Interrupt from an enabled on-chip source
- External request on $\overline{\text{NMI}}$
- Enabled external request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, or $\overline{\text{INT2}}$

In case of an interrupt, the return address is the instruction following the HALT instruction. The program can either branch back to the HALT instruction to wait for another interrupt or can examine the new state of the system/application and respond appropriately.

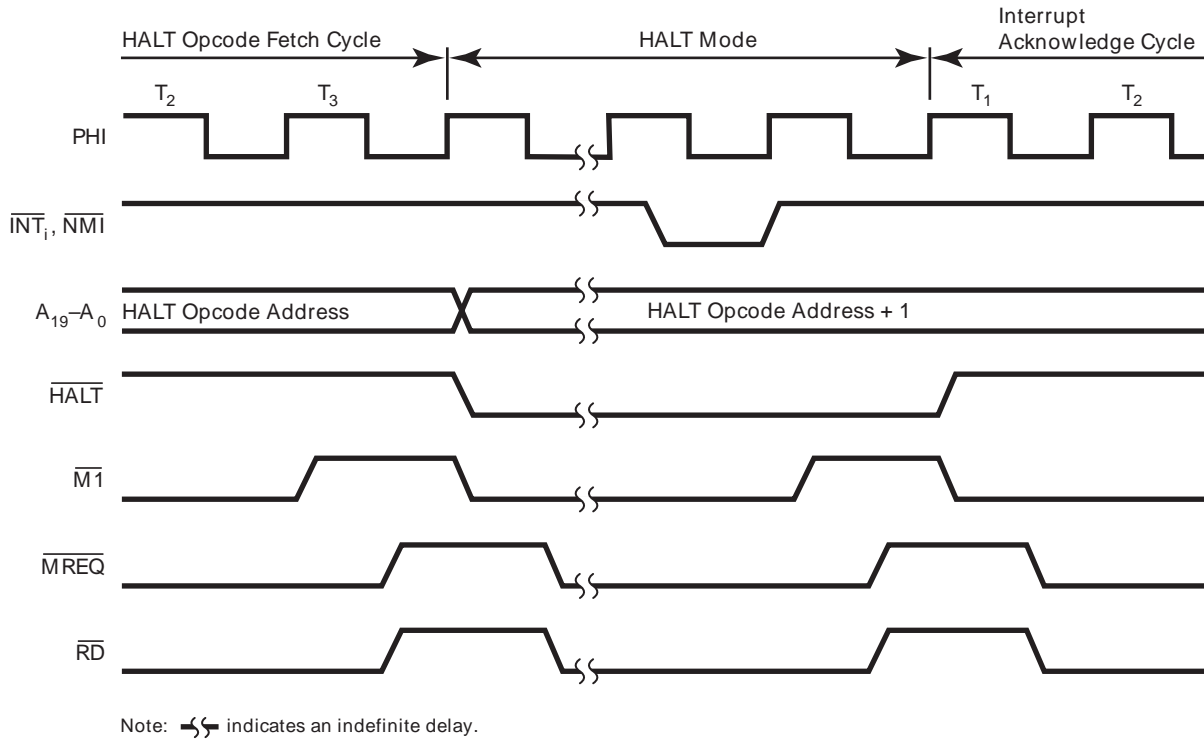


Figure 13. HALT Timing

SLEEP Mode. This mode is entered by keeping the IOSTOP bit (ICR5) and bits 3 and 6 of the CPU Control Register (CCR3, CCR6) all zero and executing the SLP instruction. The oscillator and PHI output continue operating, but are blocked from the CPU core and DMA channels to reduce power consumption. DRAM refresh stops, but interrupts and granting to an external Master can occur. Except when the bus is granted to an external Master, A19-0 and all control signals except $\overline{\text{HALT}}$ are maintained High. $\overline{\text{HALT}}$ is Low. I/O operations continue as before the SLP instruction, except for the DMA channels.

The Z8S180/Z8L180 leaves SLEEP mode in response to a Low on $\overline{\text{RESET}}$, an interrupt request from an on-chip source,

an external request on $\overline{\text{NMI}}$, or an external request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, or $\overline{\text{INT2}}$.

If an interrupt source is individually disabled, it cannot bring the Z8S180/Z8L180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 1 so that interrupts are globally enabled (by an EI instruction), the highest priority active interrupt occurs with the return address being the instruction after the SLP instruction. If an interrupt source is individually enabled, but the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z8S180/Z8L180 leaves SLEEP mode by simply executing the following instruction(s).

This condition provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt-response sequence. Figure 14 depicts the timing for exiting SLEEP mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 1.5 clock ticks to re-start.

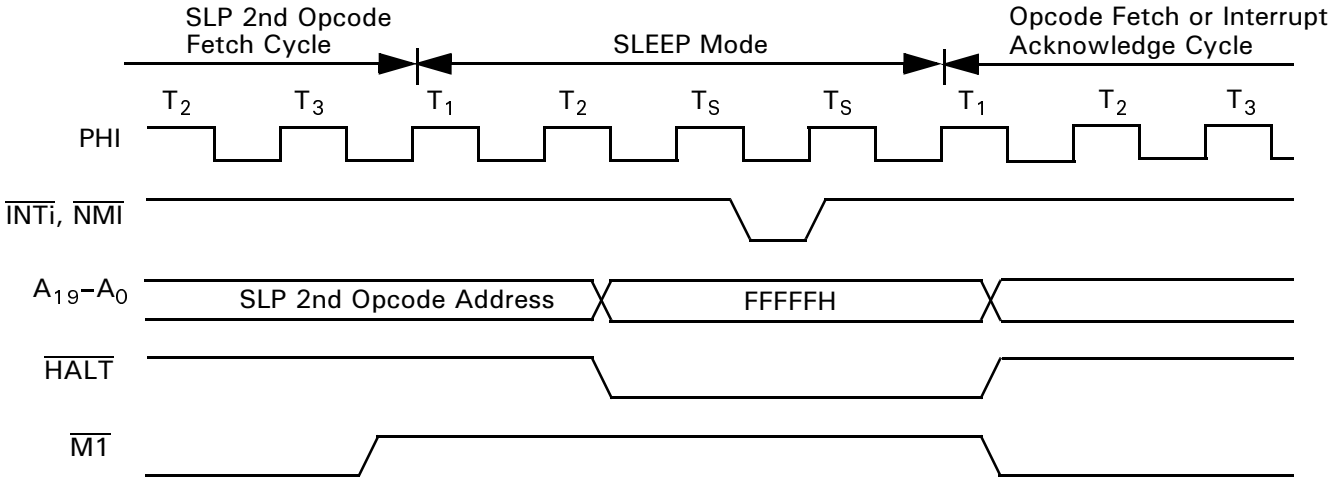


Figure 14. SLEEP Timing

IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is performed by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

IDLE Mode. Software puts the Z8S180/Z8L180 into this mode by performing the following actions:

- Set the IOSTOP bit (ICR5) to 1
- Set CCR6 to 0
- Set CCR3 to 1
- Execute the SLP instruction

The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all

internal devices stop, but external interrupts can occur. Bus granting to external Masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z8S180/Z8L180 leaves IDLE mode in response to a Low on $\overline{\text{RESET}}$, an external interrupt request on $\overline{\text{NMI}}$, or an external interrupt request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z8S180/Z8L180 leaves IDLE mode due to an $\overline{\text{NMI}}$, or due to an enabled external interrupt request when the $\overline{\text{IEF}}$ flag is 1 due to an EI instruction, the device starts by performing the interrupt with the return address of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 indicates the timing for exiting IDLE mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 9.5 clocks to restart.

OPERATION MODES (Continued)

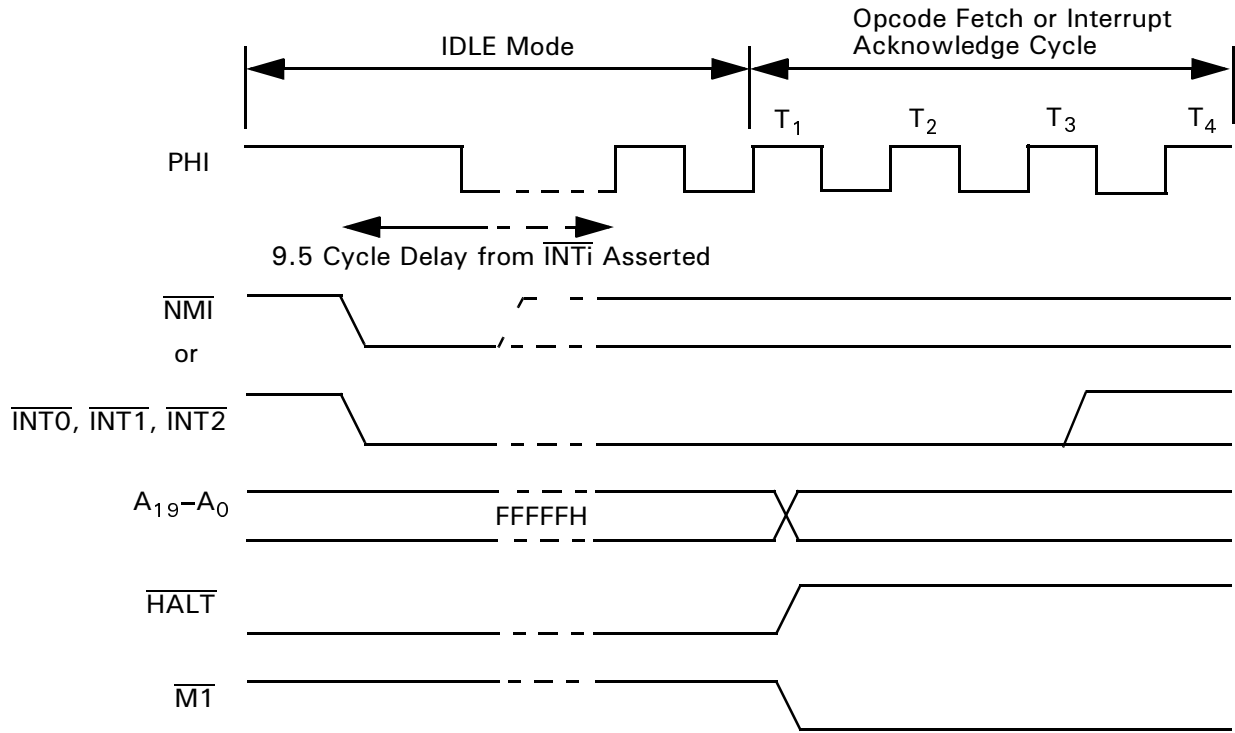


Figure 15. Z8S180/Z8L180 IDLE Mode Exit Due To External Interrupt

While the Z8S180/Z8L180 is in IDLE mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 16 depicts the timing for this sequence.

After the external Master negates the Bus Request, the Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.

Note: A response to a bus request takes 8 clock cycles longer than in normal operation.

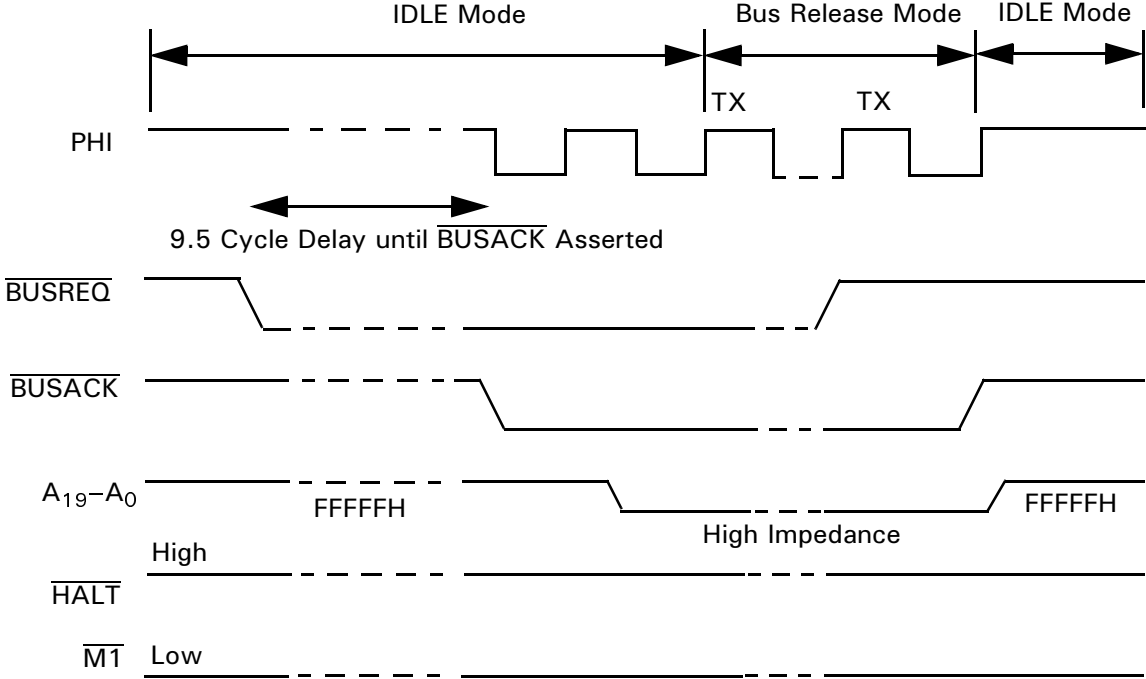


Figure 16. Bus Granting to External Master in IDLE Mode

STANDBY Mode (With or Without QUICK RECOVERY).

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INT0-2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding $\overline{\text{HALT}}$ Low and $\overline{\text{M1}}$ High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives $\overline{\text{RESET}}$ Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold $\overline{\text{RESET}}$ Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits 2^{17} (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{\text{NMI}}$ Low or an enabled $\overline{\text{INT0}}\text{--}\overline{\text{INT2}}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to

a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{\text{INT0}}$, or $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes either 64 or 2^{17} (131,072) clocks to restart, depending on the CCR3 bit.

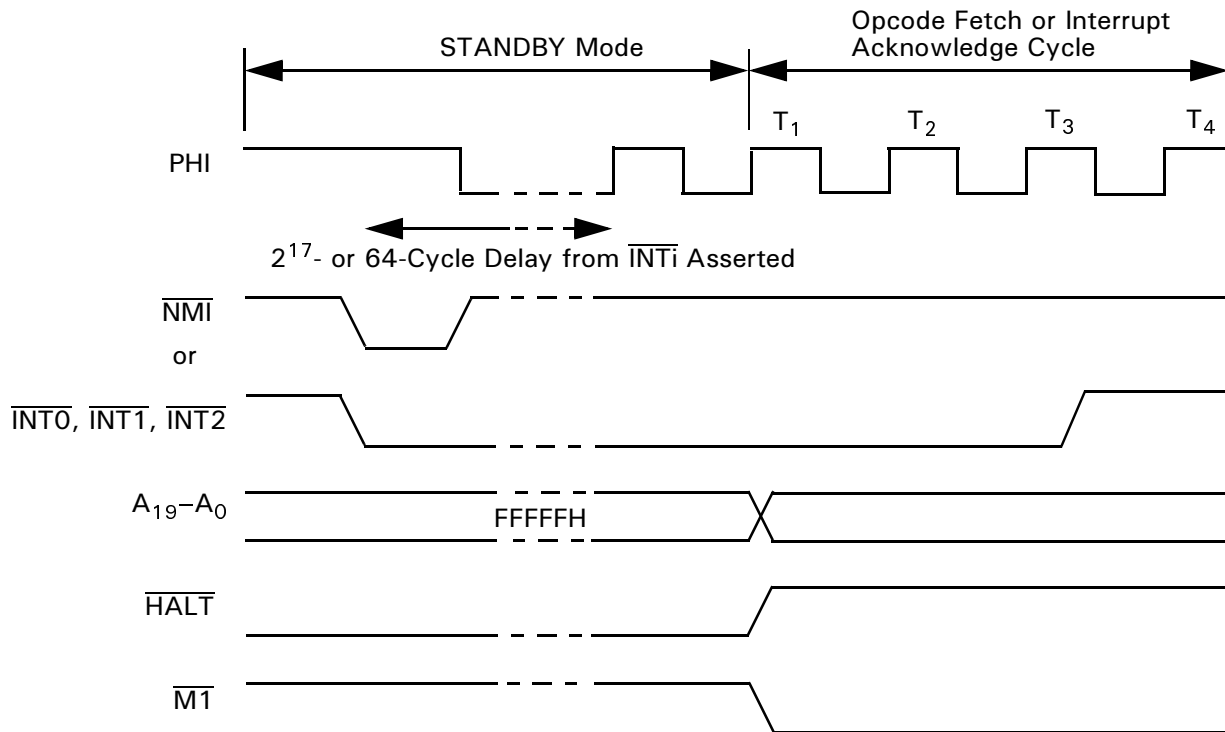


Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or 2^{17} (131,072) clock cycles to grant the bus de-

pending on the CCR3 bit. The latter (not the QUICK RECOVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

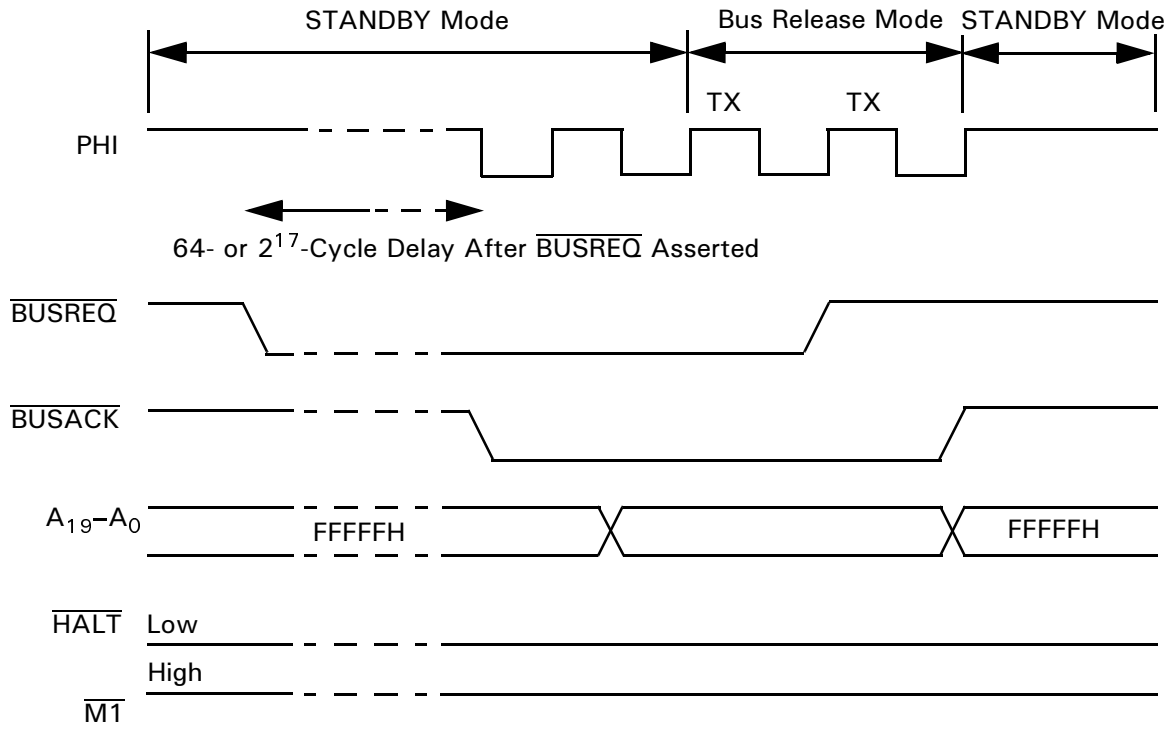


Figure 18. Bus Granting to External Master During STANDBY Mode