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Z80382/Z8L382

**Z80382 Data
Communications
Processor**

Preliminary Product Specification

PS006702-1201



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Manual Conventions

The following conventions have been adopted to provide clarity and ease of use:

- Courier Regular 10-point highlights the following items
 - Bit
 - Software code
 - File names and paths
 - Hexadecimal value





Table of Contents

Z80382, Z8L382 High-Performance Data Communications Processors . . .	1
Features	1
General Description	2
Z80382 Pin Description	6
Absolute Maximum Ratings	7
Standard Test Conditions	7
DC Characteristics	8
AC Characteristics	14
Pin Functions	37
Functional Description	47
Central Processing Unit	47
Modes of Operation	48
CPU Address Spaces	49
Data Types	52
Addressing Modes	52
Instruction Set	54
Host Interface	54
16550 MIMIC	54
Host DMA Mailbox	60
Plug-and-Play Interface	61
PCMCIA Interface	64
DMA Channels	67
DMA Channel/Device Interface	68
DMA Operation	68
Per-Channel Registers	72
Centralized DMA Registers	73
Serial Communication Channels	73
Asynchronous Serial Communications Interface (ASCI)	73
HDLC Serial Channels	77
GCI/SCIT Interface	82
Clocked Serial I/O (CSIO)	88



Counters, Timers and Other Miscellaneous Logic	89
Programmable Reload Timer	89
Watch-Dog Timer	91
Parallel Ports	92
I/O Chip Selects	93
Interrupt Logic	95
Z380-Compatible Peripheral Functions	98
Device Configuration	101
Programmable Low-Noise Drivers	102
Z382 I/O Register Maps	102
Package Information	111
Ordering Information	113
Device Errata	114
Index	115



List of Figures

Figure 1.	Z80382 Block Diagram	5
Figure 2.	Z80382 144-Pin QFP and VQFP Pin Description	6
Figure 3.	Test Load Diagram	8
Figure 4.	380C Processor Timing Diagram	16
Figure 5.	Host - PCMCIA Attribute Memory Read Timing Diagram	18
Figure 6.	Host - PCMCIA Attribute Memory Write Timing Diagram	19
Figure 7.	Host - PCMCIA I/O Read Timing Diagram	21
Figure 8.	Host - PCMCIA I/O Write Timing Diagram	23
Figure 9.	Timer Output Timing Diagram	24
Figure 10.	CSIO Receive/Transmit Timing Diagram	25
Figure 11.	ASCI Transmitter Timing Diagram	26
Figure 12.	ASCI Receiver Timing Diagram	27
Figure 13.	Baud Rate Generator Timing Diagram	28
Figure 14.	CTSA and DCDA Timing Diagram	29
Figure 15.	RTSA Timing Diagram	29
Figure 16.	General-Purpose I/O Port Timing Diagram	30
Figure 17.	HDLC Receive Timing Diagram (Full Time HDLC, RxC Input)	32
Figure 18.	HDLC Receive Timing (Full Time HDLC, RxC Output)	32
Figure 19.	HDLC Transmit Timing Diagram (Full Time HDLC)	33
Figure 20.	HDLC Timing Diagram - Non-GCI TDM Mode (for Start = 3, Length = 2, Negative Edge RxD Sampling)	35
Figure 21.	GCI/SCIT Slave and Master Timing Diagram	37
Figure 22.	380C Processor Core Register Set	50
Figure 23.	16550 MIMIC Block Diagram	56
Figure 24.	16550 MIMIC Receiver FIFO Block Diagram	57
Figure 25.	16550 MIMIC Transmitter FIFO Block Diagram	58
Figure 26.	Plug-and-Play Interface Block Diagram	62
Figure 27.	PCMCIA Interface Block Diagram	65
Figure 28.	PCMCIA Attribute Memory Organization	66
Figure 29.	General Format of a DMA List Entry	68
Figure 30.	Asynchronous Serial Communications Interface (ASCI) Block Diagram	74
Figure 31.	HDLC Channel Block Diagram (One of Three Channels Illustrated)	78
Figure 32.	GCI/SCIT Frame Structure	83



Figure 33. Monitor Handshake Timing Diagram	86
Figure 34. CSIO Block Diagram	88
Figure 35. Programmable Reload Timer Block Diagram	90
Figure 36. PRT Operation Timing Diagram	91
Figure 37. Watch-Dog Timer Block Diagram	92
Figure 38. 144-Lead Plastic QFP Package Diagram	111
Figure 39. 144-Lead Plastic Low Profile VQFP Package Diagram	112



List of Tables

Table 1.	Pin Numbers and Input/Output Classifications	8
Table 2.	Output Class Characteristics	11
Table 3.	Input Class Characteristics	12
Table 4.	DC Electrical Characteristics	13
Table 5.	AC Characteristics	14
Table 6.	Host-PCMCIA Attribute Memory Read Timing	17
Table 7.	Host-PCMCIA Attribute Memory Write Timing	19
Table 8.	Host-PCMCIA I/O Read	20
Table 9.	Host-PCMCIA I/O Write Timing	22
Table 10.	Timer Output Timing	24
Table 11.	CSIO Receive/Transmit Timing	25
Table 12.	ASCI Transmitter Timing	26
Table 13.	ASCI Receiver Timing	27
Table 14.	ASCI/CSIO Timing	28
Table 15.	General-Purpose I/O Port Timing	30
Table 16.	HDLC Receive Timing	31
Table 17.	HDLC Transmit Timing	33
Table 18.	HDLC Timing - Non-GCI TDM Mode	34
Table 19.	GCI/SCIT Timing - Slave Characteristics	35
Table 20.	GCI/SCIT Timing - Master Characteristics	36
Table 21.	Multiprocessor Unit (MPU) Signals	38
Table 22.	UART, Timer and CSIO Signals	42
Table 23.	ISA Bus Signals	43
Table 24.	HDLC Serial Channel and GCI/SCIT Signals	44
Table 25.	Parallel Ports	44
Table 26.	PCMCIA Interface Signals	45
Table 27.	Other Signals	47
Table 28.	MIMIC Programming Registers	58
Table 29.	MIMIC-Host Registers	60
Table 30.	DMA Channel/Device Interface	68
Table 31.	Type/Status Definitions	69
Table 32.	Per-Channel Registers	72
Table 33.	Pin Use Differences in TDM/Full Time Operation	77
Table 34.	HDLC Channel/GCI/SCIT Interface	79



Table 35.	GCI Subchannel Start and Length Values	79
Table 36.	Interrupt Source Priorities	96
Table 37.	Interrupt Sources and Assigned Vectors	97
Table 38.	Z80380-Compatible Registers	102
Table 39.	Z80382 ASCI, PRT, CSIO, WDT Registers	103
Table 40.	Port and New Z80382 Registers	104
Table 41.	DMA Registers	105
Table 42.	HDLC Registers	106
Table 43.	GCI/SCIT Registers	107
Table 44.	Z80382 MIMIC Registers	108
Table 45.	PCNMCI A Memory and Registers	109
Table 46.	Plug-and-Play ISA Registers	109



Z80382, Z8L382 Data Communications Processor

Features

- Embedded Z380™ Microprocessor
 - Maintains Object Code Compatibility with Z80® and Z180™ Microprocessors
 - Enhanced Instruction Set for 16-Bit Operation
 - 16 MB Linear Addressing
 - Two Clock Cycle Instruction Execution Minimum
 - Four On-Chip Register Banks
 - BC/DE/HL/IX/IY Augmented to 32 Bits
 - Clock Divide-by-Two and Multiply-by-Two Options
 - Fully Static CMOS Design with Low-Power STANDBY Mode
 - 16-Bit Internal Bus
 - Dynamic Bus Sizing (8/16-Bit Inter-Operability)
- 16550 MIMIC with I/O Mailbox, DMA Mailbox, and 16 mA Bus Drive
- Three HDLC Synchronous Serial Channels
 - Serial Data Rate of up to 10 Mbps
- GCI/SCIT Bus Interface
- Eight Advanced DMA Channels with 24-Bit Addressing
- Plug-and-Play ISA Interface
- PCMCIA Interface
- Two Enhanced ASCIs (UARTs) with 16-Bit Baud Rate Generators (BRG)
- Clocked Serial I/O Channel (CSIO) for Use with Serial Memory
- Two 16-Bit Timers with Flexible Prescalers
- Three Memory Chip Selects with Wait-State Generators
- Watch-Dog Timer (WDT)



- Up to 32 General-Purpose I/O Pins
- DC to 20 MHz Operating Frequency @ 5.0V
- DC to 10 MHz Operating Frequency @ 3.3V
- 144-Pin QFP and VQFP Style Packages

General Description

The Z80382 (Z382) is designed to address high-end data communication applications such as digital modems (ISDN, GSM, Mobitex & Modacom), xDSL and analog modems (V.34 and beyond). The Z382 provides a performance upgrade to existing Z80- and Z18x-based designs by utilizing the increased bandwidth of the 380C processor. The Z8L382 is a low voltage version of the device.

- **Notes:** In this document the notation 380C denotes the Z380-compatible CPU core which is embedded in the Z382.

An overline ($\bar{\quad}$) above a signal name indicates that the signal is asserted in the Low state and negated in the High state.

The 380C microprocessor is a high-performance processor with fast and efficient throughput and increased memory addressing capabilities. The 380C offers a continuing growth path for present Z80- or Z18x-based designs, while maintaining Z80 and Z180 object code compatibility. Its enhancements include added instructions, expanded 16 MB address space and flexible bus interface timing.

In the 380C, the basic addressing modes of the Z80 microprocessor have been augmented to include Stack Pointer Relative loads and stores, 16-bit and 24-bit indexed offsets, and more flexible Indirect Register addressing. Internally, all of the addressing modes allow up to 32-bit linear addressing; however, the Z382 has 24 address pins, therefore it can address a maximum of 16 MB of memory.

Other additions to the instruction set include a full complement of 16-bit arithmetic and logical operations, 16-bit I/O operations, multiply and divide, and a complete set of register-to-register loads and exchanges.

The 380C register file includes alternate versions of the IX and IY registers. There are four banks of registers in the 380C, along with instructions for switching among them. All of the 16-bit register pairs and index registers in the basic Z80 microprocessor register file are expanded to 32 bits.

The Z382 includes dynamic bus sizing to allow any mix of 8- and 16-bit memory, and I/O devices in a system. One application for this capability would be to copy code from a low-cost, slow 8-bit ROM to 16-bit RAM, from which it can be exe-



cutted at much higher speeds. Memory bus sizes can be configured internally by software to eliminate the need for external logic to drive MSIZE.

Some features that have traditionally been handled by external peripherals have been incorporated in the Z382. These on-chip peripherals reduce system chip count and interconnections on the external bus. These peripherals, illustrated in the Z382 Block Diagram in Figure 1, are summarized below.

HDLC Synchronous Channels. Three HDLC channels operate at serial data rates of up to 10 Mbps and feature 8-byte receive and transmit FIFOs. These can be used for modems, general data communications, and ISDN. The ISDN can be handled separately or through the GCI/SCIT bus interface. HDLC Channels always transfer data through the DMA channels. A transparent mode is selectable. Two of the HDLC cells can be pin multiplexed with the ASCIs (UARTs) to provide dynamically switchable (async-sync) DTE interfaces.

DMA Channels. The eight DMA channels provide 24-bit memory addressing and can transfer memory block sizes of up to 64 KB (16-bits) word. These DMA channels can be dynamically assigned to serve the HDLC ports, MIMIC COM port, Host DMA Mailbox, or ASCIs in any mixture. Linked list operation allows all HDLC transmitters and receivers to operate at or above T1/E1 rates simultaneously without loading the bus bandwidth.

16550 MIMIC. Provides connection to a PC ISA bus and emulation of the 16550 UART register set. Improvements include 16 mA output drivers and internal COM port address decoding to reduce external PC interface components.

ASCI. Two flexible asynchronous serial channels with baud rate generators, modem control and status.

CSIO. A clocked serial I/O channel which can be used for serial memory interface.

Timers. Two 16-bit counter/timers with flexible prescalers for wide-range timing applications.

GCI/SCIT Bus Interface. A common interface to ISDN interface devices. Internal signals from this module can be connected to the HDLC channels to provide two B-channels and one D-channel for ISDN.

Plug-and-Play ISA Interface. Provides auto-configuration in ISA (AT bus) applications.

PCMCIA Interface. Provides connectivity to a PCMCIA bus.

32-Bit General-Purpose I/O. For non-PC add-in applications, four 8-bit ports are provided for general-purpose I/O. In ISA or PCMCIA applications, the pins from two of the ports are reallocated to host bus signals and are not available. Pins from the other two ports are selectively multiplexed with on-chip peripheral functions (ASCIs, CSIO, PRT). These pins are individually programmable for input/output mode.



I/O Chip Selects. Two I/O chip selects are provided to support I/O access of external peripherals. Each has a programmable base address and provides I/O decode sizes ranging from 8 to 512 bytes.

ROM/RAM Chip Selects with Wait-State Generators. Chip select outputs are provided to decode memory addresses and provide memory chip enables. Each chip select has its own Wait State Generator to allow use of memories with different speeds.

Watch-Dog Timer. A Watch-Dog Timer (WDT) with a wide range of time-constants prevents code runaway and possible resulting system damage. The RESET input can be forced as an output upon the terminal count of the WDT. This allows external peripherals to be reset along with the Z382

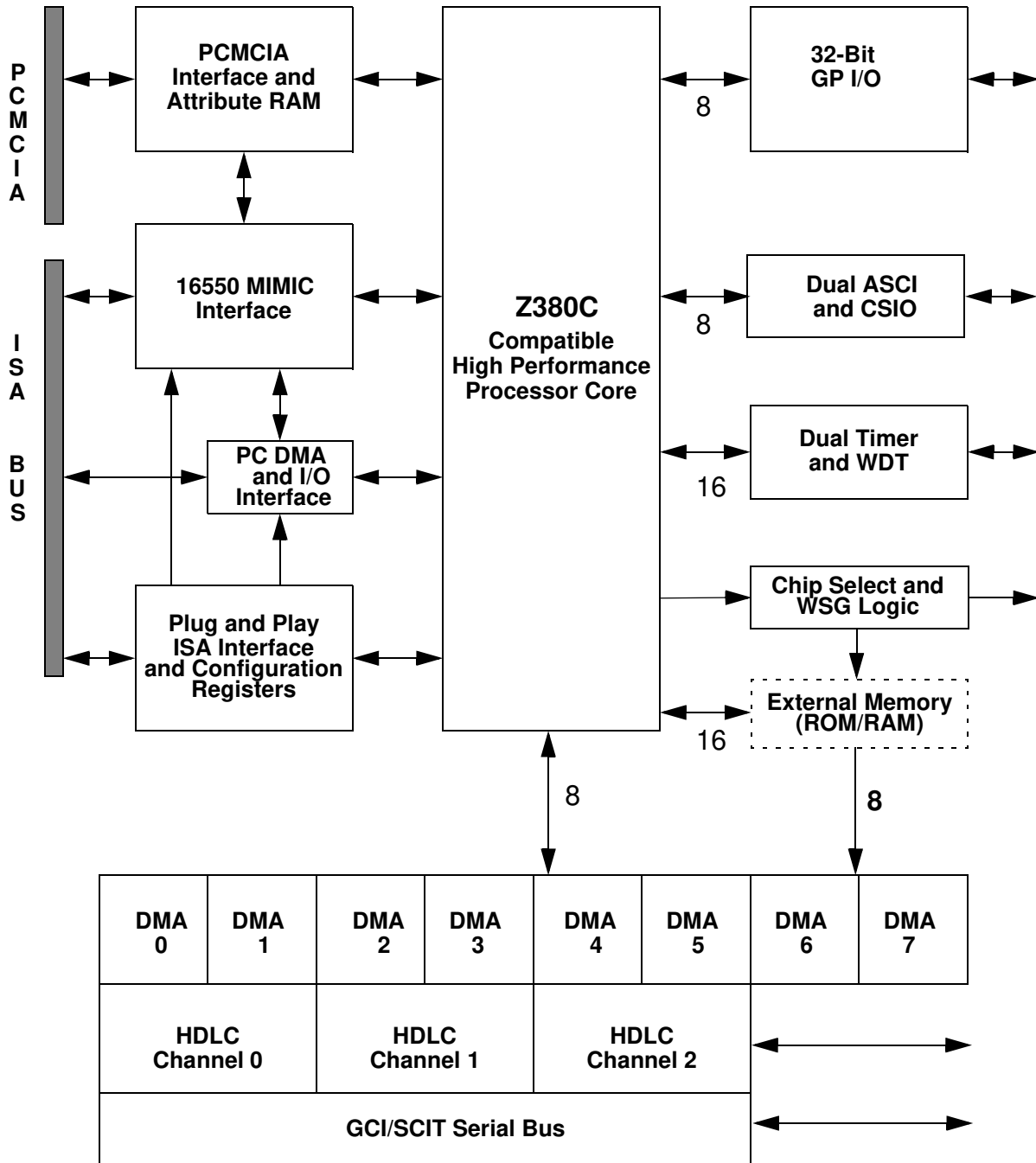


Figure 1. Z80382 Block Diagram



Z80382 Pin Description

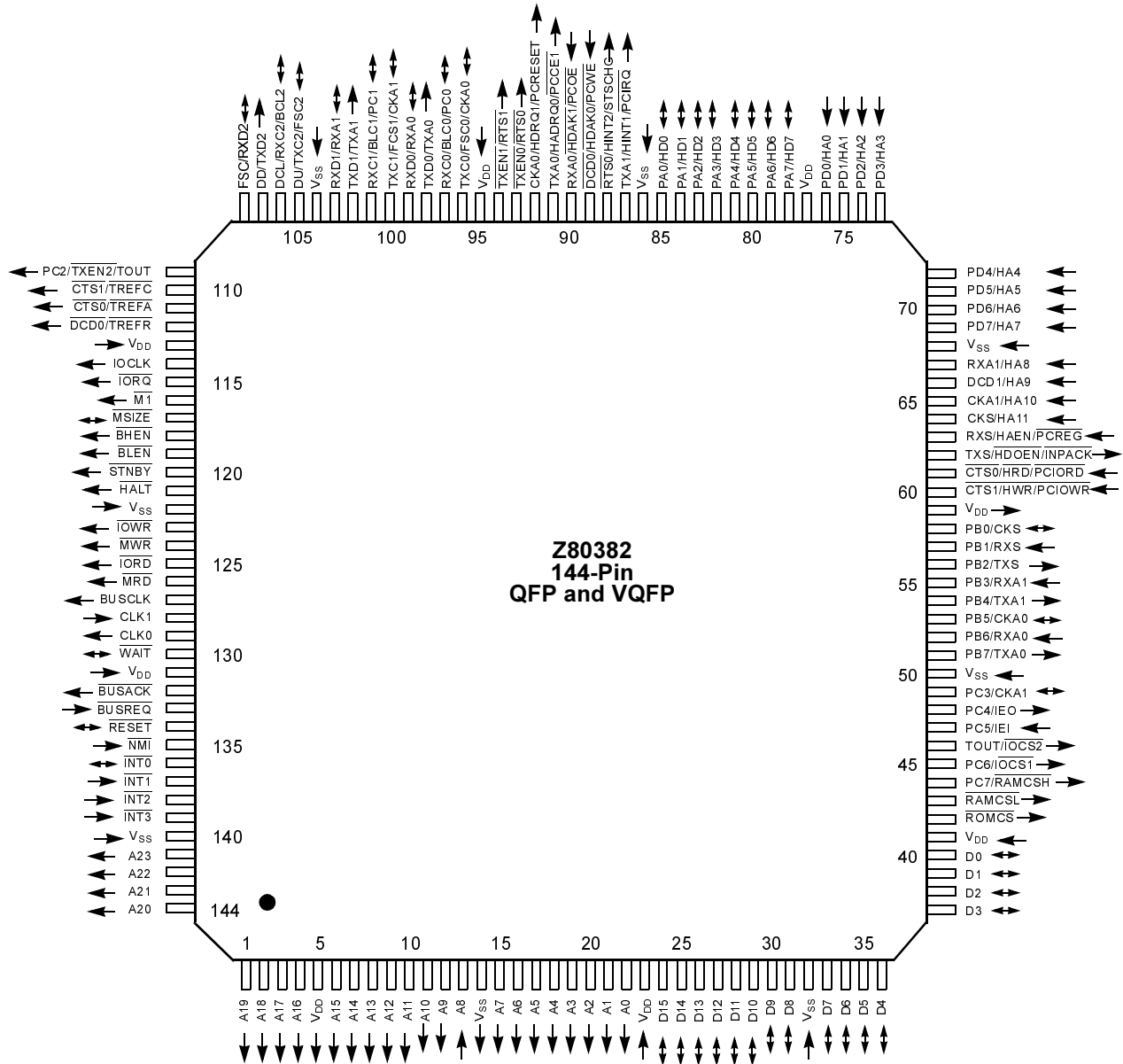


Figure 2. Z80382 144-Pin QFP and VQFP Pin Description



Absolute Maximum Ratings

Symbol	Description	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +7.0	V
V_{IN}	Input Voltage	-0.3 to $V_{DD}+0.3$	V
T_{OPR}	Operating Temp	0 to +70	°C
T_{STG}	Storage Temp	-55 to +150	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The DC Characteristics which follow apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Figure 3, Test Load Diagram).

- Operating temperature range:
 - Standard: 0°C to 70°C
- Voltage Supply Range:
 - $+4.5V \leq V_{DD} \leq +5.5V$ (Z80382 versions)
 - $+3.0V \leq V_{DD} \leq +3.6V$ (Z8L382 versions)

All AC parameters assume a load capacitance of 50 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for PHI is 125 pF.

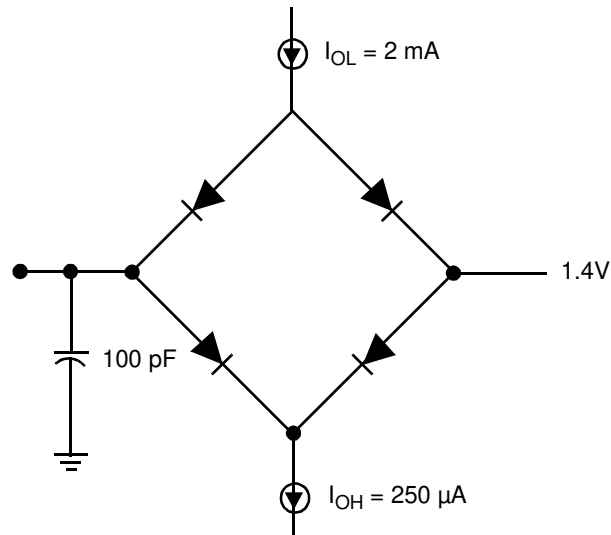


Figure 3. Test Load Diagram

DC Characteristics

Pin Numbers and Input/Output Classifications

Table 1. Pin Numbers and Input/Output Classifications

Pin	Input Class ¹	Output Class ¹	Pin Number(s)
$\overline{\text{BHEN}}$		O	118
$\overline{\text{BLEN}}$		O	119
$\overline{\text{BUSACK}}$		O	132
$\overline{\text{BUSREQ}}$	I		133
$\overline{\text{CTS0/HRD/PCIORD}}$	I		61
$\overline{\text{CTS0/TREFA}}$	I	O	111
$\overline{\text{CTS1/HWR/PCIOWR}}$	I		60
$\overline{\text{CTS1/TREFC}}$	I	O	110
$\overline{\text{DCD0/HDAK0/PCWE}}$	I		89
$\overline{\text{DCD0/TREFR}}$	I	O	112
$\overline{\text{DCD1/HA9}}$	I		66
$\overline{\text{HALT}}$		O	121



Table 1. Pin Numbers and Input/Output Classifications (Continued)

Pin	Input Class ¹	Output Class ¹	Pin Number(s)
$\overline{\text{INT0-3}}$	R		136 - 139
$\overline{\text{IORD}}$	I	3	125
$\overline{\text{IORQ}}$	I	3	115
$\overline{\text{IOWR}}$	I	3	123
$\overline{\text{M1}}$	I	3	116
$\overline{\text{MRD}}$	I	3	126
$\overline{\text{MSIZE}}$	I	D	117
$\overline{\text{MWR}}$	I	3	124
$\overline{\text{NMI}}$	R		135
$\overline{\text{RAMCSL}}$		O	43
$\overline{\text{RESET}}$	R	D	134
$\overline{\text{ROMCS}}$	O		42
$\overline{\text{RTS0/HINT2/STSCHG}}$		H	88
$\overline{\text{STNBY}}$		O	120
$\overline{\text{TXEN1-0/RTS1-0}}$		O	94 -93
$\overline{\text{WAIT}}$	I	D	130
A23-0	I	3	141 - 144, 1 - 4, 6 - 13, 15 - 22
BUSCLK		H	127
CKA0/HDRQ1/PCRESET	I	H	92
CKA1/HA10	I	3	65
CKS/HA11	I	3	64
CLKI	R		128
CLKO		O	129
D15-0	I	3	24 - 31, 33 - 40
DCL/RXC2/BCL2	I		106
DD/TXD2	I	D (DD) O (TXD2)	107
DU/TXC2/FSC2	I	D (DU) O (TXC2, FSC2)	105
FSC/RXD2	I		108



Table 1. Pin Numbers and Input/Output Classifications (Continued)

Pin	Input Class ¹	Output Class ¹	Pin Number(s)
IOCLK	I	O	114
PA7-0/HD7-0	I	H	78 -85
PB0/CKS	I	3	58
PB1/RXS	i	3	57
PB2/TXS	I	3	56
PB3/RXA1	I	3	55
PB4/TXA1	I	3	54
PB5/CKA0	I	3	53
PB6/RXA0	I	3	52
PB7/TXA0	I	3	51
PC2/TXEN2/TOUT	I	3	109
PC3/CKA1	I	3	49
PC4/IEO	I	3	48
PC5/IEI	I	3	47
PC6/IOCS1	I	3	45
PC7/RAMCSH	I	3	44
PD7-0/HA7-0	I	3	69 - 76
RXA0/HDAK1/PCOE	I	D	90
RXA1/HA8	I	3	67
RXC1-0/BCL1-0/PC1-0	I	3	101, 97
RXD1-0/RXA1-0	I	O	103, 99
RXS/HAEN/PCREG	I	D	63
TOUT/IOCS2		3	46
TXA0/HDRQ0/PCCE1	I	H	91
TXA1/HINT1/PCIRQ		H	87
TXC1-0/FSC1-0/CKA1-0	I	3	100, 96
TXD1-0/TXA1-0		O	102, 98
TXS/HDOEN/INPACK		O	62



Table 1. Pin Numbers and Input/Output Classifications (Continued)

Pin	Input Class ¹	Output Class ¹	Pin Number(s)
V _{DD}			5, 23, 41, 59, 77, 95, 113, 131
V _{SS}			14, 32, 50, 68, 86, 104, 122, 140

Note: 1. Characteristics of each pin are listed in terms of the classifications in the DC Characteristics Table 2 and Table 3 which follow.

Specifications apply over Standard Operating Conditions unless otherwise noted.

Table 2. Output Class Characteristics

Output Class ⁽¹⁾	Type	V _{OL} Max.	V _{OH} Min.	C _{OUT} Max. ⁽²⁾
O	Totem Pole	0.4V @ I _{OL} = 2.0 mA	V _{DD} - 1.2V @ I _{OH} = 200 μA	15 pF
		Slew Rate = 0.33 V/ns min @ C _{LOAD} = 50 pF		
3	3-State	0.4V @ I _{OL} = 2.0 ma	V _{DD} - 1.2V @ I _{OH} = 200 μA	
		Slew Rate = 0.33 V/ns min @ C _{LOAD} = 50 pF		
H	High Drive 3-State	0.4V max @ I _{OL} = 16 mA, V _{DD} = 5V	2.4V min @ I _{OH} = 5mA, V _{DD} = 5V	15 pF
		Slew Rate = 0.33 V/ns min @ C _{LOAD} = 50 pF		
D	Open-Drain	0.4V max @ I _{OL} = 16 mA	--	15 pF

Notes:

1. The Pin Numbers and Input/Output Classifications described in Table 1 identifies the specific output pins in each class.
2. Applies to Output only or I/O.



Table 3. Input Class Characteristics

Input Class ⁽¹⁾	V _{IL} Max. (Z80382)	V _{IL} Max. (Z8L382)	V _{IH} Min. (Z80382)	V _{IH} Min. (Z8L382)	Minimum Hysteresis
I	0.8V	0.6V	2.0V	2.0V	0.4V
<p>$I_I = \pm 10 \mu\text{A}$ max, $V_I = 0$ to 5V (includes leakage if I/O) $C_{IN} = 5 \text{ pF}$ max (if input only, see output type if I/O)</p> <p>Note: Inputs of this type include a weak-latch circuit, except that a register bit can disable those for pins PB7-0.</p>					
R	0.4V	0.4V	$V_{DD} - 0.6\text{V}$	$V_{DD} - 0.3\text{V}$	0.4V
<p>$I_I = \pm 10 \mu\text{A}$ max, $V_I = 0$ to 5V $C_{IN} = 5 \text{ pF}$ max</p> <p>Note: Inputs of this type except CLKI include a weak-latch circuit.</p>					
<p>Note: The Pin Numbers and Input/Output Classifications described in Table 1 identifies the specific input pins in each class.</p>					



Table 4. DC Electrical Characteristics

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	See Table 3				V
V_{IL}	Input Low Voltage	See Table 3				V
V_{OH}	Output High Voltage	See Table 2				V
V_{OL}	Output Low Voltage	See Table 2				V
I_{IL}	Input Leakage Current, All Inputs Except CLKI, CLKO	$V_{IN} = 0.5V$ to $V_{DD} - 0.5V$			1.0	μA
I_{TL}	Tristate Leakage Current	$V_{IN} = 0.5$ to $V_{DD} - 0.5$			1.0	μA
I_{DD}	V_{DD} Supply Current ^(1, 3) Normal Operation	BUSCLK = 10 MHz $V_{DD} = 3.3V$			75	mA
		BUSCLK = 10 MHz $V_{DD} = 5V$			90	mA
		BUSCLK = 20 MHz $V_{DD} = 5V$			150	mA
I_{DDS}	V_{DD} Supply Current Standby Mode ^(1, 2, 3)	BUSCLK = 10 MHz $V_{DD} = 3.3V$			50	μA
		BUSCLK = 10 MHz $V_{DD} = 5V$			50	μA
		BUSCLK = 20 MHz $V_{DD} = 5V$			50	μA

Notes:

1. V_{IH} min = $V_{DD} - 1.0V$, V_{IL} max = 0.8V. All output terminals are at no load.
2. On-chip peripherals with independent clocks are inactive (not being clocked).
3. BUSCLK is the internal processor clock frequency.



AC Characteristics

380C Processor Timing (See Figure 4.)

Specifications apply over Standard Operating Conditions unless otherwise noted.
C_L = 50 pF for outputs.

Table 5. AC Characteristics

Symbol	Parameter	Z80382		Z8L382		Unit
		Min.	Max.	Min.	Max.	
t1	Clock Cycle Time ¹	25	DC	50	DC	ns
t2	Clock High Time ¹	10		20		ns
t3	Clock Low Time ¹	10		20		ns
t4	Clock Rise Time ¹		3		5	ns
t5	Clock Fall Time ¹		3		5	ns
t6	CLKI Low to BUSCLK High Delay		25		35	ns
t7	CLKI High to BUSCLK Low Delay		25		35	ns
t8	BUSCLK High to Output Valid ²		10		10	ns
t9	BUSCLK Low to Output Valid ³		10		10	ns
t10	Input Setup to BUSCLK Rise ⁴	10		15		ns
t11	Input Hold from BUSCLK High ⁴	0		0		ns
t12	$\overline{\text{BUSREQ}}$ Setup to BUSCLK Fall ⁵	10		15		ns
t13	$\overline{\text{BUSREQ}}$ Hold from BUSCLK Low ⁵	0		0		ns
t14	$\overline{\text{WAIT}}$ Setup to BUSCLK Rise ⁶	10		15		ns
t15	$\overline{\text{WAIT}}$ Hold from BUSCLK High ⁶	0		0		ns
t16	$\overline{\text{WAIT}}$ Setup to BUSCLK Fall ⁶	15		15		ns
t17	$\overline{\text{WAIT}}$ Hold from BUSCLK Low ⁶	0		0		ns
t18	$\overline{\text{NMI}}$ Width Low	15		15		ns
t19	$\overline{\text{RESET}}$ Width Low	10		10		t1
t20	$\overline{\text{INT1}}$, $\overline{\text{INT2}}$, $\overline{\text{INT3}}$ Low Width ⁷	15		15		ns
t21	$\overline{\text{INT1}}$, $\overline{\text{INT2}}$, $\overline{\text{INT3}}$ High Width ⁷	15		15		ns



Table 5. AC Characteristics (Continued)

Symbol	Parameter	Z80382		Z8L382		Unit
		Min.	Max.	Min.	Max.	
Notes:						
1. Applies to the oscillator or external clock input. The maximum internal clock frequency (BUSCLK) is limited to 20 MHz for the Z80382 and 10 MHz for the Z8L382. Input clock frequencies greater than these values must use the CLKI/2 mode for creating BUSCLK. This is the default state after Reset.						
2. Applies to A23-0, $\overline{\text{BHEN}}$, $\overline{\text{BLEN}}$, $\overline{\text{IOCLK}}$, $\overline{\text{IOCS1}}$, $\overline{\text{IOCS2}}$, $\overline{\text{ROMCS}}$, $\overline{\text{RAMCSL}}$, $\overline{\text{RAMCSH}}$, M1, $\overline{\text{BUSACK}}$, $\overline{\text{MRD}}$, $\overline{\text{MWR}}$, $\overline{\text{TREFA}}$, $\overline{\text{TREFC}}$, $\overline{\text{TREFR}}$						
3. Applies to D15-0, $\overline{\text{HALT}}$, $\overline{\text{STNBY}}$, $\overline{\text{IORQ}}$, $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{MSIZE}}$, $\overline{\text{BUSACK}}$, $\overline{\text{MRD}}$, $\overline{\text{MWR}}$, $\overline{\text{TREFC}}$, $\overline{\text{TREFR}}$						
4. Applicable for Data Bus and $\overline{\text{MSIZE}}$ inputs.						
5. $\overline{\text{BUSREQ}}$ can also be asserted/deasserted asynchronously.						
6. External waits asserted at $\overline{\text{WAIT}}$ input.						
7. In edge-triggered mode.						