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ZiLOG

Totally Logical

Z90102/103/104

40-PIN LOW-COST DIGITAL TELEVISION CONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O
Z90102	4	236	24
Z90103	6	236	24
Z90104	8	236	24

Note: *General-Purpose

8-Bit CMOS Microcontroller for Consumer Television, Cable and Satellite Receiver Applications.

- Lowest Cost DTC Family Member
- Low Power Consumption
- Fast Instruction Pointer—1.5 µs @ 4 MHz
- Two Standby Modes—STOP and HALT
- Low Voltage Detection/Voltage Sensitive Reset
- Port 2 (8-Bit Programmable I/O) and Port 3 (2-Bit Input, 3-Bit Output) Register Mapped Ports
- Port 6 (6-Bit Input and Tristate Comparator AFC Input) Memory Mapped I/O Ports
- All Digital CMOS Levels Schmitt-Triggered
- Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speed up to 4 MHz
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC or External Clock Drive
- Permanently Enabled Watch-Dog/Power-On Reset Timer
- 3K x 6-Bit Character Generator ROM
- 120 x 7-Bit Video RAM
- Mask Programmable 96-Character Set Display. The 90102, 90103, and 90104 features an 8-Row x 20 Column Format with an 11x15 Pixel Character Cell. The 90102, 90103 90104 is Capable of Supporting English, Korean, Thai, Chinese and Japanese High Resolution Characters.
- Fully Programmable Color Attributes Including Row Character, Row Background/Fringes, Frame Background/Position, Bar Graph Color Change, and Character Size
- Programmable Display Position and Character Size Control
- One Pulse Width Modulators (14-Bit Resolution) for Voltage Synthesis Tuner Control.
- Three Pulse Width Modulator (8-Bit Resolution) for Picture Control
- Three Pulse Width Modulators (6-Bit Resolution) for Audio Control

GENERAL DESCRIPTION

The Z90102/103/104 is a 40-pin Low-Cost Digital Television Controller equipped with 4, 6, and 8 KB of ROM and 236 bytes of RAM. The Z90102/103/104 features ZiLOG's Z8® STOP Mode MCU technology, and is CMOS-compatible. The DTC offers a mask-programmed ROM which enables the Z8® MCU to be used in a high-volume production application device embedded with a custom program (customer supplied program). The devices are combined togeth-

GENERAL DESCRIPTION (Continued)

er with the Z86C27 and Z86127 to provide support for mid-range and low-end TV applications.

ZiLOG's DTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z90102/3/4 architecture is characterized by utilizing ZiLOG's advanced highly-integrated design methodology. The device features an 8-bit internal data path controlled by a Z8 microcontroller, On Screen Display (OSD) logic circuits, and Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and 3), interrupt control logic (one software, two external and three internal interrupts), and a standby mode recovery input port (Port 3, P30).

The OSD control circuits support 8 rows x 20 columns of characters. The character color is specified by row. One of the eight rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying either low resolution (5 x 7 dot pattern) or high-resolution (11 x 15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Three 6-bit PWM ports are used for controlling audio signal levels. Three 8-bit PWM ports are used to vary picture levels.

For DTC applications demanding powerful I/O capabilities, the Z90102/3/4 provides 24 I/O pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide timing, status signals, parallel I/O, and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Video RAM, and Register File. The Register File is composed of 236 bytes of general-purpose registers, two I/O Port registers, 15 control and status registers, and three reserved registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the DTC offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Note: All Signals with an overline, "$\overline{\ }$", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

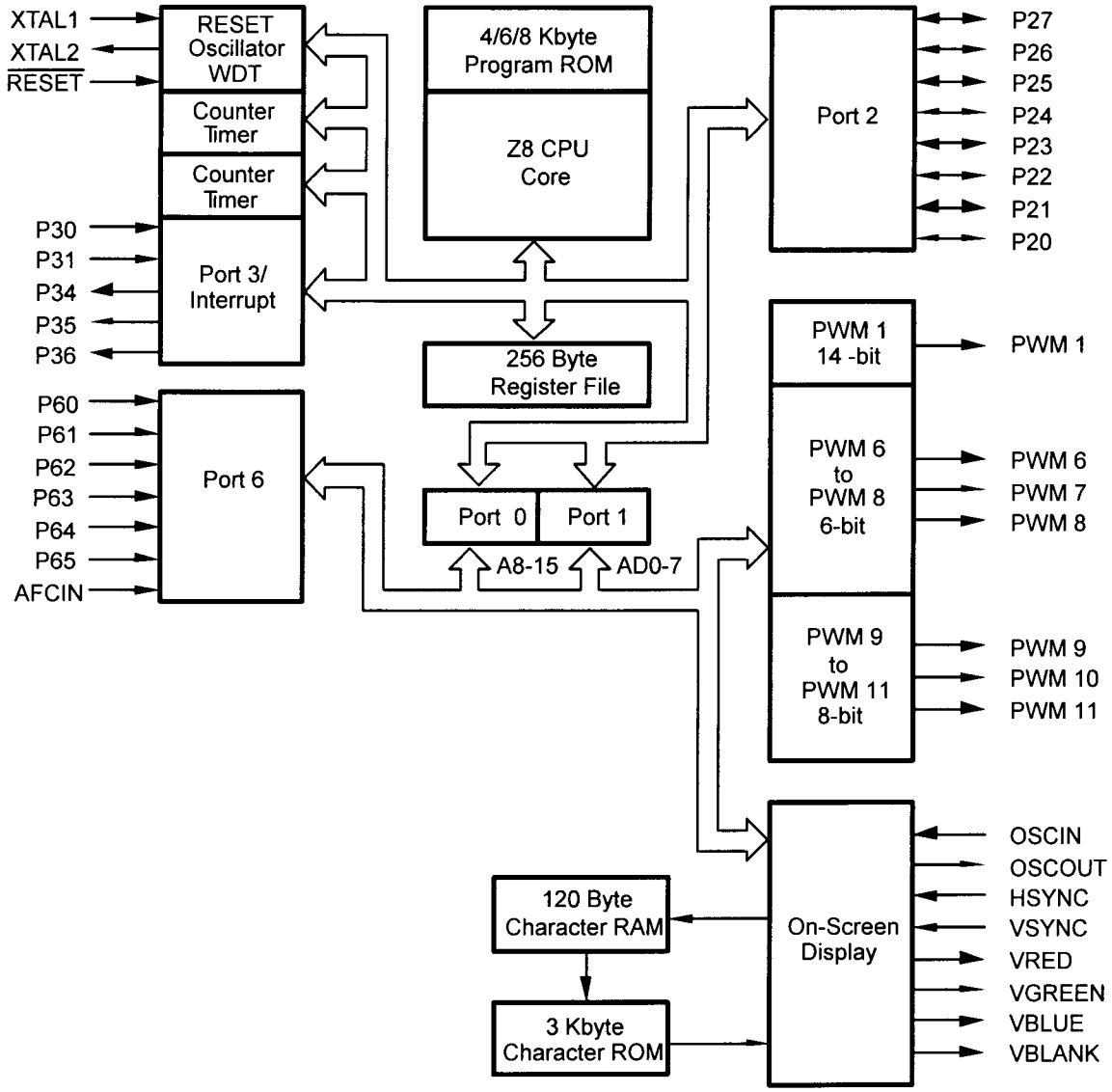


Figure 1. Functional Block Diagram

PIN DESCRIPTION

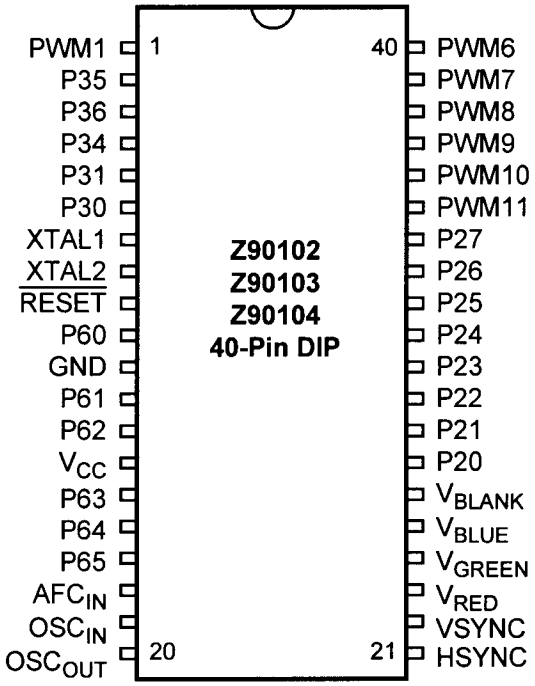


Figure 2. 40-Pin Mask-ROM Plastic DIP

Table 1. 40-Pin Mask-ROM Plastic DIP

40-Pin	Name	Function	Direction
1	PWM1	Pulse Width Modulator 1	Output
2,3	P35–36	Port 3, Pins 5, 6	Output
4	P34	Port 3, Pin 4	Output
5	P31	Port 3, Pin 1	Input
6	P30	Port 3, Pin 0	Input
7	XTAL1	Crystal Oscillator	Input
8	XTAL2	Crystal Oscillator	Output
9	$\overline{\text{RESET}}$	System Reset	Input
10	P60	Port 6, Pin 0	Input
11	GND	Ground	
12	P61	Port 6, Pin 1	Input
13	P62	Port 6, Pin 2	Input
14	V_{CC}	Power Supply	
15,16,17	P63–65	Port 6, Pins 3, 4, 5	Input
18	AFC_{IN}	AFC Voltage Level	Input
19	OSC_{IN}	Video Dot Clock Osc	Input
20	OSC_{OUT}	Video Dot Clock Osc	Output
21	HSYNC	Horizontal Sync	Input
22	VSYNC	Vertical Sync	Input

Table 1. 40-Pin Mask-ROM Plastic DIP

40-Pin	Name	Function	Direction
23	V_{RED}	Video Red	Output
24	V_{GREEN}	Video Green	Output
25	V_{BLUE}	Video Blue	Output
26	V_{BLANK}	Video Blank	Output
27–34	P20–27	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
35	PWM11	Pulse Width Modulator 11	Output
36	PWM10	Pulse Width Modulator 10	Output
37	PWM9	Pulse Width Modulator 9	Output
38	PWM8	Pulse Width Modulator 8	Output
39	PWM7	Pulse Width Modulator 7	Output
40	PWM6	Pulse Width Modulator 6	Output

PIN DESCRIPTION

XTAL1, XTAL2. . These pins are a time-based input and output, respectively. These pins connect to the internal parallel-resonant clock crystal (4 MHz max) oscillator circuit with two capacitors to GND. XTAL1 is also used as an external clock input.

SCLK System Clock. . SCLK is the internal system clock. This pin is used to clock external glue logic.

HSYNC. This pin represents a Schmitt triggered, CMOS-level input pin. Horizontal Sync is an input pin that accepts an externally generated Horizontal Sync signal of either negative or positive polarity.

VSYNC. This pin represents a Schmitt-triggered, CMOS-level input pin. Vertical Sync is an input pin that accepts an externally generated Vertical Sync signal of either negative or positive polarity.

OSC_{IN}, OSC_{OUT}. These pins represent the Video Oscillator input and output, respectively. Oscillator input and output pins are used here for on-screen display circuits. These pins connect to an inductor and two capacitors to generate the character dot clock (typically around 6 MHz). The dot clock frequency determines the character pixel width and phase synchronized to HSYNC.

V_{BLANK}/Video Blank. This pin is a CMOS output pin with programmable polarity. V_{BLANK} is used as a superimpose control port to display characters from video RAM. The signal controls Y signal output of the CRT and turns off the incoming video display, while the characters in video RAM are superimposed on the screen. The red, green, and blue outputs drive the three electron guns on the CRT directly, while the blank output turns off the Y signal.

V_{BLUE}/Video Blue. This pin is a CMOS Output of the Blue video signal (B–Y) and is programmable for either polarity.

V_{GREEN}/Video Green. This pin is a CMOS Output of the Green video signal (G–Y) and is programmable for either polarity.

V_{RED}/Video Red. This pin is a CMOS Output of the Red video signal (R–Y) and is programmable for either polarity.

Port 2 (P27–P20). Port 2 is an 8-bit, CMOS-compatible port, and is bit-programmable for either input or output. Input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 32).

Port 3 (P30, P31, P34–P36). Port 3 (P30 input), is read directly. If appropriately enabled, a negative edge event is latched in IRQ3 to initiate an IRQ3 vectored interrupt. An application could place the device in STOP Mode when P30 goes Low (in the IRQ3 interrupt routine). P30 initiates a STOP Mode recovery when it subsequently goes to a High. Port 3, P31 are read directly. If appropriately enabled, a negative edge event is latched in IRQ2 to initiate an IRQ2 vectored interrupt. P31 High is signified as the TIN signal to Timer1. Port 3, P34 and P35 are general-purpose output lines. Port 3, P36 is used as a general-purpose output or as an output for TOUT (from Timer1 or Timer2) or SCLK (Figure 34).

Port 6 (P65–P60). Port 6 is a 6-bit, CMOS-compatible input port that is Schmitt-triggered. The outputs of the AFC comparators internally feed into the Port 6, bit 6 and bit 7 inputs (Figure 35).

AFC_{IN}. This pin is a comparator input port that is memory-mapped. The input signal is supplied to two comparators with VTH1=2/5 V_{CC} and VTH2=3/5 V_{CC} typical threshold voltage. The comparator outputs are internally connected to Port 6, bit 6 and bit 7. AFC_{IN} is typically used to detect the AFC voltage level to accommodate digital automatic fine-tuning functions.

Pulse Width Modulator 1 (PWM). PWM1 is typically used as the D/A converter for Voltage Synthesis Tuning systems. This pn is a push-pull output with 14-bit resolution.

Pulse Width Modulator 6–8 (PWM). PWM8–PWM6 are Pulse Width Modulators with 6-bit resolution.

Pulse Width Modulator 9, 10, 11 (PWM). PWM9–PWM11 are Pulse Width Modulator circuits with 8-bit resolution. These PWMs are 12 volt, open-drain outputs.

Pulse Width Modulator 1, 6, 7, 8 (PWM). These pins are programmed as general-purpose outputs. PWM 1 is 5 V_{OH} push-pull, and PWMs 6, 7, 8 are 12 volt open-drain outputs.

$\overline{\text{RESET}}$. This pin is the System Reset. Code is executed from memory address 000CH after the $\overline{\text{RESET}}$ pin is set to a High level. The reset function is also carried out by detecting a V_{CC} transition state (automatic Power-On Reset) so that the external reset pin can be permanently tied to V_{CC}. A low level on $\overline{\text{RESET}}$ forces a restart of the device.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters	Min	Max	Units	Notes
V_{CC}	Power Supply Voltage	–0.3	+7	V	1
V_I	Input Voltage	–0.3	V_{CC} +0.3	V	
V_I	Input Voltage	–0.3	V_{CC} +0.3	V	2
V_O	Output Voltage	–0.3	13.2	V	3,4
I_{OH}	Output Current High		–10	mA	5
I_{OH}	Output Current High		–100	mA	6
I_{OL}	Output Current Low		20	mA	5
I_{OL}	Output Current Low		200	mA	6
T_A	Operating Temperature				7
T_{STG}	Storage Temperature	–65	+150	C	

Notes:
1. Voltage on all pins with respect to GND.
2. Port 2 open-drain.
3. PWM open-drain outputs.
4. Absolute maximum operating voltage 13.2V.
   Absolute maximum momentary (non-operating) voltage is 16.0V.
5. One pin.
6. All pins.
7. See Ordering Information.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 3).

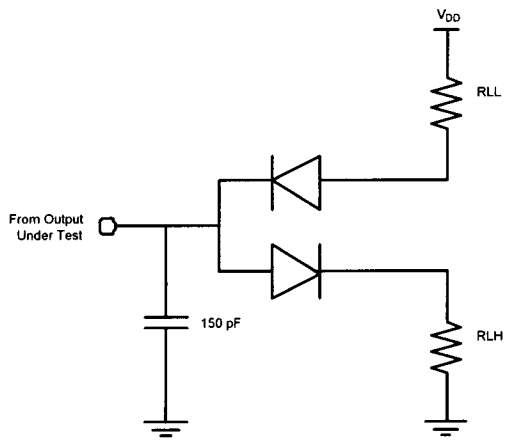


Figure 3. Test Load Diagram

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V; Freq =1.0 MHz; unmeasured pins to GND.

Parameter	Max	Units
Input capacitance	10	pF
Output capacitance	20	pF
I/O capacitance	25	pF
AFC_{IN} input capacitance	10	pF

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +4.5V to +5.5V; F_{OSC} = 4 MHz

		T_A = 0°C to +70°C		Typical			
Sym	Parameter	Min	Max	@ 25°C	Units	Conditions	Notes
V_{IL}	Input Voltage Low	0	0.2 V_{CC}	1.48	V		
V_{ILC}	Input XTAL/Osc In Low		0.07 V_{CC}	0.98	V	External Clock Generator Driven	
V_{IH}	Input Voltage High	0.7 V_{CC}	V_{CC}	3.0	V		
V_{IHC}	Input XTAL/Osc In High	0.8 V_{CC}	V_{CC}	3.2	V	External Clock Generator Driven	
V_{HY}	Schmitt Hysteresis	0.1 V_{CC}		0.8	V		
V_{PU}	Maximum Pull-Up Voltage		13.2		V		1,2
V_{OL}	Output Voltage Low		0.4 0.4	0.16 0.19	V V	I_{OL} = 1.00 mA I_{OL} = 0.75 mA 1	
V_{00-01}	AFC Level 01 In		0.45 V_{CC}	1.9	V		
V_{01-11}	AFC Level 11 In	0.5 V_{CC}	0.75 V_{CC}	3.12	V		
V_{OH}	Output Voltage High	V_{CC} –0.4		4.75	V	I_{OH} = –0.75 mA	
I_{IR}	Reset Input Current		–80	–46	µA	V_{RL} = 0_V	
II_L	Input Leakage	–3.0	3.0	0.01	µA	0V, V_{CC}	
I_{OL}	Tristate Leakage	–3.0	3.0	0.02	µA	0V, V_{CC}	
I_{CC} I_{CC1} I_{CC2}	Supply Current		20 6 10	13.2 3.2 2.0	mA mA µA	All inputs at rail & outputs floating	

Notes:

1. PWM open-drain.
2. Recommended operating voltage 12V with maximum positive tolerance 10% (for example, 13.2V).

AC CHARACTERISTICS

Timing Diagrams

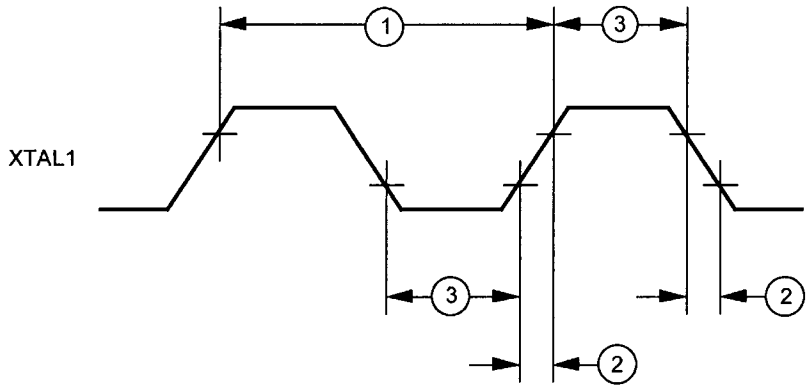


Figure 4. External Clock

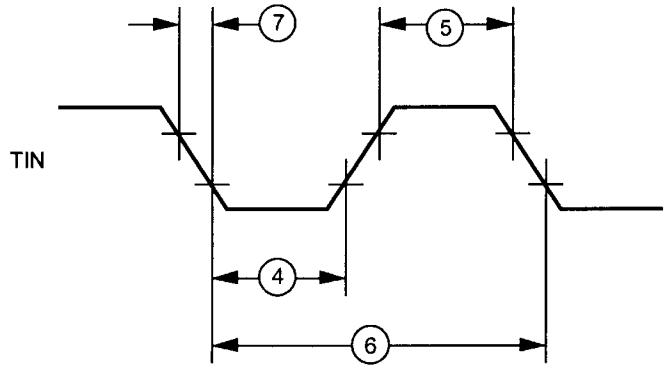


Figure 5. Counter Timer

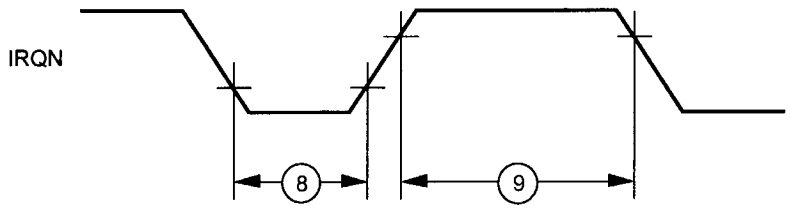


Figure 6. Interrupt Request

AC CHARACTERISTICS (Continued)

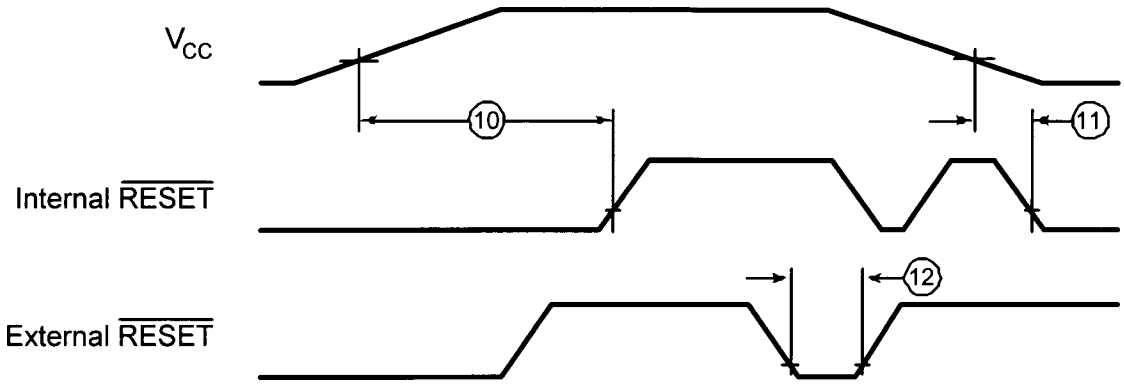


Figure 7. Power-On Reset

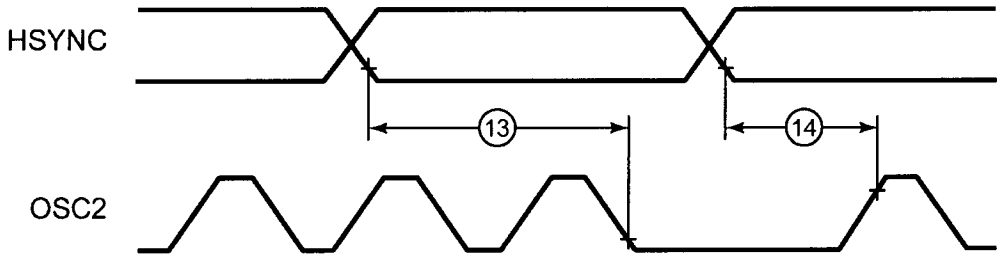


Figure 8. On-Screen Display

AC CHARACTERISTICS*

T_A = 0° C to +70° C; V_{CC} = +4.5V to +5.5V; F_{OSC} = 4 MHz

No	Symbol	Parameter	Min	Max	Unit
1	TpC	Input Clock Period	250	1000	ns
2	TrC,TfC	Clock Input Rise and Fall		15	ns
3	TwC	Input Clock Width	125		ns
4	TwTinL	Timer Input Low Width	70		ns
5	TwTinH	Timer Input High Width	3TpC		
6	TpTin	Timer Input Period	8TpC		
7	TrTin,TfTin	Timer Input Rise and Fall		100	ns
8a	TwIL	Int Req Input Low	70		ns
8b	TwIL		3TpC		
9	TwIH	Int Request Input High	3TpC		
10	TdPOR	Power On Reset Delay	25	100	ms
11	TdLVIRES	Low Voltage Detect to	200		ns
		Internal RESET Condition			
12	TwRES	Reset Minimum Width	5TpC		
13	TdHsOl	HSYNC Start to VOSC Stop	2TpV	3TpV	
14	TdHsOh	HSYNC End to VOSC Start		1TpV	
15	TdWDT	WDT Refresh Time		12	ms

Note:
*Refer to DC Characteristics for details on switching levels.

FUNCTIONAL DESCRIPTION

The Z8 DTC incorporates special functions to enhance the Z8's versatility in consumer, industrial and television control applications.

Pulse Width Modulator (PWM). The Z90102/103/104 features seven PWM channels (Figure 9). There are three types of PWM circuits: PWM1 (one channel of 14-bit resolution) typically used for Voltage Synthesis Tuning, PWM8–PWM6 (three channels of 6-bit resolution) typically used for audio level control, and PWM9, 10, 11 (three channels of 8-bit resolution) typically used for picture level control. The PWM control registers are mapped into external memory and are accessed through LDE and LDEI instructions.

PWM1. The PWM circuit is a push-pull output.

PWMs 6 through 11. The PWM circuits exhibit maximum values (on-times) when all 1s are loaded in their PWM Value registers (and minimum value for all 0s). PWM1 exhibits a maximum value for all 0s and minimum value for all 1s.

On-Screen Display (OSD). The OSD features a capability of displaying 8 rows x 20 columns of 96 kinds of characters for high-resolution (11 x 15 dots) patterns (Figure 10 and Figure 11).

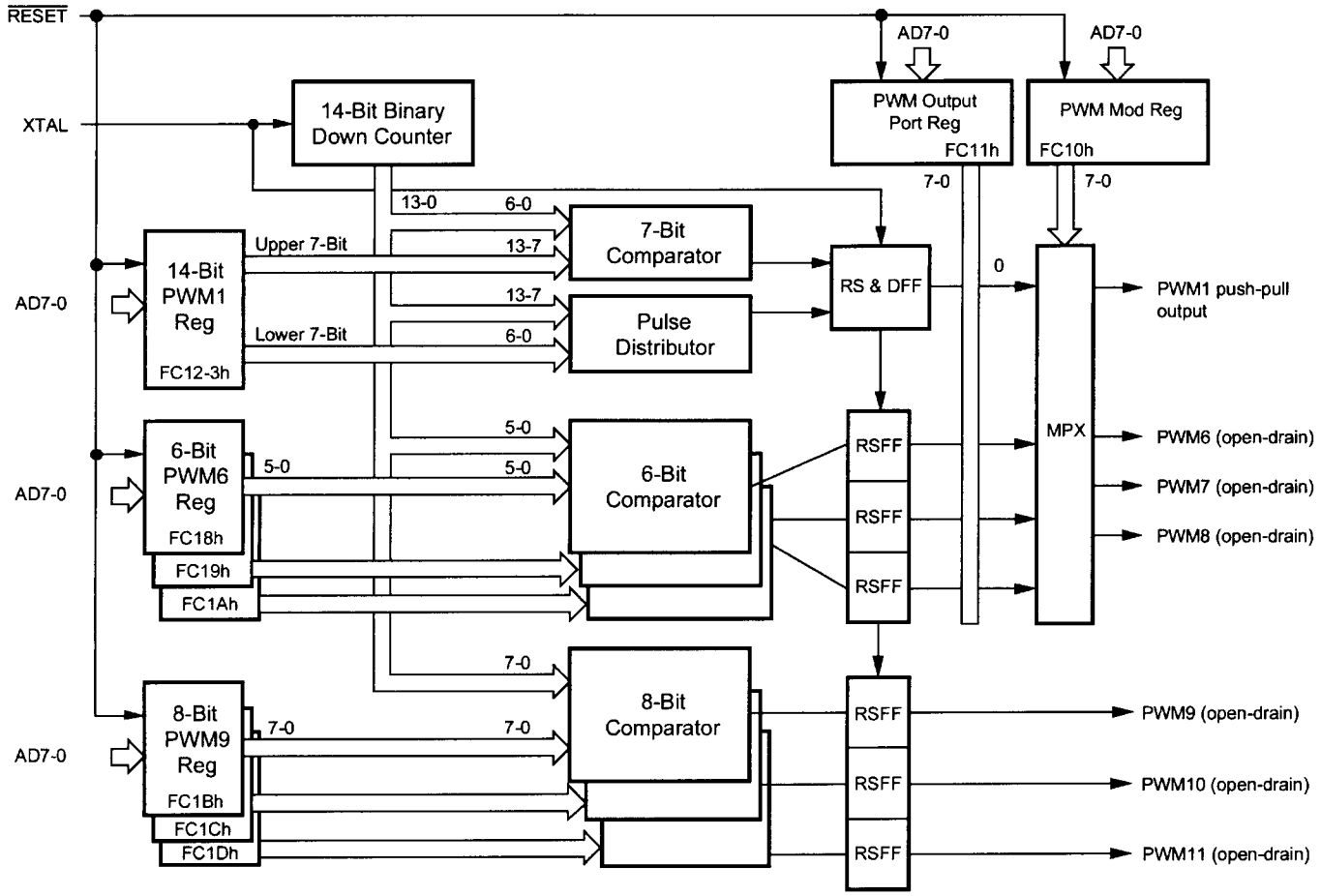


Figure 9. Pulse Width Modulator Block Diagram

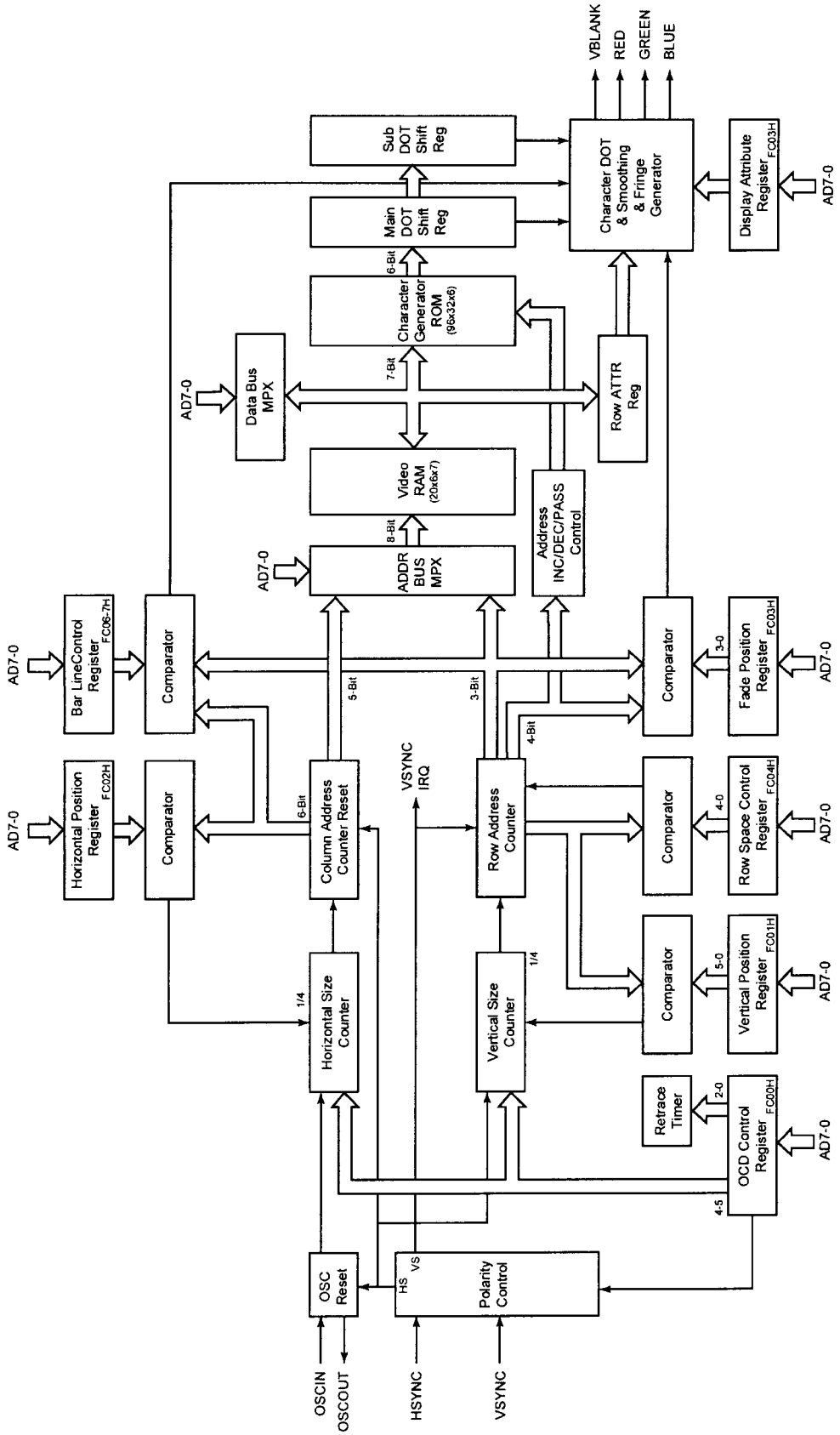


Figure 10. On-Screen Display Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

The OSD features are as follows:

- **Character Color:** Seven kinds of color are specified on a row basis.
- **Character Pixel Size:** Four character pixel sizes are selected for a high-resolution (1HL, 2HL, 3HL, and 4HL) Horizontal Line (HL).
- **Polarity Selections:** This function selects active Low or High for horizontal/vertical sync input and RGB outputs.
- **Display Position:** This function displays 64 vertical positions by 4HL units and 64 horizontal positions by a 4-dot clock.
- **Inter-Row Spacing:** Inter row vertical line spacing is set from 2HL to 17HL.
- **Fade In/Out Control:** Fade position is determined in vertical direction.
- **Bar Line Type Display:** One of the rows is selected to display an analog bar line every half column by setting second color with the proper character set.
- **Fringe Function:** Fringe off/on and the color selected using this feature.
- **Background Color:** Eight kinds of color including black background color.
- **ON/OFF Control:** Character display backgrounds are turned on and off using this feature.
- **Number of Display Characters:** 8 rows x 20 columns.
- **Character Set:** 96 (11 x 15 dots).

Character Generator ROM. The character generator ROM is organized as 3 KB of six bits. The ROM defines either 11 x 15 dot (high resolution)

Video RAM. The Video RAM is organized as 8-row arrays (21 x 7 bits each). The first location of each row array contains the attribute for that row. Row attributes include programmable character color, row background color, and control for background off/on. The next 20 bytes contain row character data. Each character byte contains the ASCII code in order to select one of the 96 displayable characters. LDE or LDEI instructions are required to access the Video RAM (Figure 11).

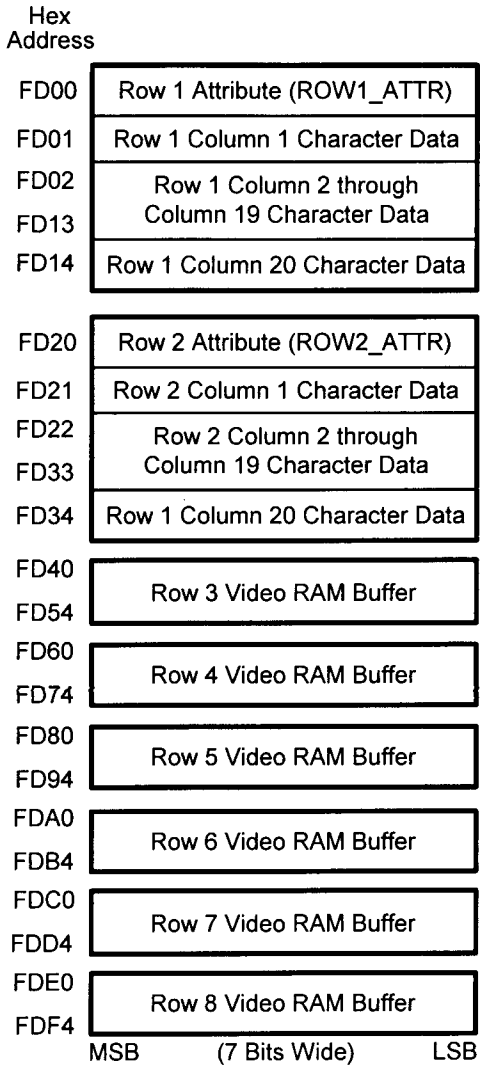


Figure 11. Video RAM Configuration

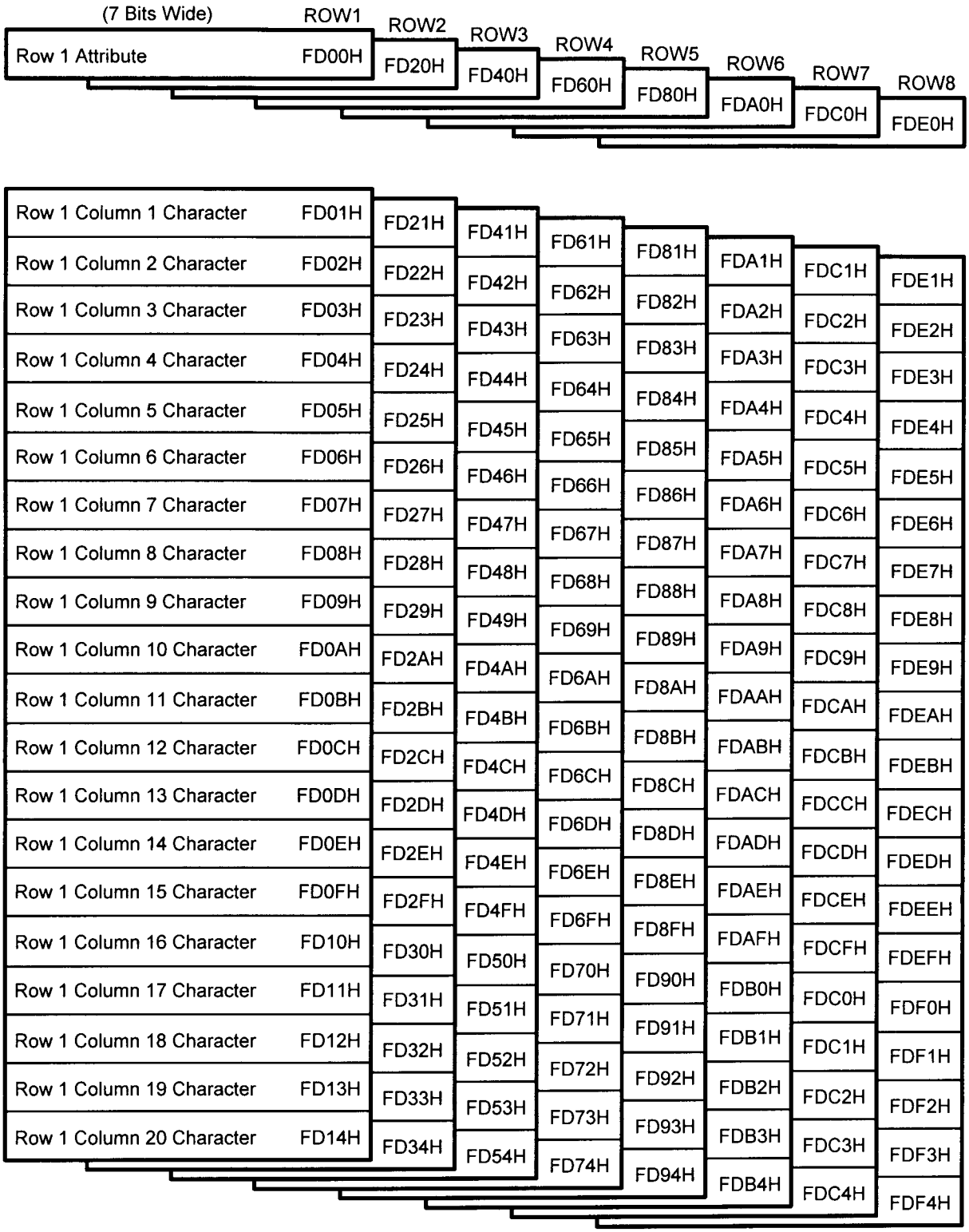


Figure 12. Video RAM Map
(Write/Read Registers)

FUNCTIONAL DESCRIPTION (Continued)

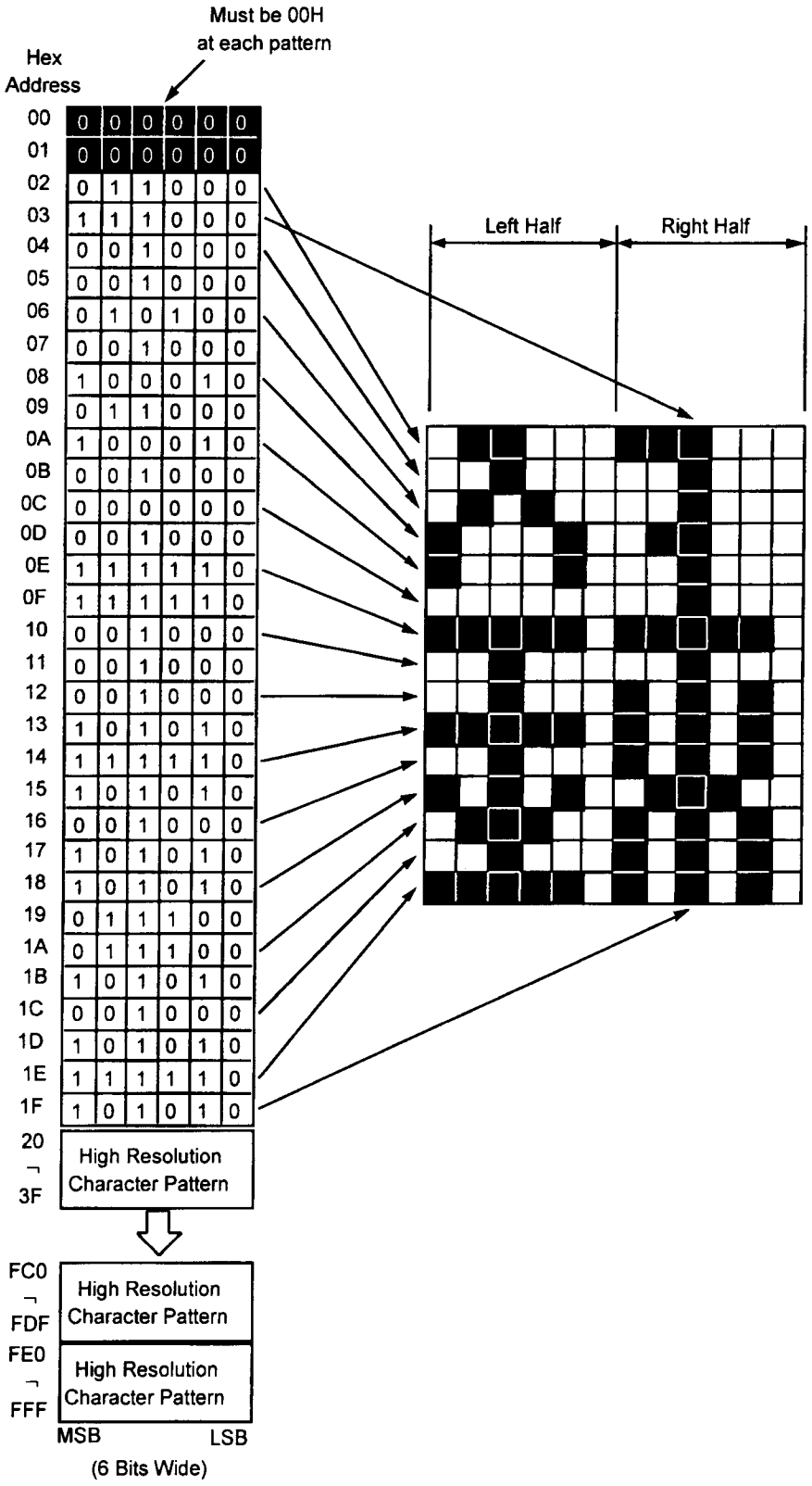


Figure 13. High Resolution Character ROM Configuration

Program Memory. The IRQ vector table is located in the lower address space. The vector address is fetched after the corresponding interrupt and program control is passed to the specified vector address. The IRQ1 vector is fixed to the VSYNC interrupt request and occurs at the leading edge of the filtered VSYNC input. Program memory starts at address 000CH after reset.

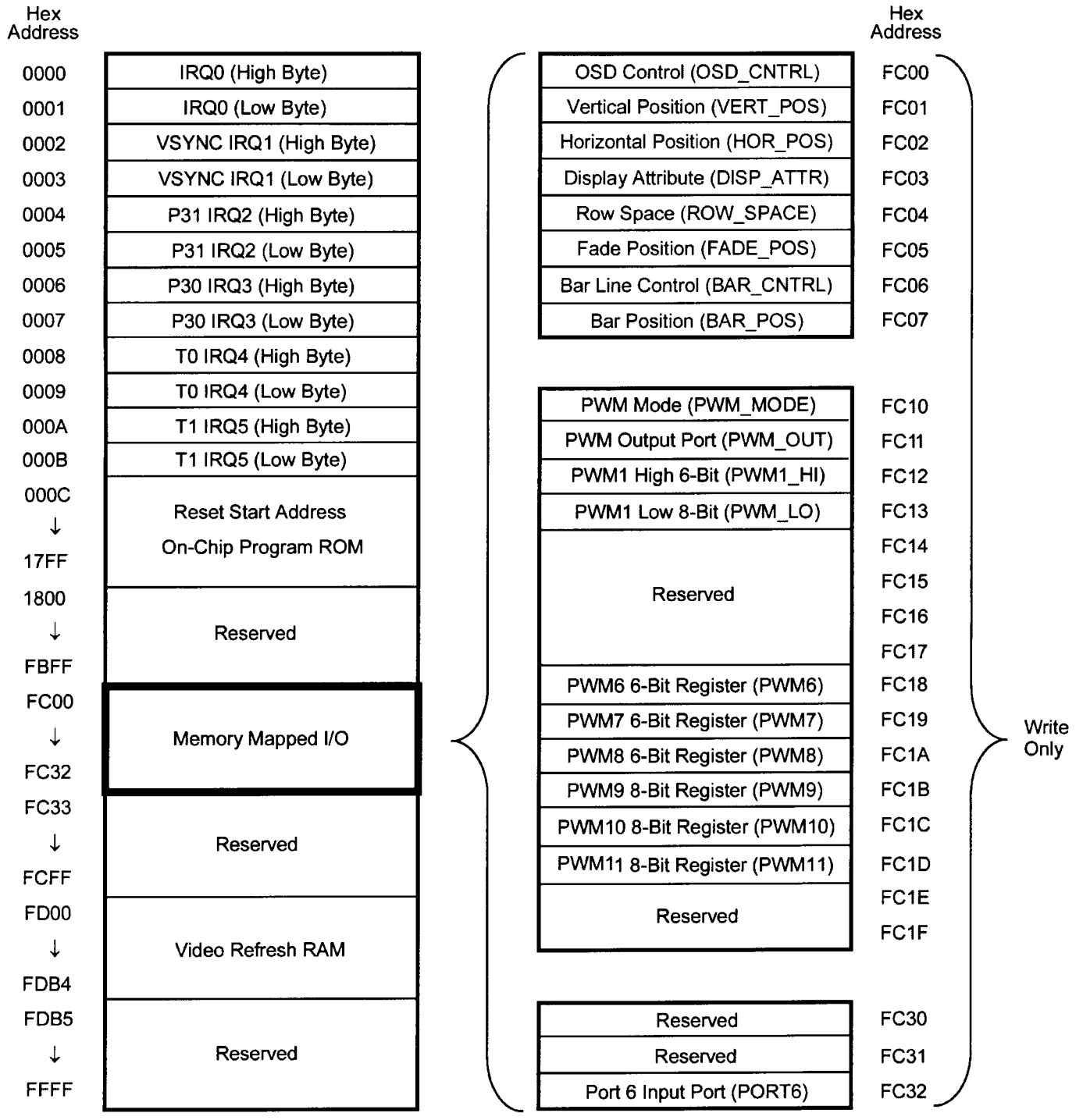


Figure 14. Program Memory

FUNCTIONAL DESCRIPTION (Continued)

Memory Mapped Register. All control registers and I/O ports (except Port 2 and Port 3) are assigned to program memory space. Address space FC00H contains OSD control registers, PWM output registers, and Port 6 I/O registers. Two bits of the decoded AFC_{IN} port are assigned to the Port 6 input port. LDE and LDEI instructions are required to transfer data between the Register File and the Memory Mapped Registers.

Register File. A total of 256 byte registers are implemented in the Z8 core. Address 00H, 01H and FOH are reserved. The register file consists of two I/O Port registers, 236 general-purpose registers and 15 control and status registers (Figure 15). The instructions access registers directly or indirectly with an 8-bit address field, thereby allowing short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into sixteen working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group (Figure 16).

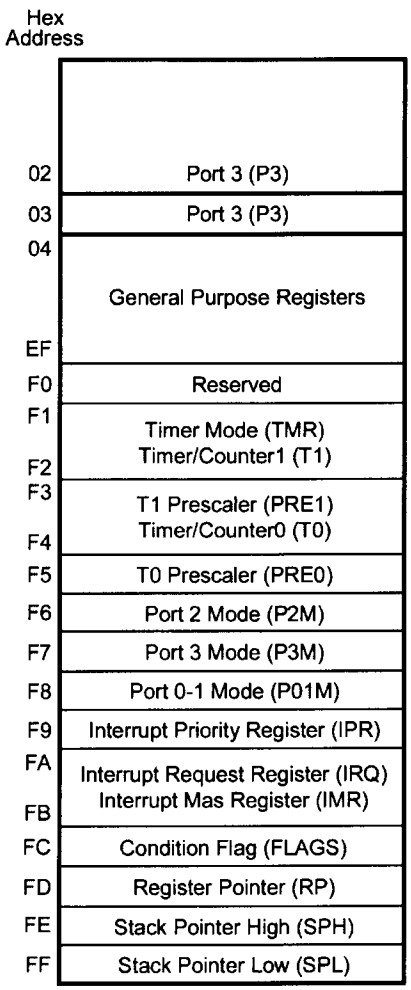


Figure 15. Register File Configuration

Note: Register Bank E0–EF is only accessed through a working register and indirect addressing modes.

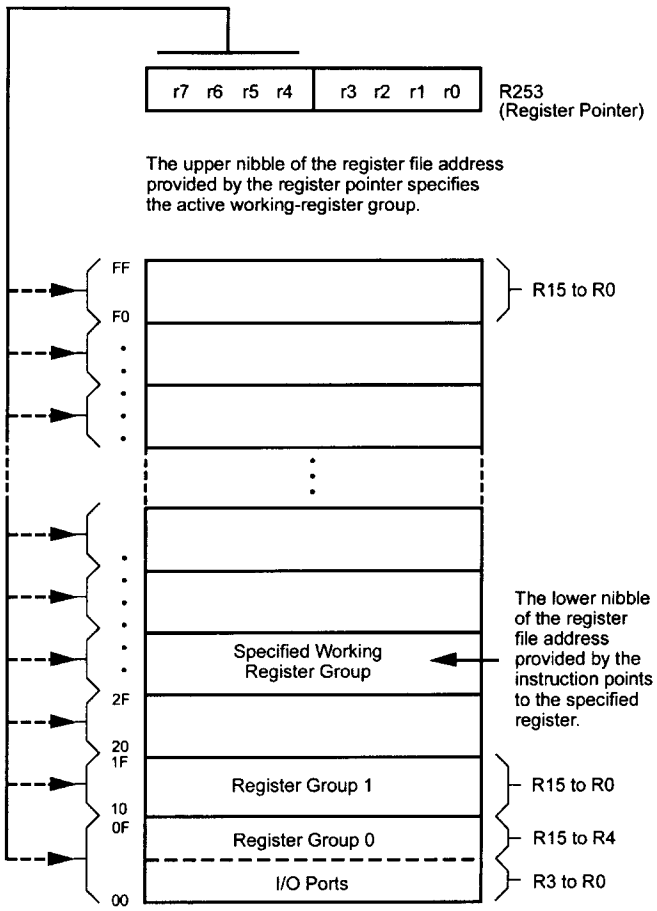


Figure 16. Register Pointer—Detail

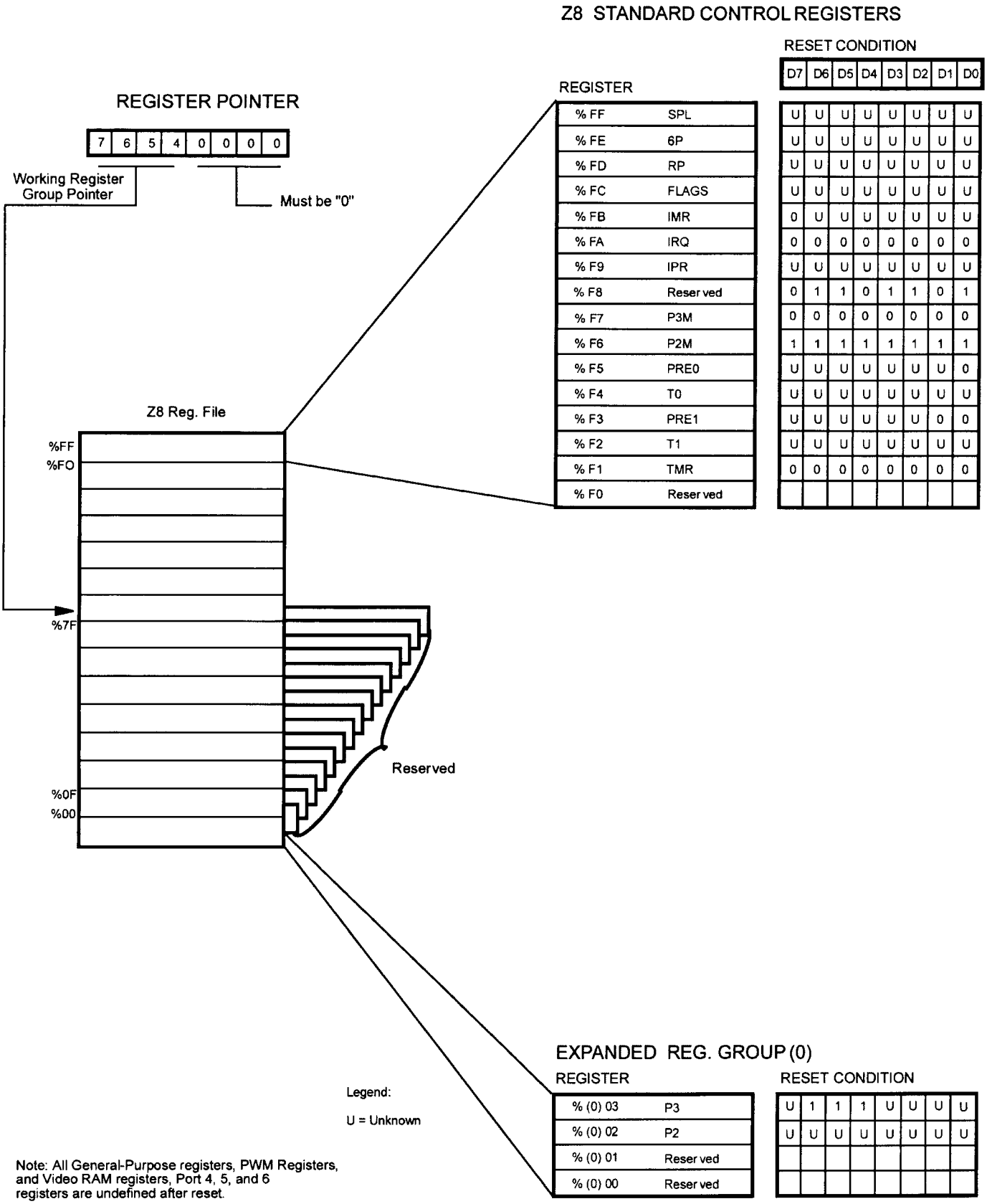


Figure 17. Z90102/3/4 Register File Reset Condition

FUNCTIONAL DESCRIPTION (Continued)

Stack. Either the internal register file or the external data memory is used for the stack. An 8-bit Stack Pointer is used for the internal stack that resides within the 236 general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0–T1), each driven by its own 6-bit programmable prescaler (PRE0 and PRE1). The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 18).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user definable and is the internal microprocessor clock (XTAL clock/4), or an external signal input through Port 3, P31. The counter/timers are programmably cascaded by connecting the T0 output to the input of T1.

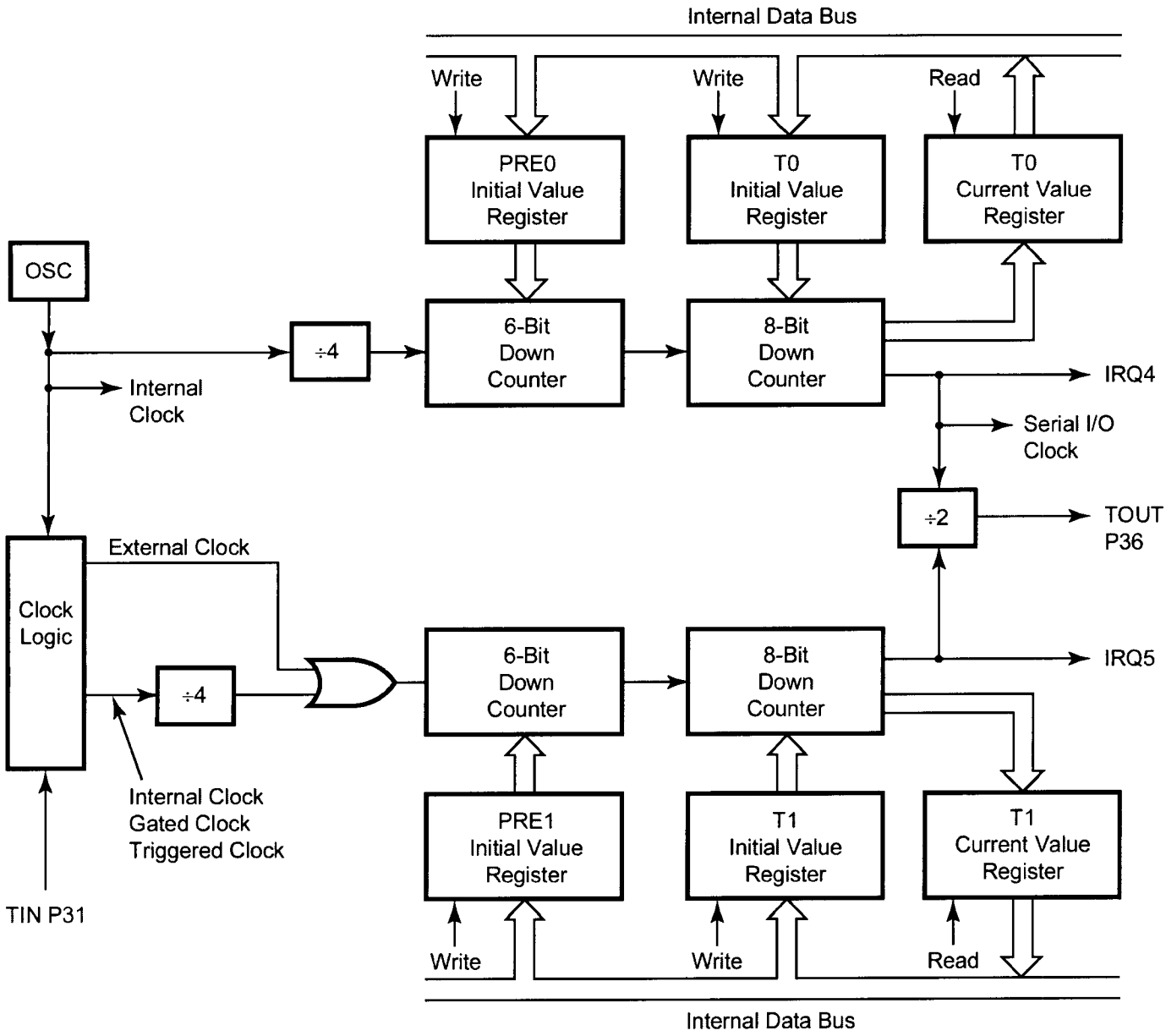


Figure 18. Counter/Timer Block Diagram

Interrupts. The DTC features six different interrupts from six different sources. These interrupts are maskable and prioritized (Figure 19). The six sources are divided as follows: two sources are claimed by Port 3 (P30, P31), one by VSYNC, two by the counter/timers, and one by software trigger only.

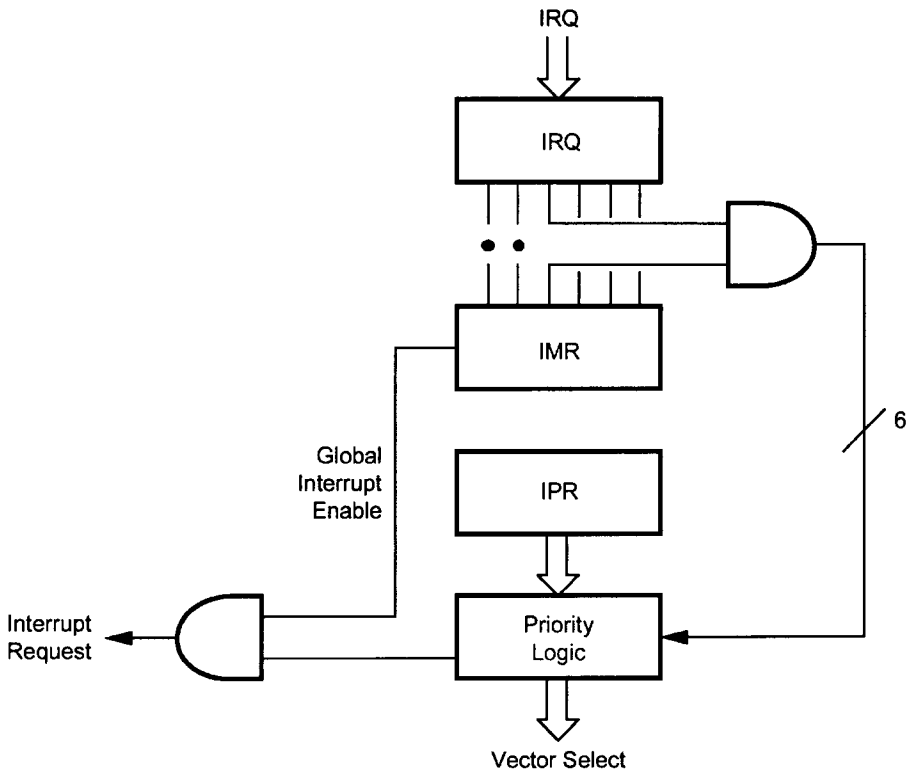


Figure 19. Interrupt Block Diagram

HALT Mode. The Z90102/3/4 is driven by two internal clocks—TCLK and SCLK. Both clocks oscillate at the crystal frequency. TCLK provides the clock signal for the counter-timers and the interrupt block. SCLK provides the clock signal for all other CPU blocks. HALT Mode turns off the internal CPU clock (SCLK), but not the XTAL oscillation. The counter/timers and external interrupts remain active. The device may be recovered by interrupts (either externally or internally generated). An interrupt request may be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. The STOP instruction stops crystal oscillation, thereby stopping both SCLK and TCLK, and causing the device to cease operation. The STOP Mode is released by two methods. The first method is to reset the device. A High input condition on Port 3 (P30) is the second method. After releasing the STOP Mode by using either one of the two methods, program execution begins at location 000CH. To complete an instruction prior to entering the standby modes, a NOP instruction must be placed before the HALT or STOP instructions. This instruction is required because of the instruction pipelining.

Example:

```
FF NOP          ; clear the pipeline
6F STOP         ; enter STOP Mode
                  or
FF NOP          ; clear the pipeline
7F HALT         ; enter HALT Mode
```

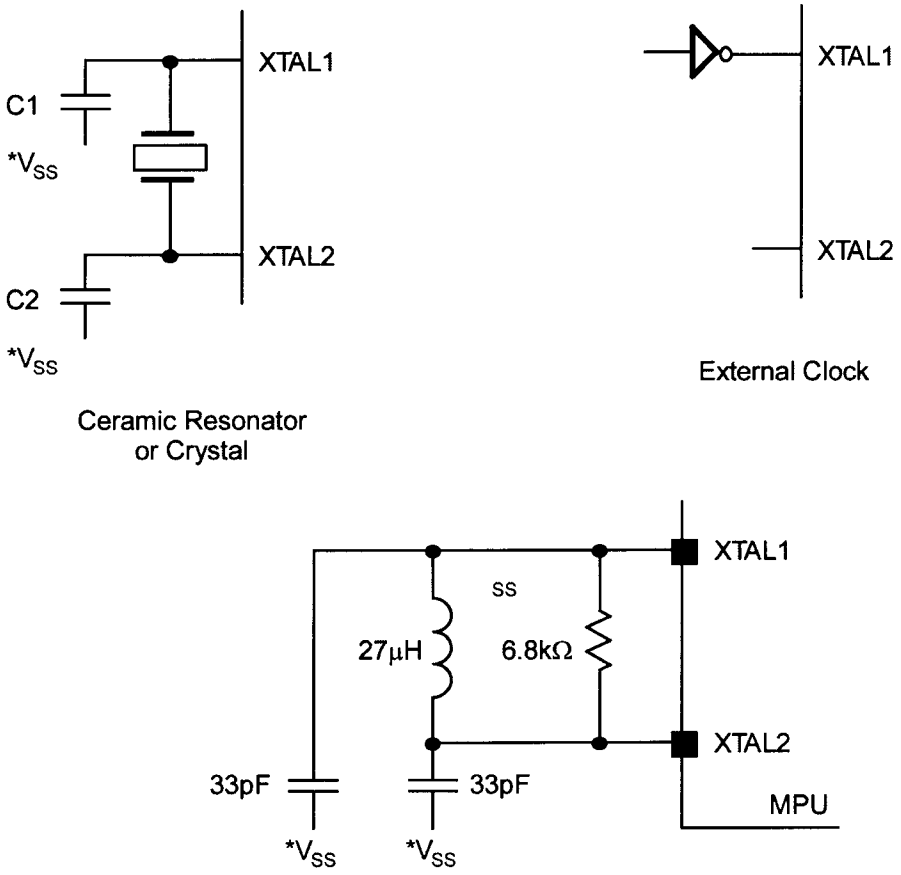
Note: In STOP Mode, the XTAL2 pin features an internal pull-up while the OSC_{OUT} features an internal pull-down.

Clock. The Z90102/3/4 on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal is an AT

FUNCTIONAL DESCRIPTION (Continued)

cut, parallel-resonant, 4-MHz max crystal, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal source is connected across XTAL1 and XTAL2 using the crystal manufacturer's recommended capacitors (10 pF < CL < 300 pF, where C1=C2=CL) from each pin to device ground (Figure 20).



* Must be connected to V_{SS} pin and not system ground.

Figure 20. Oscillator Configuration

Watch-Dog Timer (WDT). The Z90102/3/4 is equipped with a permanently enabled Watch-Dog Timer which must be refreshed every 12 ms. Failure to refresh the timer results in a reset of the device. The WDT is permanently enabled and is initially reset upon POR. Every subsequent WDT instruction resets the timer. The Watch-Dog Timer may or may not be enabled during the STOP Mode. The instruction WDT 4F (HEX) enables the timer during HALT. If the WDH instruction is used, and if the HALT Mode is not released, causing the Watch-Dog Timer to not be retriggered (by the WDT instruction) within 12 ms, a device reset occurs. The WDT instruction affects the Z (Zero) S (Sign), and V (Overflow) flags. WDT does not run during STOP Mode.

V_{CC} Voltage Sensitive Reset (VSR). Reset is globally driven if V_{CC} is below the specified voltage (Figure 21).

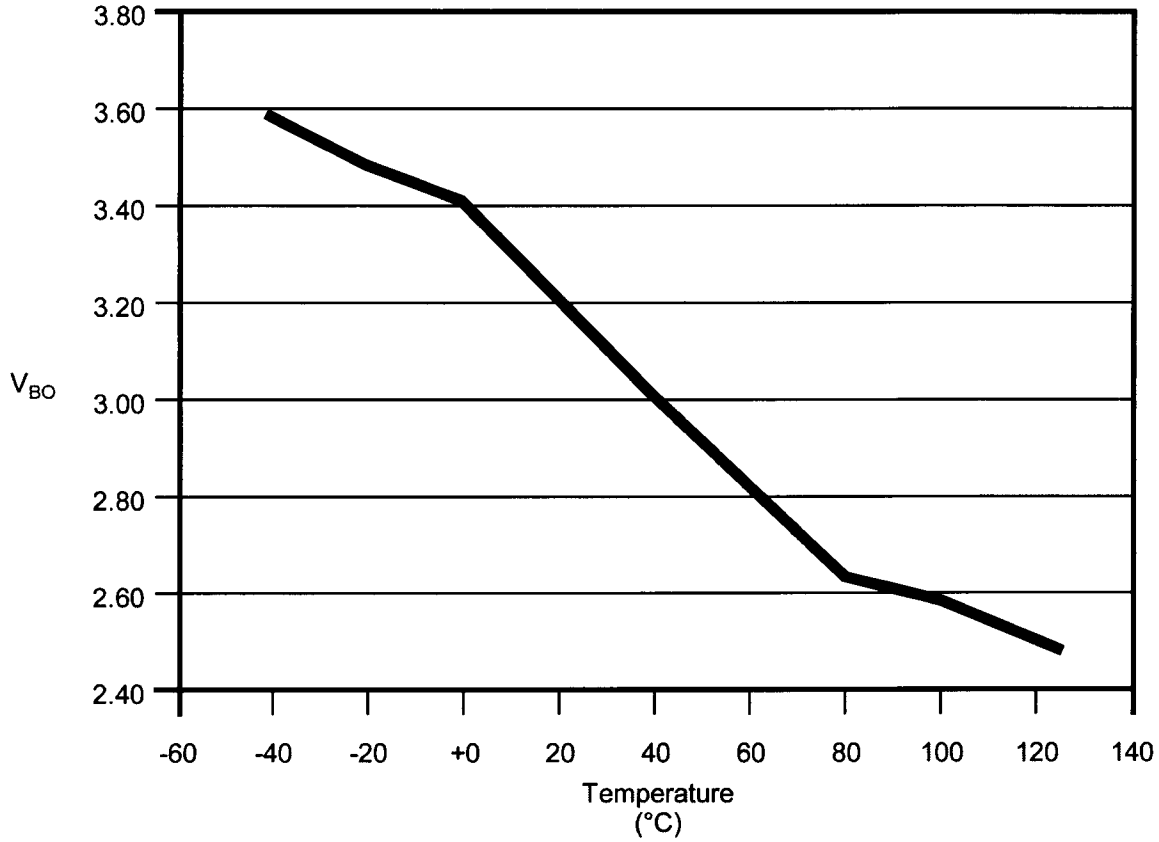


Figure 21. Voltage Sensitive Reset vs Temperature

STANDARD CHARACTER SETS

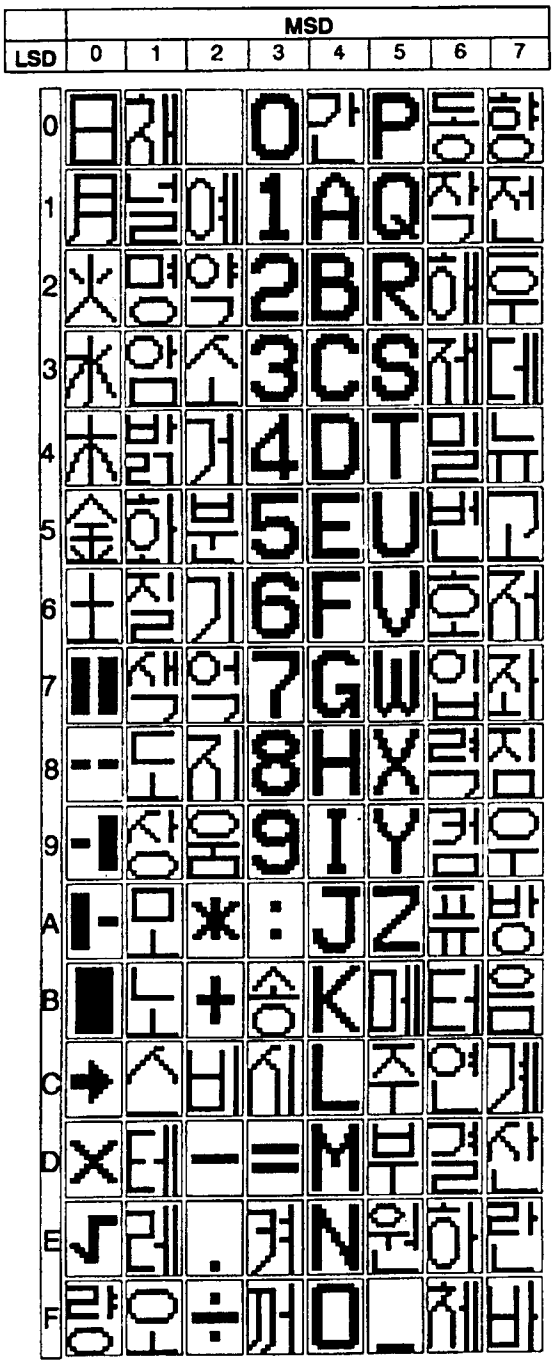


Figure 22. Standard Character Sets

SUMMARY

Input/Output Circuits

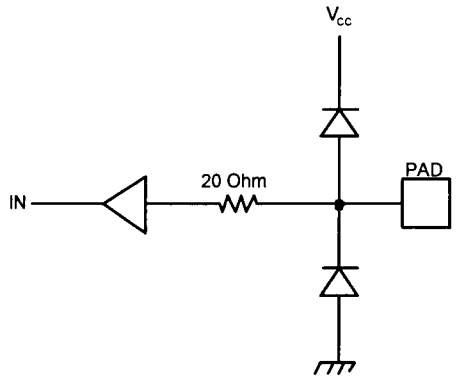


Figure 23. Input Only (Pad Type 1)

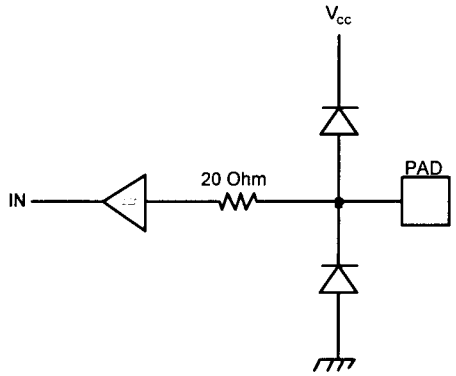


Figure 24. Input Only, Schmitt-Triggered (Pad Type 2)

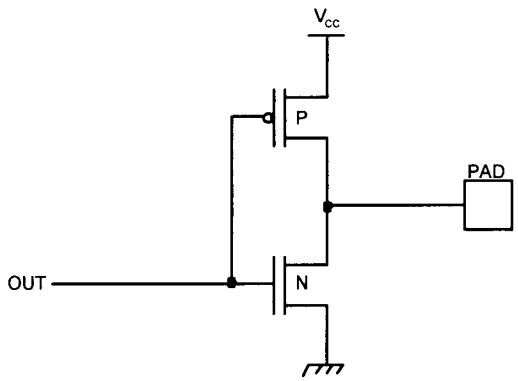


Figure 25. Output Only (Pad Type 3)

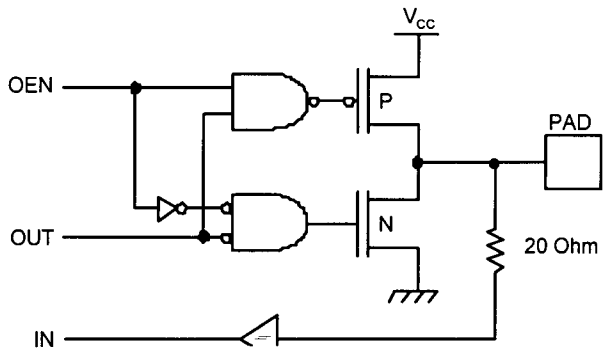


Figure 26. Input/Output Tristate (Pad Type 4)

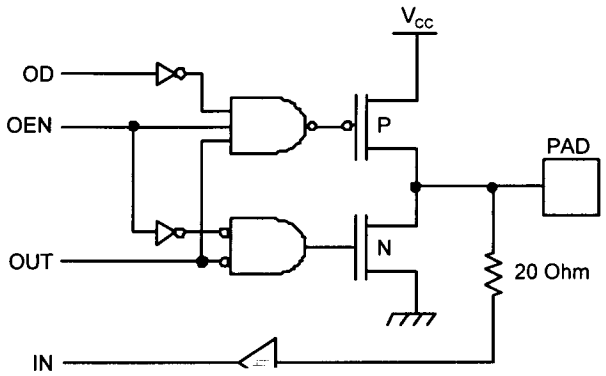


Figure 27. Input/Output, Tristate, Open-Drain

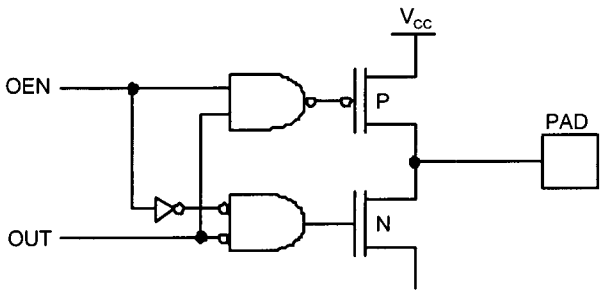


Figure 28. Output Only, Tristate