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Z90255 ROM and Z90251 OTP

32 KB Television Controller with OSD

Product Specification

PS001301-0800

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Z90255 ROM and Z90251 OTP 32 KB TV Controller with On-Screen Display

1 Overview

The Z90255 and Z90251 are the ROM and OTP versions of a Television Controller with On-Screen Display (OSD) that contains 32 KB of program memory.

- The **Z90251** is the one-time programmable (OTP) controller used to develop code or prototypes for specific television applications or initial limited production. Program ROM and Character Generation ROM (CGROM) in the Z90251 are both programmable.
- The **Z90255** incorporates the ROM code developed by the customer with the Z90251. Customer code is masked into both program ROM and CGROM.

An application-specific controller designed to provide complete audio and video control of television receivers and video recorders, the Z90255 provides advanced OSD features. Figure 1 illustrates a typical TV system application using the Z90255. Figure 2 is a block diagram of the Z90255 architecture.

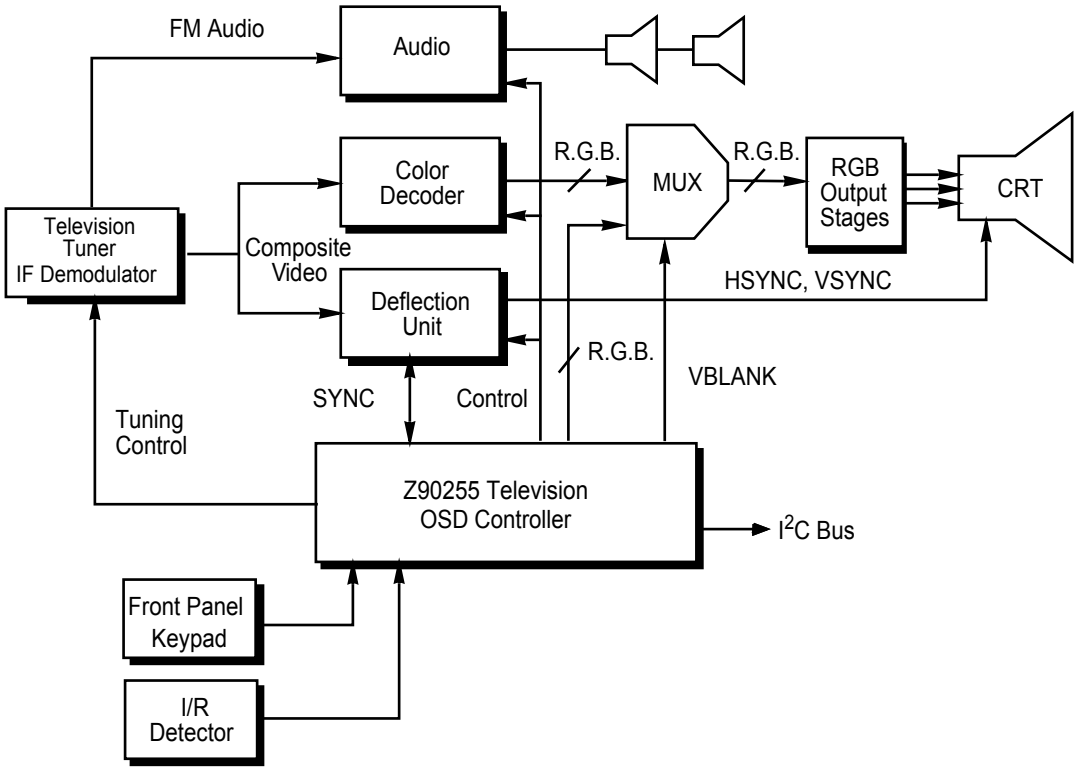

Figure 1 Z90255-Based TV System Application

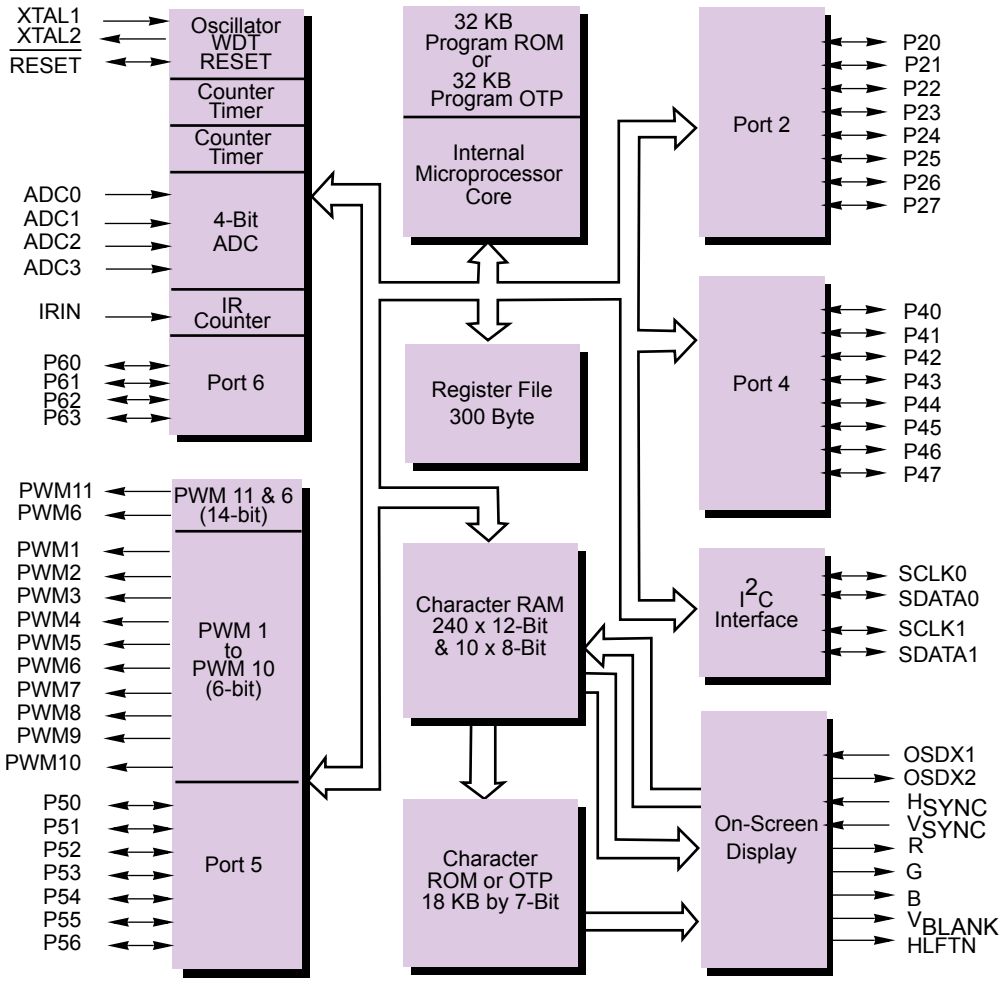

Figure 2 Z90255 Block Diagram

Note: PWM 6 can be either a 6-bit or 14-bit output.

The Z90255 takes full advantage of Zilog's Z8 expanded register file space to offer greater flexibility in creating a user-friendly On-Screen Display (OSD).

Three basic addressing spaces are available: Program memory, Video RAM (VRAM) and the Register file. The register file is composed of 300 bytes of general-purpose registers, 16 control and status registers, one I/O port register and three reserved registers.

The OSD module supports 10 rows by 24 columns of characters. Each character color can be specified. There are eight foreground colors and eight background colors. When the foreground and background colors are the same, the background is transparent.

If Row, Second color and Character set are defined, an analog bar line can be displayed for volume control, signal levels, and tuning.

The OSD can display four character sizes:

- 1X (14 x 18 pixels)
- 2X (28 x 36 pixels)
- Double width (28 x 18 pixels)
- Double height (14 x36 pixels)

Inter-row spacing can be programmed within 0 to 15 Horizontal scan lines. Using multiple characters with zero inter-row spacing allows the creation of large psuedo icons.

A 14-bit Pulse Width Modulator (PWM) port provides necessary voltage resolution for a voltage synthesizer tuning system. Ten 6-bit PWM ports are used to control audio (base, treble, balance and volume) and video (contrast, brightness, color, tint and sharpness) signal levels.

There are 27 I/O pins grouped into four ports. These I/O pins can be configured through software to provide timing, status signals, serial and parallel input and output.

For real-time events, such as counting, timing and data communication, two on-chip counter/timers are implemented. The Z90255 is packaged in a 42-pin SDIP and provides an ideal, reliable solution for high-volume consumer television applications.

1.1 Pin Assignment and Descriptions

Figure 3 shows the pin numbers for production and OTP device format.

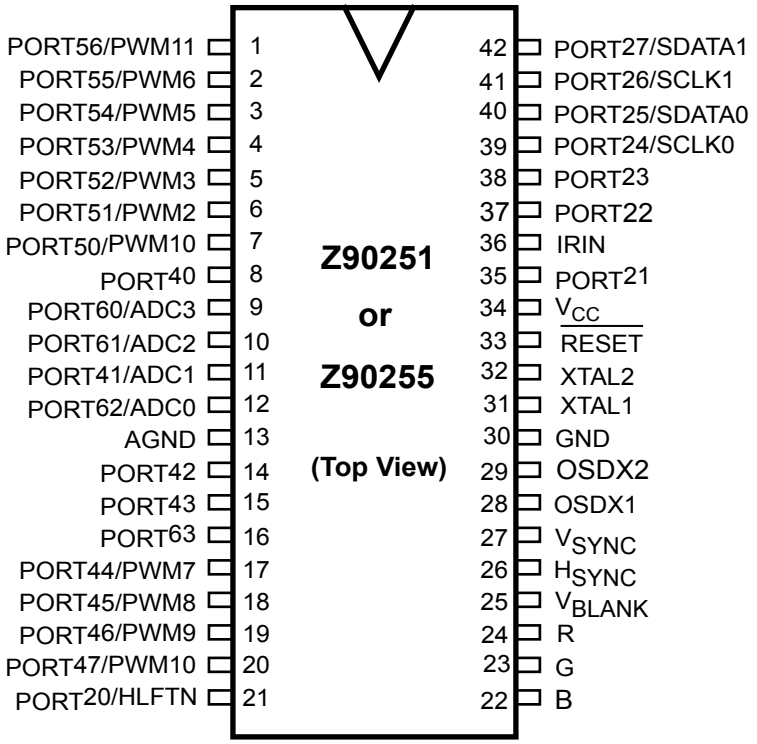

Figure 3 Z90255 and Z90251 Pin Assignments

Notes: 1 The pins on the Z90255 and Z90251 are assigned to perform the functions identified in Tables 1, 2 and 3.

2 PWM 6 can be either 6-bit or 14-bit PWM outputs.

3 All signals with an overbar are active Low.

Table 1 Z90255 Production Device Pin Assignment

Name	Pin Function	Package 42-Pin SDIP	Direction	POR
V_{CC}	+5 Volts	34	Power	Power
GND, AGND	0 Volts	30, 13	Power	Power
IRIN	Infrared Remote Capture Input	36	I	I
PWM11	14-bit Pulse Width Modulator Output	1	O	N/A
PWM10-PWM1[1]	6-Bit Pulse Width Modulator Output	20, 19, 18, 17, 2, 3, 4, 5, 6, 7	O	N/A
P5 (6-0)	Bit Programmable I/O Ports	1, 2, 3, 4, 5, 6, 7	I/O	I
P2 (7-0)	Bit-Programmable I/O Ports	42, 41, 40, 39, 38, 37, 35, 21	I/O	I
HLFTN	Halftone Output	21	O	N/A
SDATA0, SDATA1	I^2C Data, Bidirectional (Send/Receive) Serial Data Lines	40, 42[2]	I/O	N/A
SCLK0, SCLK1	I^2C Clock	39, 41[2]	I/O	N/A
P6 (3-0)	Bit-Programmable I/O Ports	16, 12, 10, 9	I/O	I
P4 (7-0)	Bit-Programmable I/O Ports	20, 19, 18, 17, 15, 14, 11, 8	I/O	I
XTAL1	Crystal Oscillator Input	31	I	I
XTAL2	Crystal Oscillator Output	32	O	O
OSDX1	Dot-Clock Oscillator Input	28	I	I
OSDX2	Dot-Clock Oscillator Output	29	O	O
H_{SYNC}	Horizontal Synchronization	26	I	I
V_{SYNC}	Vertical Synchronization	27	I	I
VBLANK	Video Blanking	25	O	O
R,G,B	Video Red, Green, Blue	24, 23, 22	O	O
ADC3-ADC0	4-Bit Analog-to-Digital Converter Input	9, 10, 11, 12	AI	I
$\overline{\text{RESET}}$	System Reset	33	I/O	I

Note: 1 PWM 6 can be either 6-bit or 14-bit PWM outputs.

2 When Pins 39-42 are configured for I^2C, pins 39 and 40 comprise one channel, and pins 41 and 42 comprise another channel

1.2 Single-Purpose Pin Descriptions

Table 2 lists the single-purpose pin acronyms, pin names, and descriptions.

Table 2 Single-Purpose Pin Descriptions

Acronym	Pin Name(s)	Description
AGND	Analog Ground	Analog Ground
B	Blue	CMOS output of the blue video signal B. Video blue can be programmed for either polarity.
G	Green	CMOS output of the green video signal G. Video green can be programmed for either polarity.
GND	Ground	Ground
H_{SYNC}	Horizontal Sync	Input pin for external horizontal synchronization signal
IRIN	IR Capture Input	Infrared Remote capture input
OSDX1, OSDX2	On-Screen Display Dot Clock Oscillators	These oscillator input and output pins for on-screen display circuits are connected to an inductor and two capacitors to generate the character dot clock. The dot clock frequency determines the character pixel width and phase synchronized to HSYNC
P21, P22, P23	Port 2 bits 1 - 3	Bidirectional digital port, configured to read digital data or to send output to an attached device.
P40, P42, P43	Port 4 bit 0, bits 2 and 3	Bidirectional digital port, configured to read digital data or to send output to an attached device.
P63	Port 6 bit 3	P63 input can be read directly at 03H. A negative edge event is latched to IRQ3. An IRQ3-vectored interrupt occurs if appropriately enabled. A typical application places the device in Stop mode when P63 goes Low (IRQ3 interrupt routine). When P63 subsequently goes High, a Stop-Mode Recovery is initiated.
R	Red	CMOS output of the red video signal R. Video red can be programmed for either polarity.
$\overline{\text{RESET}}$	System Reset	System reset

Table 2 Single-Purpose Pin Descriptions (Continued)

Acronym	Pin Name(s)	Description
V_{BLANK}	Video Blank	CMOS output, programmable polarity. This pin is used as a super-impose control port to display characters from video RAM. The signal controls Y-signal output of CRTs and turns off the incoming video display while the characters in video RAM are super-imposed on the screen. The output ports of color data directly drive three electron guns on the CRT; at the same time VBLANK output turns off the Y signal.
V_{CC}	Power Supply	Power supply
V_{SYNC}	Vertical Sync	Input pin for external vertical synchronization signal.
XTAL1, XTAL2	Time-Based Input Output	These pins connect to the internal parallel-resonant clock crystal oscillator circuit with two capacitors to GND. XTAL1 can be used as an external clock input.

1.3 Multiplexed Pin Descriptions

Table 3 lists the Multiplexed Pin acronyms, pin names, and descriptions.

Table 3 Multiplexed Pin Descriptions

Acronym	Pin Name(s)	Description
P20/HLFTN	Port 2 bit 0 or Halftone Output	Port 2 bit 0 can be programmed as an input or output line.
P24/SCLK0	Port 2 bit 4 or I^2C Clock	Port 2 bit 4 or I^2C Clock
P25/SDATA0	Port 2 bit 5 or I^2C Data	Port 2 bit 5 or I^2C Data
P26/SCLK1 P27/SDATA1	Port 2 bit 6 or I^2C Clock Port 2 bit 7 or I^2C Data	Port 2 bit 6 or I^2C Clock Port 2 bit 7 or I^2C Data
P62/ADC0	Port 6 bit 2 or Analog-to-Digital Converter Channel 0	P62 can be read directly. A negative edge event is latched into IRQ2 to initiate an IRQ2-vectored interrupt if appropriately enabled.
P60/ADC3	Port 6 bit 0 or Analog-to-Digital Converter Channel 3	Port 6 bit 0 can be programmed as an input or output line.

Table 3 Multiplexed Pin Descriptions (Continued)

Acronym	Pin Name(s)	Description
P61/ADC2	Port 6 bit 1 or Analog-to-Digital Converter Channel 2	Port 6 bit 1 can be programmed as an input or output line.
P41/ADC1	Port 4 bit 1 or Analog-to-Digital Converter Channel 1	Port 4 bit1 can be programmed as an input or output line.
P44/PWM7	Port 4 bit 4 or Pulse Width Modulator 7	These port pins can be programmed as input or output ports. Each PWM channel has 6-bit resolution.
P45/PWM8	Port 4 bit 5 or Pulse Width Modulator 8	
P46/PWM9	Port 4 bit 6 or Pulse Width Modulator 9	
P47/PWM10	Port 4 bit 7 or Pulse Width Modulator 10	
PWM11/P56	Pulse Width Modulator 11 or Port 5 bit 6	The PWM signal-generator channel has 14-bit resolution. Port 5 bit 6 and port 5 bit 5 can be programmed as inputs or outputs.
PWM6/P55	Pulse Width Modulator 6 or Port 5 bit 5	
PWM6/P55	Pulse Width Modulator 6 or Port 5 bit 5	These port pins can be programmed as input or output ports. Each PWM signal-generator channel has 6-bit resolution.
PWM5/P54	Pulse Width Modulator 5 or Port 5 bit 4	
PWM4/P53	Pulse Width Modulator 4 or Port 5 bit 3	
PWM3/P52	Pulse Width Modulator 3 or Port 5 bit 2	
PWM2/P51	Pulse Width Modulator 2 or Port 5 bit 1	The PWM signal-generator channel has 6-bit resolution. Port 5 bit 1 and Port 5 bit 0 can be programmed as an input or output port.
PWM1/P50	Pulse Width Modulator 1 or Port 5 bit 0	The PWM signal-generator channel has 6-bit resolution. Port 5 bit 0 can be programmed as an input or output port.

Note: PWM6 can be either 6-bit or 14-bit output.

The Z90251 requires Zilog's Z90259ZEM Emulator with its proprietary Zilog Developmental Studio (ZDS) software for programming. To view how code is working, the emulator uses a ZOSD board which connects directly to a television screen. Refer to Figure 4.

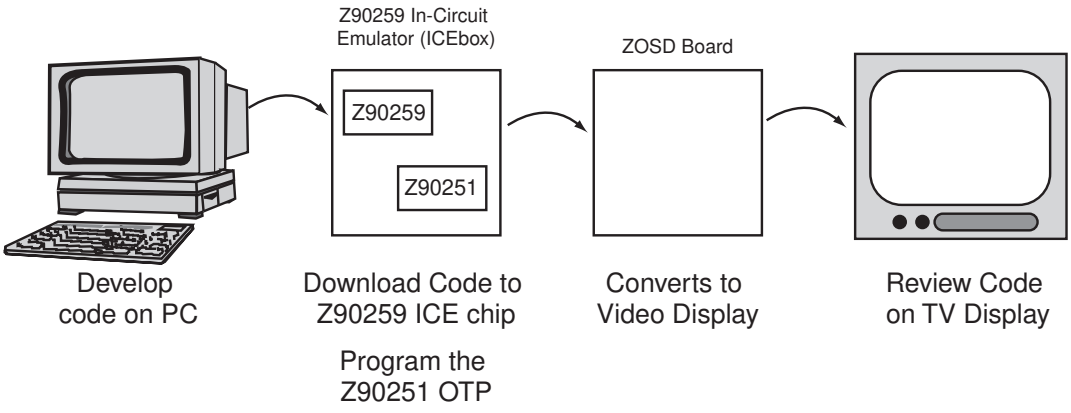

Figure 4 Code Development Environment

2 Memory Description

A total of 300 bytes of general purpose register memory is implemented in the Z90255. These registers are composed of 236 registers from the standard register file and 64 registers from the expanded register file.

2.1 Standard Register File

The Z90255 Standard Register File consists of two I/O port registers (02h and 03h), 236 general purpose registers (04h-EFh) and 15 (F1h-FFh) control and status registers. Registers 00h, 01h, and F0h are reserved. Figure 5 is the register file map. Instructions can access registers directly or indirectly with an 8-bit address field. This also allows short 4-bit addressing using the Register Pointer. In the 4-bit mode, the register file is divided into sixteen working register groups. The upper nibble of the Register Pointer (FDh) addresses the starting location of the active working-register group.

Note: Registers E0h-EFh are only accessed through a working-register and indirect addressing mode.

2.2 Expanded Register File

The register file has been expanded to provide additional system control registers, additional general purpose registers, and expanded mapping of peripheral devices and I/O ports in the register address area.

The lower nibble of the Register Pointer (FDh) addresses the Expanded Register File (ERF) Bank. The 0h value in the lower nibble identifies the Standard Register File to be addressed. Any other value from 1h to Fh selects an ERF Bank. When an ERF Bank is selected, register addresses from 00h to 0Fh access the sixteen ERF Bank registers, which in effect replace the first sixteen locations of the Z90255 Standard Register File. Only ERF Bank 4, ERF Bank 5, ERF Bank 6, ERF Bank 7, ERF Bank A, ERF Bank B, ERF Bank C and ERF Bank F are implemented in the Z90255 controller (Table 4).

2.3 Program Memory

The Z90255 has 32KB of program memory. Refer to Figure 6. The first 12 bytes of the program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to interrupt and program control routine addresses which are passed to the specified vector address. The IRQ0 vector is permanently assigned to the IR interrupt request. The IRQ1 vector is permanently assigned to the V_{SYNC} and H_{SYNC} interrupt request. Program memory starts at address 000Ch after being reset.

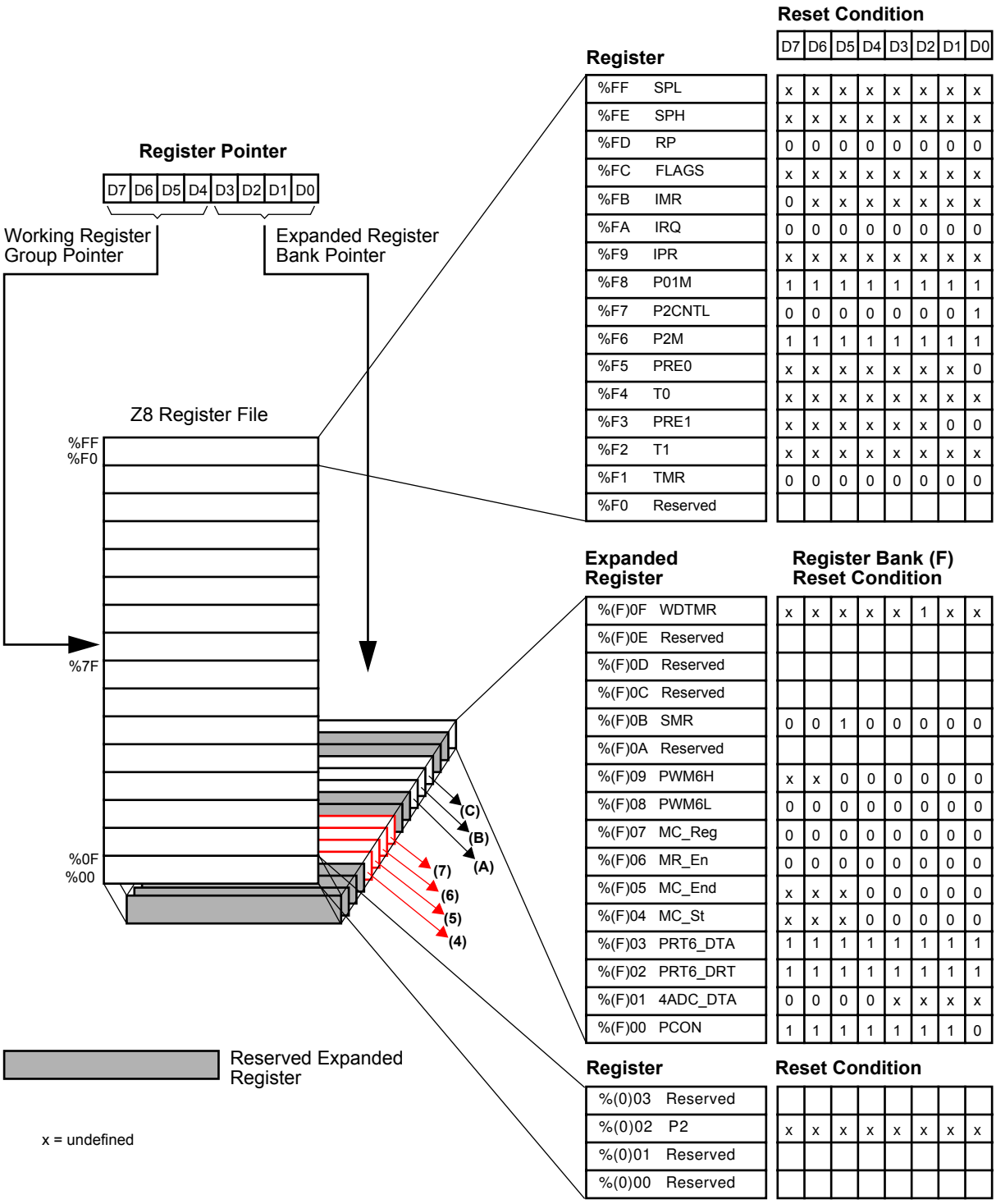

Figure 5 Register File Map

Table 4 Register File Map

BANK 4		BANK 5		BANK 6		BANK 7	
Address	**Description**	**Address**	**Description**	**Address**	**Description**	**Address**	**Description**
00h-0Fh	Gen. Pur. Reg.	00h-0Fh	Gen. Pur. Reg.	00h-0Fh	Gen. Pur. Reg.	00h-0Fh	Gen. Pur. Reg.

BANK A		BANK B	
Address	**Description**	**Address**	**Description**
00h	OSD Control Register(OSD_CNTL)	00h	PWM11-High Data Register(PWM11H)
01h	Vertical Position Register(VERT_POS)	01h	PWM11-Low Data Register(PWM11L)
02h	Horizontal Position Register(HOR_POS)	02h	PWM1 Data Register(PWM1)
03h	Display Attribute Register(DISP_ATTR)	03h	PWM2 Data Register(PWM2)
04h	Row Space Register (ROW_SPACE)	04h	PWM3 Data Register(PWM3)
05h	Fade Position1 Register(FADE_POS1)	05h	PWM4 Data Register(PWM4)
06h	Fade Position2 Regisiter(FADE_POS2)	06h	PWM5 Data Register(PWM5)
07h	Second Color Control Register(SNDCLR_CNTRL)	07h	PWM6(6-bit) Data Register(PWM6_6)
08h	Second Color Position Register(SNDCLR_POS)	08h	PWM7 Data Register(PWM7)
09h	Color Palette0 Register(CLR_P0)	09h	PWM8 Data Register(PWM8)
0Ah	Color Palette1 Register(CLR_P1)	0Ah	PWM9 Data Register(PWM9)
0Bh	Color Palette2 Register(CLR_P2)	0Bh	PWM10 Data Register(PWM10)
0Ch	Color Palette3 Register(CLR_P3)	0Ch	Port 5 Data Register(PRT5_DTA)
0Dh	Color Palette4 Register(CLR_P4)	0Dh	PWM Mode Register(P_MODE)
0Eh	Color Palette5 Register(CLR_P5)	0Eh	Port 5 Direction Register(PRT5_DRT)
0Fh	Color Palette6 Register(CLR_P6)	0Fh	

BANK C		BANK F	
Address	**Description**	**Address**	**Description**
00h	3-bit ADC Data Register(3ADC_DTA)	00h	Port Configuration Register(PCON)
01h	Timer Control Register0(TCR0)	01h	4-bit ADC Data Register (4ADC_DTA)
02h	Timer Control Register1(TCR1)	02h	Port6 Direction Register(PRT6_DRT)
03h	IR Capture Register0(IR_CP0)	03h	Port6 Data Register (PRT6_DTA)
04h	IR Capture Register1(IR_CP1)	04h	Mesh Column Start Register(MC_ST)
05h	Port4 Data Register(PRT4_DTA)	05h	Mesh Column End Register(MC_END)
06h	Port4 Direction Register(PRT4_DRT)	06h	Mesh Row Enable Register(MR_EN)
07h	Interrupt Status Register(INT_ST)	07h	Mesh Control Register(MC_REG)
08h	Port4 Pin_out Selection Register(PIN_SLT)	08h	PWM6 High Data Register(PWM6H_14)
09h	Color Index Register(CLR_IDX)	09h	PWM6 Low Data Register (PWM6L_14)
0Ah	I2C Data Register(I^2C_DATA)	0Ah	
0Bh	I2C Command Register(I^2C_CMD)	0Bh	Stop Mode Register(SMR)
0Ch	I2C Control Register(I^2C_CNTL)	0Ch	
0Dh		0Dh	
0Eh		0Eh	
0Fh		0Fh	WDT Mode Register(WDTMR)

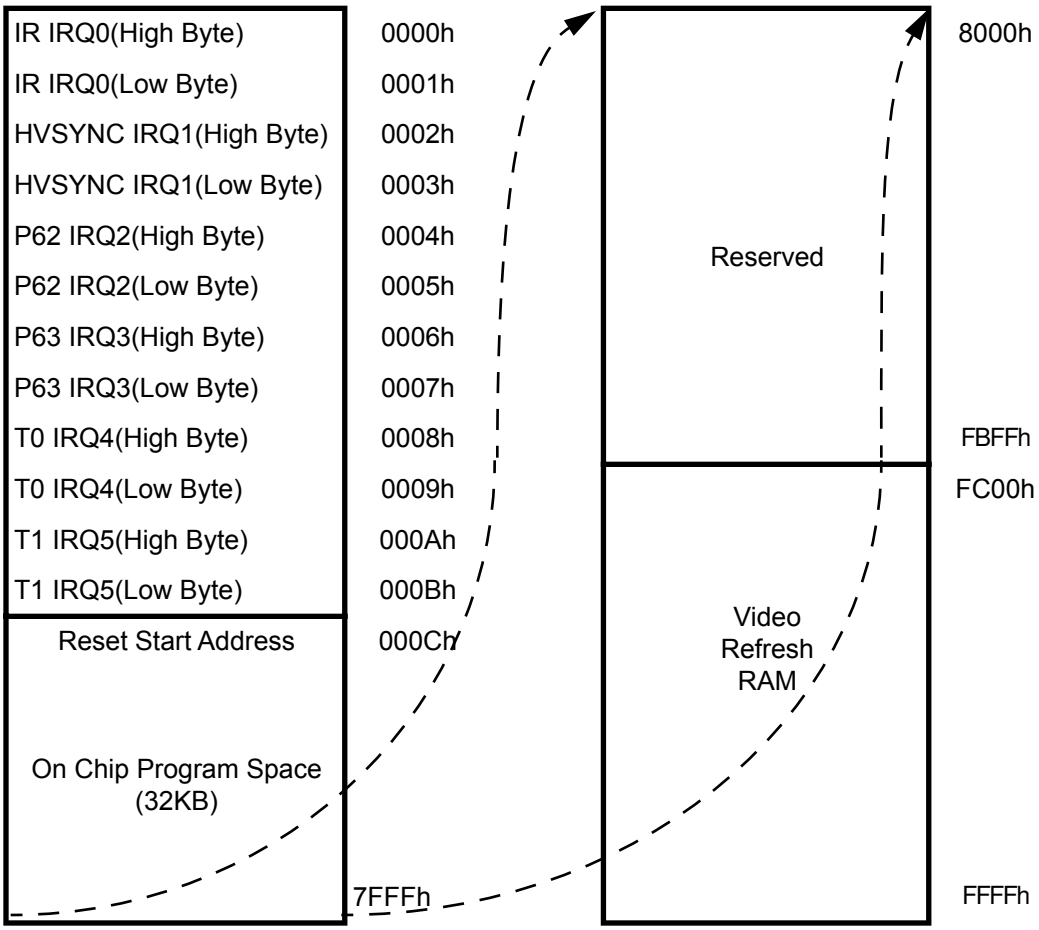

Figure 6 Program Memory Map

3 Watch-Dog Timer (WDT)

The Watch-Dog Timer (WDT) is driven by an internal RC oscillator. Therefore accuracy is dependent on the tolerance of the RC components. Table 5 describes the Watch-Dog Timer Mode register bits.

Table 5 Watch-Dog Timer Mode Register 0Fh: Bank F

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	1	0	1

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
reserved	7-4	W	0	Must be 0
WDT During Stop	3	W	0 1	Off On POR
WDT During Halt	2	W	0 1	Off On POR
WDT TAP	1, 0	W	00 01 10 11	6 msec 12 msec POR 24 msec 96 msec

WDT During Halt Mode (T2)

Bit 2 determines if the WDT is active during Halt Mode. A 1 value indicates active during Halt. The default is 1. A WDT timeout during Halt Mode resets control registers and ports to their default reset conditions.

Bit 3 determines if the WDT is active during Stop mode. A 1 value indicates active during Stop mode. A WDT timeout during Stop mode resets control registers and ports to their default reset conditions.

Bits 4, 5, 6 and 7 are reserved and must be cleared to 0.

The WDTMR register is accessible only during the first 60 processor cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Reset, or a

Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise.

The WDT is permanently enabled after Reset. To ensure that the WDT is set properly, use the following instructions as the first two instructions:

```
DI
WDT
```

The Watch-Dog timer must then be constantly refreshed within the required timeout by executing the WDT Instruction.

Note: Executing the WDT instruction affects the Z (zero), S (sign), and V (overflow) flags.

A system reset overrides all other operating conditions and puts the microcontroller into a known state. To initialize the chip's internal logic, the Reset input must be held Low for at least 5 XTAL clock cycles. The control registers and ports are reset to default conditions after a POR, a reset from the Reset pin, or a WDT timeout while in Run Mode and Halt Mode. The control registers and ports are not reset to their default conditions after Stop Mode Recovery and WDT timeout while in Stop Mode.

The program counter is loaded with 000Ch. I/O ports and control registers are configured to their default reset states.

Resetting the microcontroller does not Affect the contents of the general-purpose registers.

The Watch-Dog Timer (WDT) is a retriggerable, one-shot timer that resets the microcontroller if it reaches its terminal count. When operating in the Run, Halt or Stop Modes, a WDT reset is functionally equivalent to a hardware POR reset.

4 Stop Mode and Halt Mode Operation

4.1 Power-Down Halt-Mode Operation

The Halt Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the counter/timer(s) and interrupt logic.

To enter the Halt Mode, the instruction pipeline must be flushed first to avoid suspending execution in mid-instruction. To do this, the application program must

execute a NOP instruction (opcode = FFh) immediately before the Halt instruction (opcode 7Fh), that is,

```
FF      NOP     ;clear the instruction pipeline
7F      Halt    ;enter Halt Mode
```

The Halt Mode is exited by interrupts, generated either externally or internally. When the interrupt service routine is completed, the user program continues from the instruction after Halt.

The Halt Mode can also be exited via a POR/Reset activation or a Watch-Dog Timer (WDT) timeout. In this case, program execution restarts at the reset-restart address 000Ch.

To reduce power consumption further in the Halt Mode, the Z90255 and Z90251 allow dynamic internal clock scaling. Clock scaling can be accomplished on the fly by reprogramming bit 0 and/or bit 1 of the Stop-Mode Recovery register (SMR).

Note: Internal clock scaling directly effects Counter/Timer operation: adjustment of the prescaler and downcounter values might be required.

4.2 Stop Mode Operation

The Stop Mode provides the lowest possible device standby current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the Stop Mode, the instruction pipeline must be flushed first to avoid suspending execution in mid-instruction. To do this, the application program must execute a NOP instruction (opcode=FFh) immediately before the Stop instruction (opcode=6Fh), that is,

```
FF      NOP     ;clear the instruction pipeline
6F      Stop    ;enter Stop Mode
```

The Stop Mode is exited by any one of the following resets: Power-On Reset activation, WDT timeout, or a Stop-Mode Recovery source. When reset is generated, the processor always restarts the application program at address 000Ch.

POR/Reset activation is present on the Z90255 and Z90251 and is implemented as a reset pin and/or an on-chip power on reset circuit.

When the WDT is configured to run during Stop mode, the WDT timeout generates a Reset ending Stop Mode.