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ZG2100M/ZG2101M Wi-Fi® Module Data Sheet

2.4 GHz 802.11b Low Power Transceiver Module

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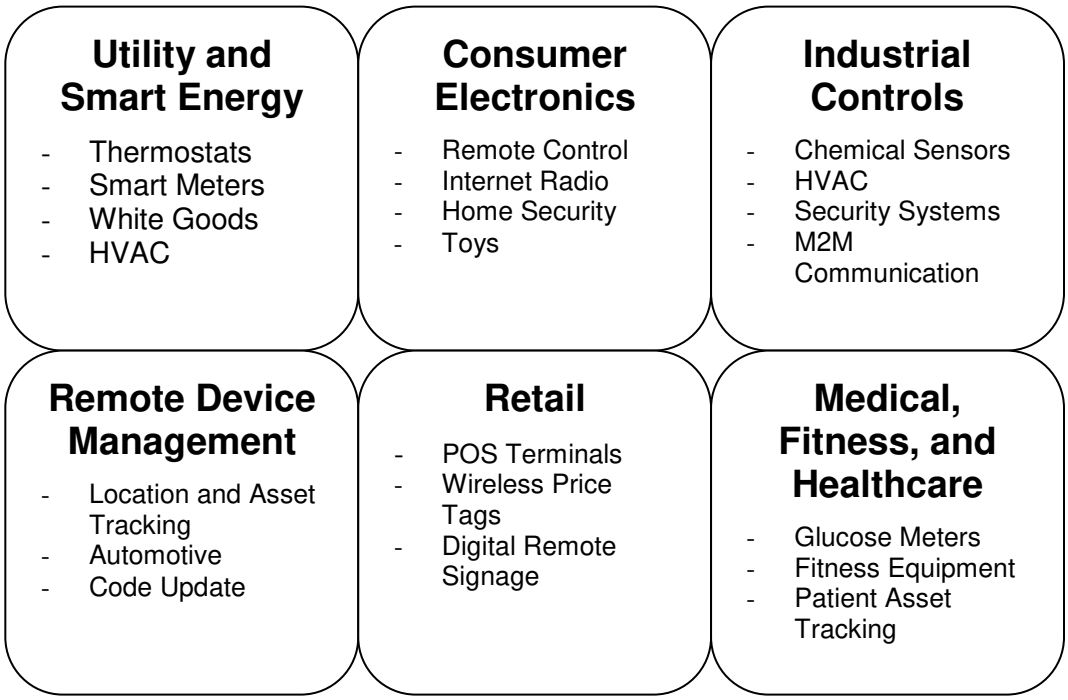
2.4 GHz 802.11b Low Power Transceiver Module



Features

- Single-chip 802.11b including MAC, baseband, RF and power amplifier
- Data Rate: 1 & 2 Mbps
- 802.11b/g/n compatible
- Low power operation
- API for embedded markets, no OS required
- PCB or external antenna options
- Hardware support for AES and RC4 based ciphers (WEP, WPA, WPA2 security)
- SPI slave interface with interrupt
- Single 3.3V supply, operates from 2.7V to 3.6V (see section 5)
- 21mm x 31mm 36-pin Dual Flat pack PCB SM Package
- Wi-Fi Certified, RoHS and CE compliant
- FCC Certified (USA, FCC ID: W7O-ZG2100-ZG2101)
- IC Certified (IC: 8248A-G21ZEROG)
- Fully compliant with EU & meets the R&TTE Directive for Radio Spectrum
- Radio Type Approval Certified (Japan, ZG2100M based solution ID: AC164136-2 – 005WWCA0311 005GZCA0149)

Description

The ZG2100M & ZG2101M modules are low-power 802.11b implementations. All RF components, the baseband and the entirety of the 802.11 MAC reside on-module, creating a simple and cost-effective means to add Wi-Fi connectivity for embedded devices. The module(s) implement a high-level API, simplifying design implementation and allowing the ZG2100M or ZG2101M to be integrated with 8- and 16-bit host microcontrollers. Hardware accelerators support the latest Wi-Fi security standards.

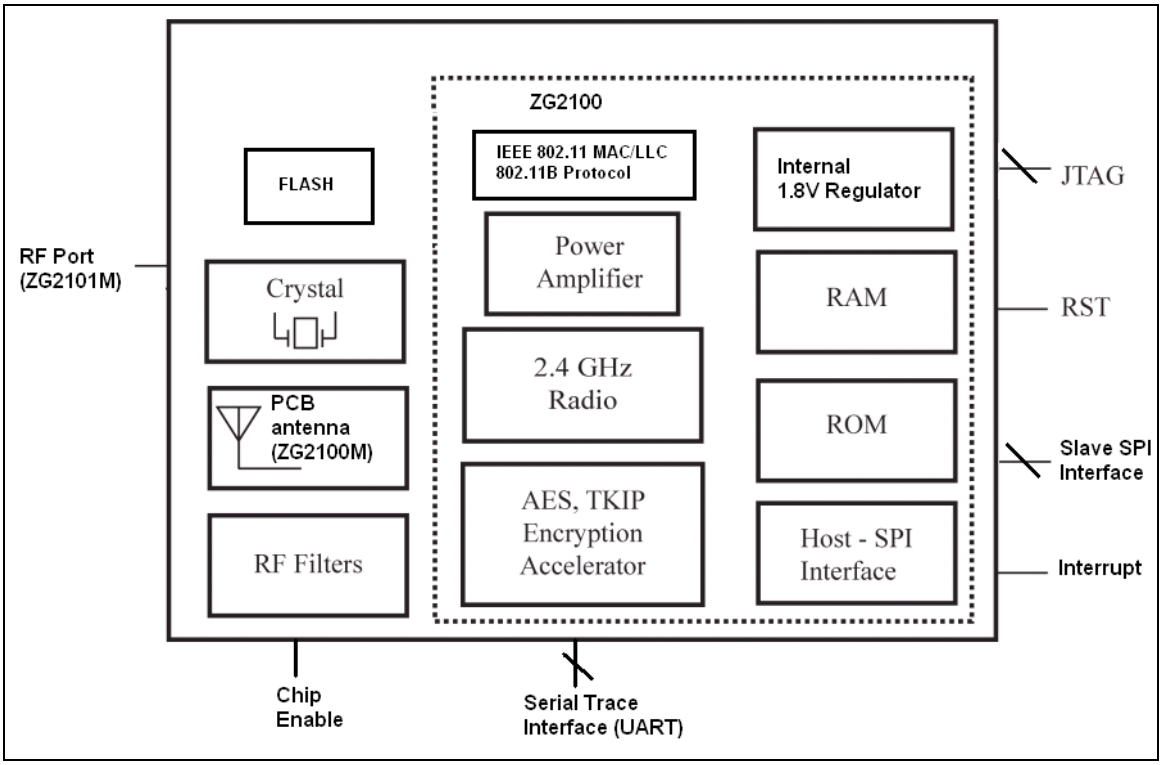


Figure 1: ZG2100M/ZG2101M Module: Functional Block Diagram

Table of Contents

1 Key Features

Ease of Software Development

- Simple API suited for embedded market
- Targeted for low resource host processors
- Entire MAC integrated on-chip
- Serialized MAC address, each device comes with an unique MAC address in range 001EC0xxxxxx
- Simple usage model, no requirement for OS

Low Power Operation

- Low power, 250uA sleep mode with fast wake up, 0.1uA hibernate,
- Sleep power state managed by ZG2100, enabling low average power while maintaining AP association without host control
- Battery operable from 2.7v to 3.6v (see power specs for limitations)

RF

- Integrated PA
- Support for external PA for high RF output power applications
- Power output +10dBm typical at antenna
- Power output programmable from +0dBm to meet varying application needs
- Min RX sens.of-91dBm @ 1MB/Sec. at antenna
- Integrated PCB antenna (ZG2100M)
- Support for external antenna available (ZG2101M)

Low External Component Count

- Fully integrated RF frequency synthesizer, reference clock, and Integrated PA
- Single 3.3V supply

Wi-Fi & Regulatory

- Supports 1Mbps & 2Mbps and module-based solutions are “Wi-Fi certified” for 802.11b
- Hardware support for AES, and RC4 based ciphers (WEP, WPA, WPA2 security)
- FCC Certified (USA, FCC ID: W7O-ZG2100-ZG2101), IC Certified (IC: 8248A-G21ZEROG), Radio Type Approval Certified (Japan, ZG2100M based solution ID: AC164136-2 – 005WWCA0311 005GZCA0149, Wi-Fi Certified, RoHS and CE compliant, and fully compliant with European Market and meet the R&TTE Directive for Radio Spectrum

2. Detailed Description

2.1 Overview

The ZG2100 single-chip 802.11b transceiver includes MAC, baseband, RF and power amplifier, and built in hardware support for AES, and TKIP (WEP, WPA, WPA2 security). The device has an API targeted for embedded markets so an operating system is not required for operation. There is a fully integrated radio ideal for 1 & 2Mbps operation with optional support for external PA and antenna switch operation.

The ZG2100M modules incorporate the ZeroG ZG2100 single chip 802.11b transceiver with all associated RF components, crystal oscillator, and bypass and bias passives along with a printed antenna to provide a fully integrated Wi-Fi I/O solution controllable from an 8 or 16-bit processor. The ZG2101M module is similar but bypasses the on-board PCB antenna and uses a U.FL connector for connection to an external antenna.

Interface is via SPI slave interface with interrupt for HOST operation. The modules support RS232 serial interfaces (requires level shifter) for debug and JTAG boundary scan. Operation is via a single 3.3V supply, supporting various power states, such as hibernate and SLEEP, for end applications long battery life. ZG2100M contains a built in PCB antenna for ease of system integration and significant BOM reduction.

The module is manufactured on an FR4 PCB substrate, with components on the top surface only. Connection is made as a surface mount component via flat pack (no pin) connections on two sides.

2.2 Supply Blocks and Boot-Up Sequence for Single 3.3V Supply

The internal regulators for the digital and analog core power supplies are enabled by keeping the chip enable pin (CE_N) low. The waveforms for the core supplies, illustrated on the following page, as shown when powering up the ZG2100M/ZG2101M with a nominal 3.3V applied to VDD_3.3. There is an internal power-on-reset detect which starts the boot sequence from the internal ROM when the core supply (VDD_1.8) is up. After approximately 50 ms from when VDD_3.3 supply is within specification, the ZG2100M/ZG2101M is ready for operation.

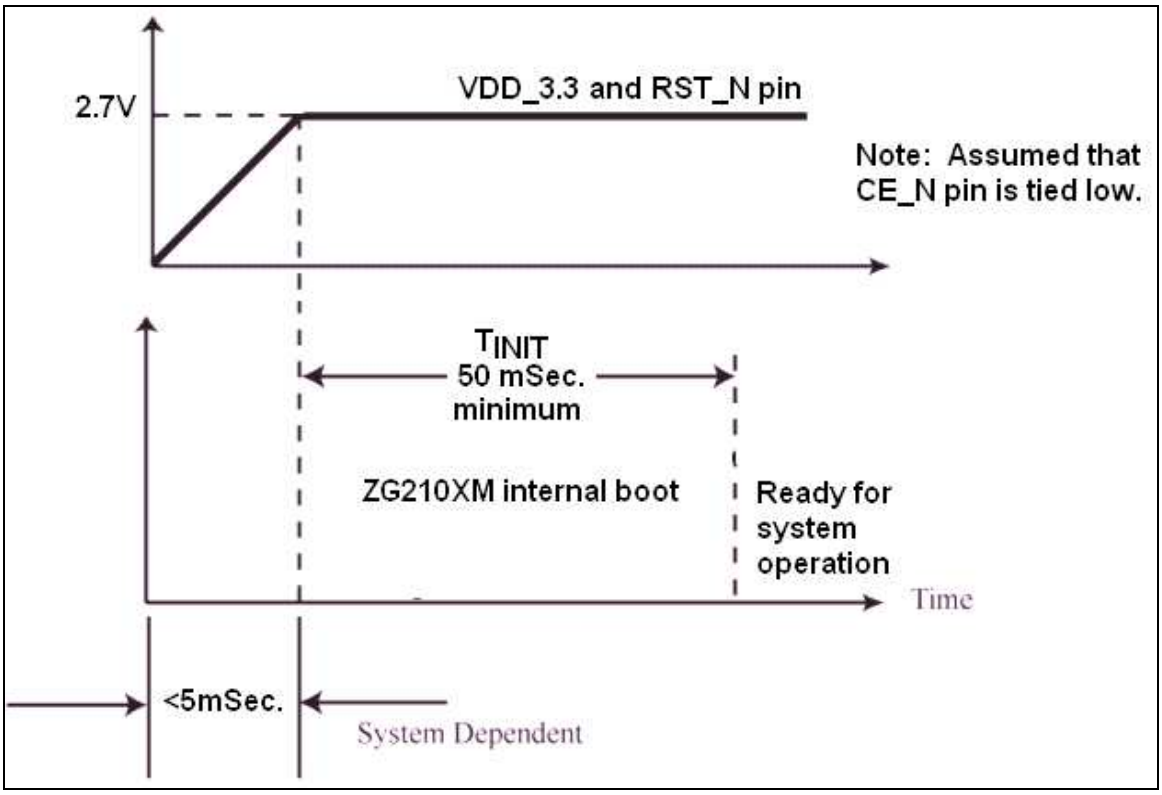


Figure 2: ZG2100M/ZG2101M Boot Sequence Timing.
Refer to Section 4.1 Electrical Characteristics, Note 1.

2.3 ZG2100 Power States

The power state definitions are as follows:

	VDD_3.3	CE_N	Circuitry
OFF	0V	0V	Power disconnected to ZG2100
HIBERNATE	3.3V	3.3V	All internal circuitries are OFF
SLEEP	3.3V	0V	Reference clock and internal bias circuitry are ON
RX ON	3.3V	0V	Receive circuits are ON
TX ON	3.3V	0V	Transmit circuits are ON
STANDBY			Transition State Only

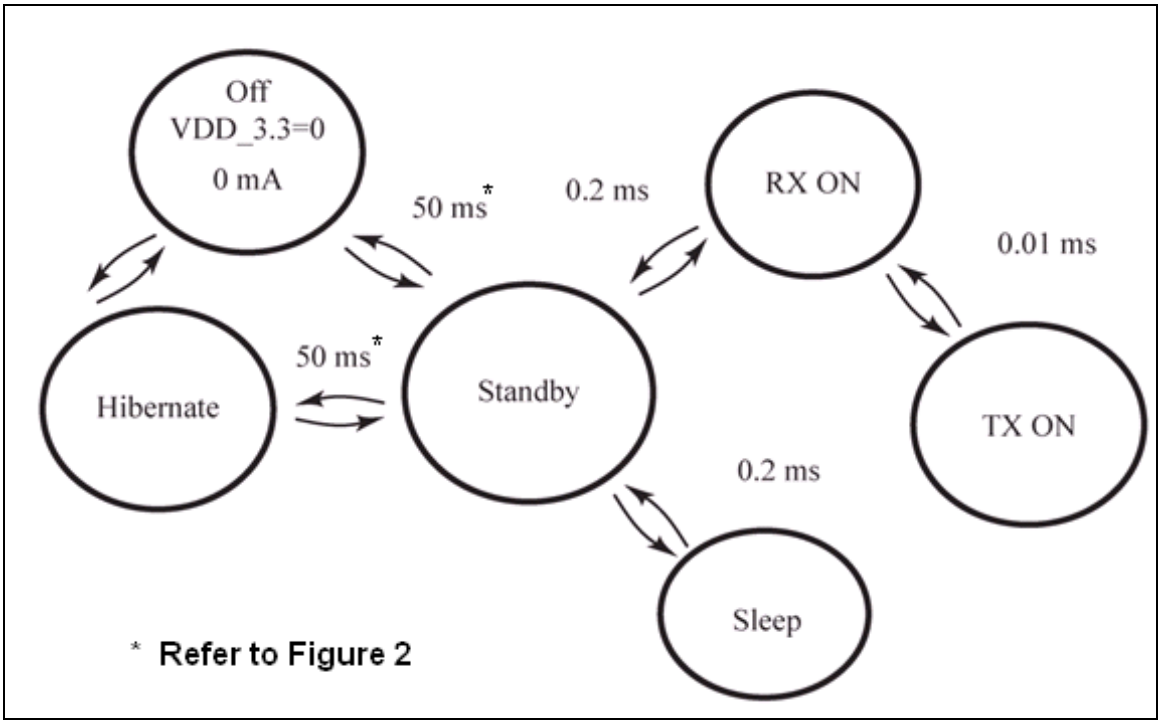


Figure 3: ZG2100M/ZG2101M Power State Diagram

2.4 Electrostatic discharge (ESD)

The ZG2100 IC, integrated within the ZG2100M/ZG2101M, has passed ESD HBM JEDEC Standard No. 22-A114 / 2000 Volts and ESD CDM JEDEC Standard No. 22-C101 / 500V all pins. Users must exercise ESD handling precautions when working with the product either in component form, or exposed PCBs.

2.5 JTAG Interface

Joint Test Action Group (JTAG) is the common name used for the IEEE 1149.1 standard entitled Standard Test Access Port and Boundary-Scan Architecture for test access ports used for testing printed circuit boards using boundary scan. ZG2100M/ZG2101M supports JTAG boundary scan. JTAG_EN and JTAG_RST_N need to be driven HIGH to enable JTAG mode.

2.6 Serial Interface for Trace

ZG2100M/ZG2101M incorporates Transmitted Data pin (UART0_TX) and Received Data pin (UART0_RX) for serial testing purposes. These pins can be connected to commercially available RS-232 line drivers/ receivers with appropriate external level shifters. The ZG2100 serial interface is fully tested at 115200 bits/seconds baud rate with RS232/UART interface applications.

2.7 SPI Interface

2.7.1 SPI Slave Interface with Interrupt for Host Operation

The slave Serial Peripheral Interface Bus (SPI) is used to interface with the HOST. The slave SPI interface works with ZG2100M/ZG2101M Interrupt line (INT_NX). When data is available for the HOST during operation, the INT_NX line is asserted low by ZG2100. The INT_NX line is de-asserted high, by ZG2100M/ZG2101M, after the data is transferred to the HOST SPI buffer. The SPI CLK Speed can be up to 25MHz.

2.7.2 Host-Control SPI Interface

The slave SPI interface implements the [CPOL=0; CPHA=0] and [CPOL=0; CPHA=1] modes (0 and 3) of operation. That is, data is clocked in on the first rising edge of the clock after Chip Select goes valid.

Data on the bus is required to be big endian, with most significant bit on the bus first and least significant bit going last. There are two decode regions. One for register access and one for a FIFO interface. Operation for both regions is shown below. The INT_NX signal allows interrupts to be signaled to the host device.

As an example of any 32-bit register access, suppose a write to register 0xF0_0F18 is desired:

Write to host register 0x38 with addr[31:16] (0x00f0). 24 bit transaction.
Write to host register 0x39 with addr[15:0] (0x0F18). 24 bit transaction.
Write to host register 0x3a with data[31:16]. 24 bit transaction.
Write to host register 0x3b with data[15:0]. 24 bit transaction.
Write to host register 0x37 with a byte that has the following pattern: 8 bit transaction
[7:4] byte enables (active high for the valid bytes that you want to write in steps 3 and 4).
[3:0] - 4'b0001 -> activate write to register

For a read of 0xF0_0D00:

Write to host register 0x38 with addr[31:16] (0x00F0). 24 bit transaction.
Write to host register 0x39 with addr[15:0] (0x0F18). 24 bit transaction.
Write to host register 0x37 with a byte that has the following pattern: 8 bit transaction
[7:4] byte enables (active high for the valid bytes that you want to read in steps 1 and 2).
[3:0] - 4'b0011 -> active read of register
Read host register 0x3a to get data [31:24] 24 bit transaction
Read host register 0x3b to get data [15:0] 24 bit transaction

Each of the steps above is a single SPI transaction; the chip select (CE_N) is active low during each step.

2.7.3 SPI Timing Characteristics

Characteristic	Min	Max
SPI, Data setup to falling clock	1 ns	
SPI, Data hold from falling clock	1 ns	
SPI SLAVE CLK		25 MHz
SPI MASTER CLK		25 MHz

Figure 4: ZG2100M/ZG2101M SPI Timing Characteristics

2.74 SPI Timing

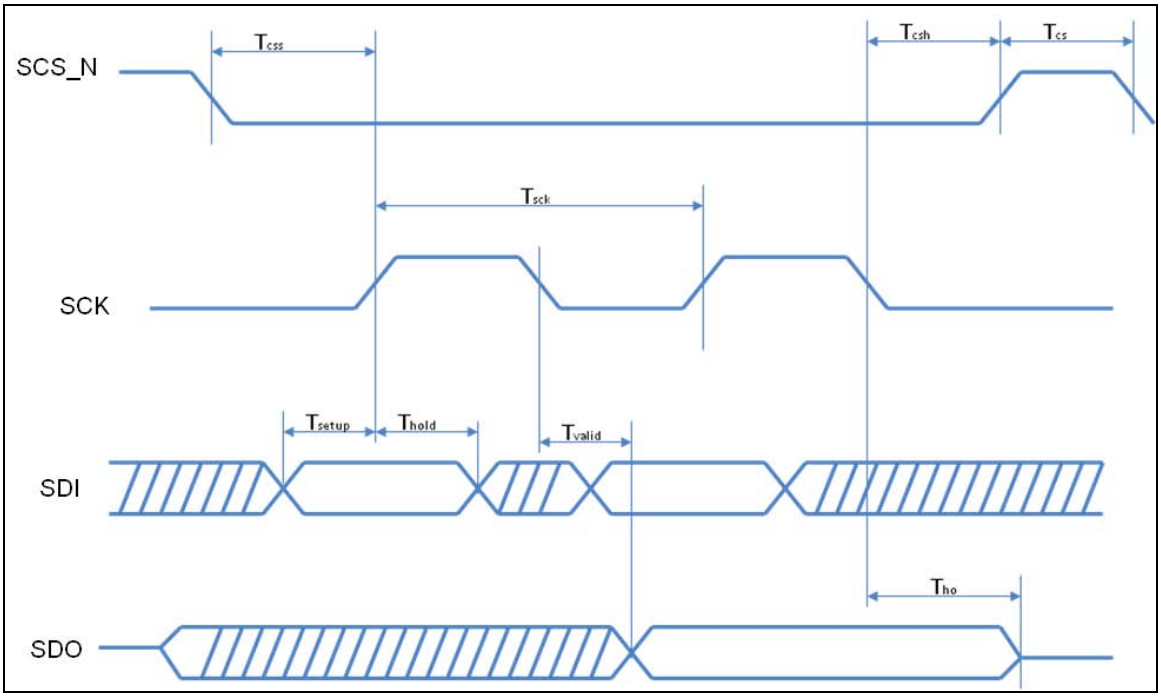


Figure 5: ZG2100M/ZG2101M SPI Timing Waveform

Symbol	Parameter	Min	Typ	Max
Tsck	SCK Clock Period	40 ns		
Tcs	SCS_N High Time	50 ns		
Tcss	SCS_N Setup Time	50 ns		
Tcsh	SCS_N Hold Time	50 ns		
Tsetup	SDI Setup Time	10 ns		
Thold	SDI Hold Time	10 ns		
Tvalid	Output Valid			15 ns
Tho	Output Hold Time	0		15 ns

Figure 6: ZG2100M/ZG2101M SPI Timing Data

2.7.5 SPI Register Access

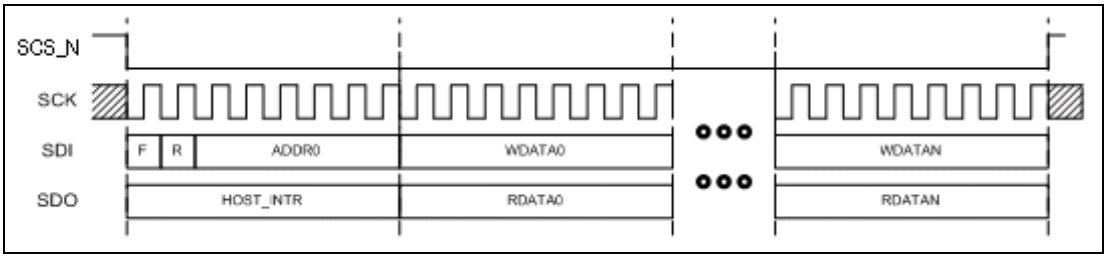


Figure 7: ZG2100M/ZG2101M SPI Register Access

F is a select between FIFO space and register space. If this bit is a 1, the data FIFO space is selected. If this bit is a 0, the register address space is selected.

R is the Read/Write bit. If this bit is a 1, the operation is a read. If this bit is a 0, the operation is a write

ADDR0 is the starting address for the transaction. This value is only used for register accesses and is ignored during FIFO accesses.

WDATAn is the write data byte. This is only used from write operations and is ignored during read operations.

RDATAn is the read data byte. This is always valid for both, read and write operations. If contains the current value of any register location.

HOST_INTR is the 8-bit interrupt register.

2.8 FIFO Interface

HOST FIFO Basic Commands
FCMD[2:0]
- 0x0 – RFIFO_CMD
- 0x1 – WCONT (Continue Previous Packet)
- 0x2 – WSTART0 (Start Packet, head/continue)
- 0x3 – WSTART1 (Start Packet, head0/continue)
- 0x4 – WEND CMD
- 0x5 – REND CMD

2.8.1 FIFO Read

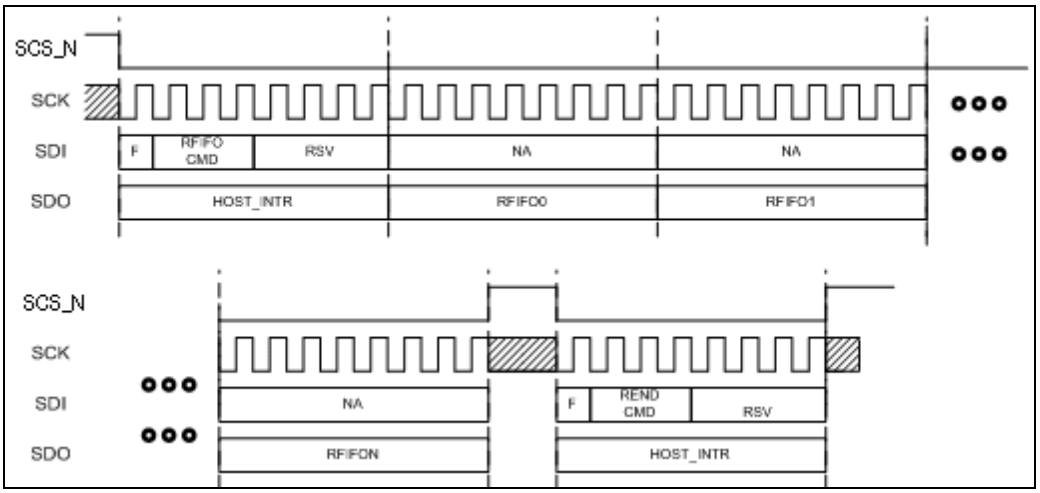


Figure 8: ZG2100M/ZG2101M FIFO Read Timing

2.8.2 FIFO Write

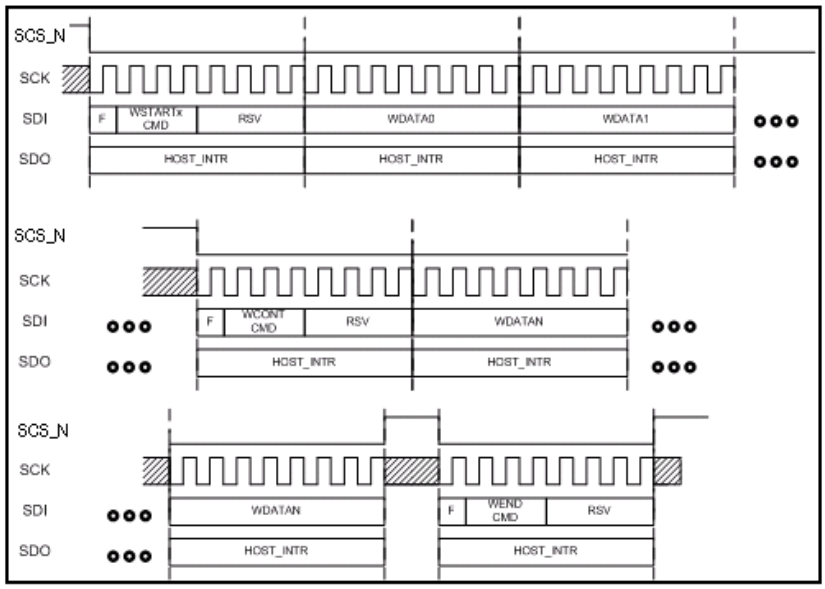


Figure 9: ZG2100M/ZG2101M FIFO Write Timing

2.9 Fully-Integrated Radio

ZG2100M/ZG2101M incorporates a fully integrated radio Ideal for 1 & 2 Mbps operation with optional support for external PA operation. The direct conversion TX design incorporates an integrated PA, with up to +10dBm typical at antenna, and fully integrated internal power control loop. The direct conversion RX chain utilizes Automatic Gain Control that allows ZG2100M/ZG2101M to receive with a minimum input Level sensitivity (1Mbps @ <8% PER) of -91 dBm typical at the antenna. The ZG2100M/ZG2101M only needs an external crystal for a reference clock.

2.10 Internal ROM/RAM/NVM

ZG2100M/ZG2101M incorporates internal ROM, RAM, and NVM. The internal ROM and RAM are reserved only for ZG2100M/ZG2101M operations. The NVM holds information such as the MAC address, TX manufacturing calibration values, and frequency calibration values.

2.11 Hardware Support for AES and TKIP

ZG2100M/ZG2101M supports Wi-Fi encryption methodology (AES and RC4 based ciphers).

3. ZG2100M/ZG2101M Pin-Out and Function

Pins	Name	Internal Bias	Required Bias Resistor	Description
1	GND			Ground
2	VDD_1.8			See below
3	JTAG_TDO	H		JTAG data out
4	JTAG_TCK		Constant drive	JTAG Clock in
5	JTAG_TMS	H		JTAG Mode in
6	JTAG_TDI	H		JTAG data in
7	RST_N		Constant drive	Chip reset in
8	DNC			Do Not Connect
9	JTAG_RST_N		Constant drive	JTAG Reset in, pulling this pin low will keep JTAG idle (reset)
10	GND			Ground
11	VDD_1.8			See below
12	DNC			Do Not Connect
13	DNC			Do Not Connect
14	DNC			Do Not Connect
15	DNC			Do Not Connect
16	RES		Pull-down	FLASH Write Protect. See below.
17	VDD_3.3			3.3V Power
18	GND			Ground
19	GND			Ground
20	CE_N			Chip enable in
21	JTAG_EN	L		JTAG Enable in, this pin needs to be high for Boundary Scan use
22	DNC			Do Not Connect
23	SCS_N		Constant drive	Serial chip select from host (input)
24	VDD_1.8			See below
25	GND			Ground
26	UART_RX	H		Debug Serial in
27	UART_TX			Debug Serial out
28	GND			Ground
29	VDD_3.3			3.3V Power
30	GND			Ground
31	VDD_1.8			See below
32	SDO			Serial data out to host
33	INT_NX		Pull-up	Interrupt to host (output)
34	SCK		Constant drive	Serial clock in from host
35	SDI		Constant drive	Serial data in from host
36	GND			Ground

Notes:

1. VDD_1.8 is an internally used supply rail. **DO NOT USE** these pins to drive other components.
2. Signals that note “Constant drive” must either be constantly driven by the host, or have a pullup or pulldown in case the host is likely to tri-state the signal during power down modes. The constant drive is used to ensure defined operation of the part and to minimize leakage current during low power modes.
3. RES is used as write-protect for the internal module SPI Flash. For production use, this pin should be pulled low. Host control will enable in-field FLASH updates.

4. Package Information

4.1 Module Drawing

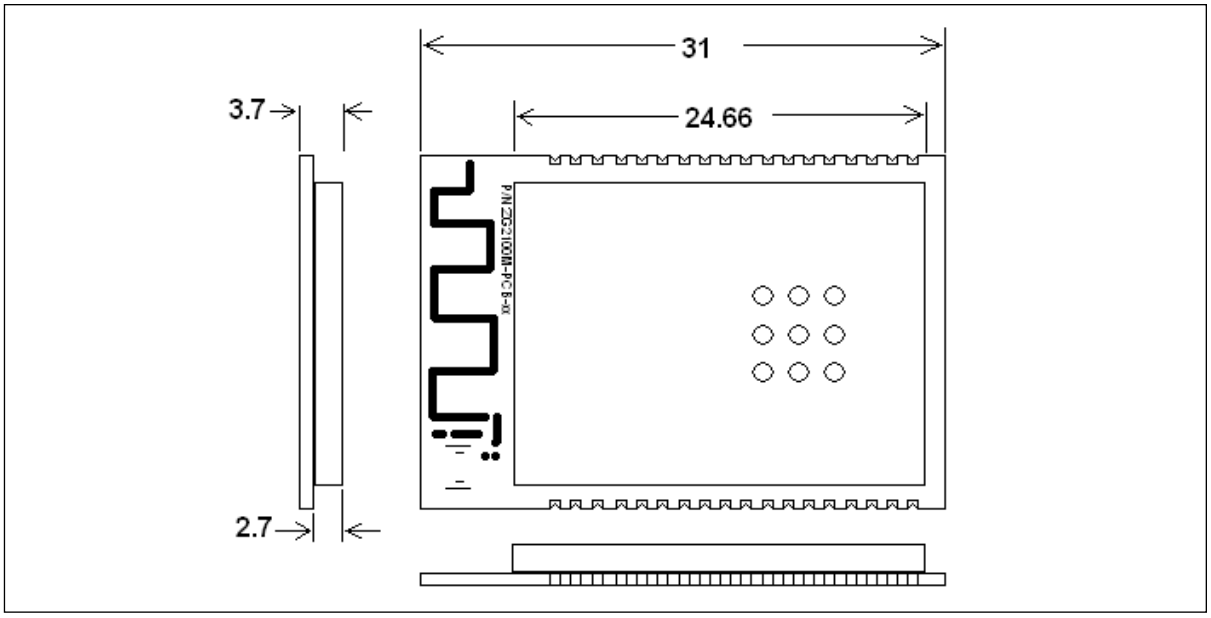


Figure 10: ZG2100M Module Physical Dimensions
All measurements are in millimeters. Tolerances for measures 0-10 mm is +/- 0.05 mm.
Tolerances for measures 10-50 mm is +/- 0.1 mm

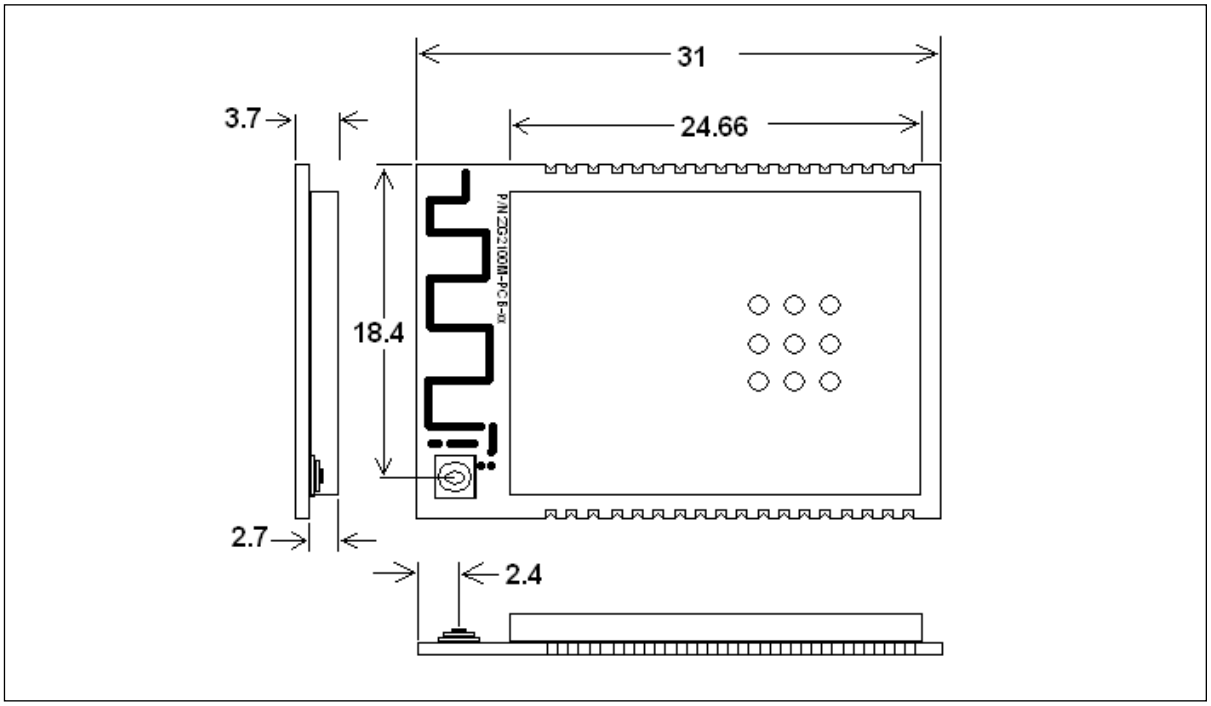


Figure 11: ZG2101M Module Physical Dimensions
All measurements are in millimeters. Tolerances for measures 0-10 mm is +/- 0.05 mm.
Tolerances for measures 10-50 mm is +/- 0.1 mm

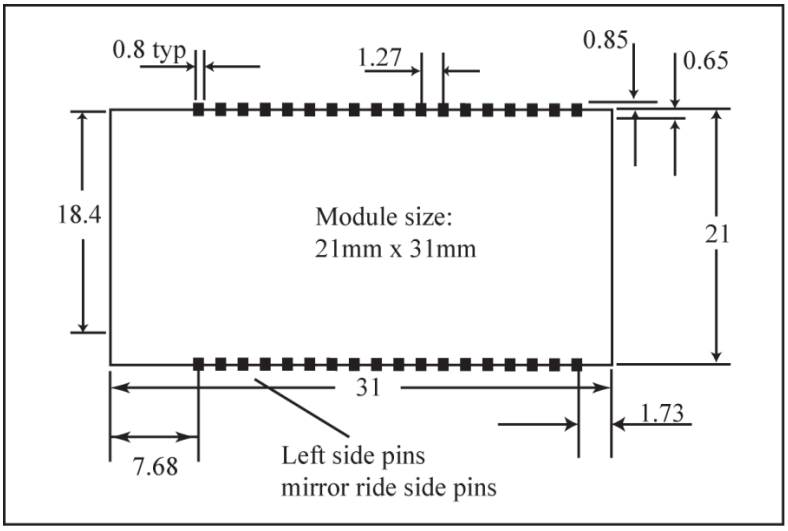


Figure 12: ZG2100M/ZG2101M Module Layout Pad Dimensions

4.2 Module Layout Guidelines

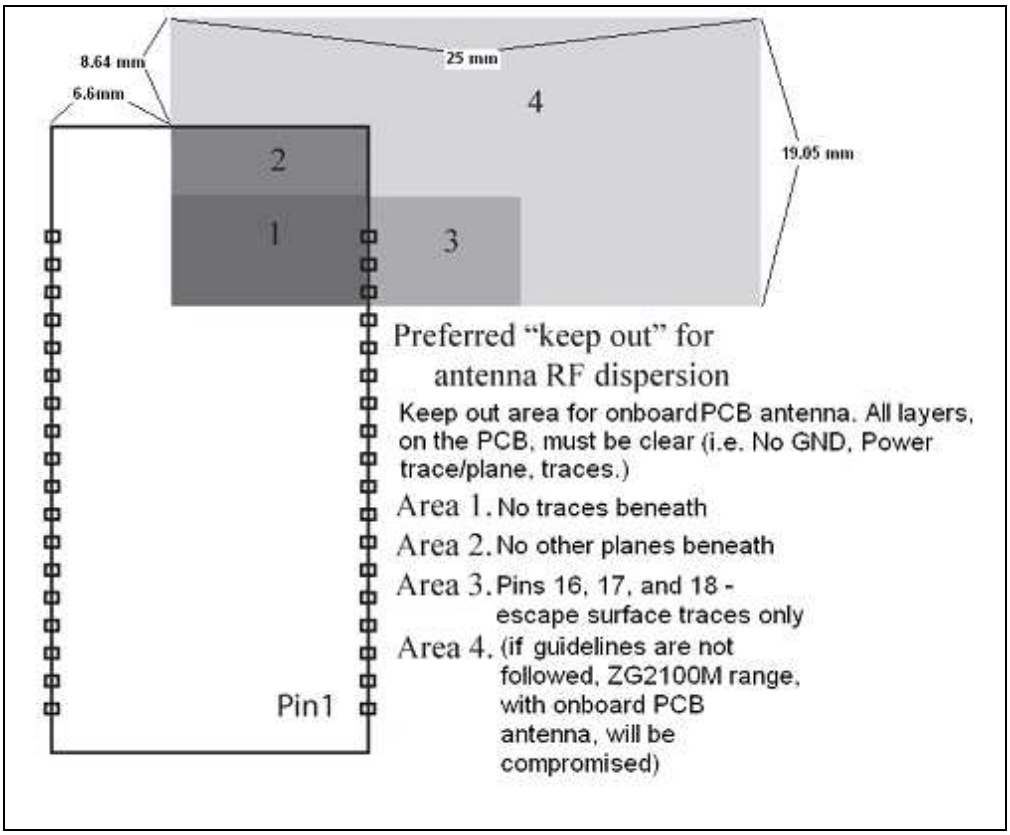


Figure 13: ZG2100M "Keep Out" Areas.

In addition to the guidelines in Figure 13, note the following suggestions:
ZG2100M and ZG2101M

- Bypass capacitors for VDD_3.3 should be as close as possible.
- Do not route any nets to VDD_1.8
- Do not use VDD_1.8 to source any external nets.
- Never place the antenna very close to metallic objects.
- The external antennas need a reasonable ground plane area for antenna efficiency.
- ZG2100M onboard PCB antenna specific
- Do not use a metallic or metalized plastic for the end product enclosure.
- Keep Plastic enclosure 1cm min height above the ZG2100M PCB antenna while maintaining the keep-out area, as shown in Figure 13.

4.3 Module Use Schematic

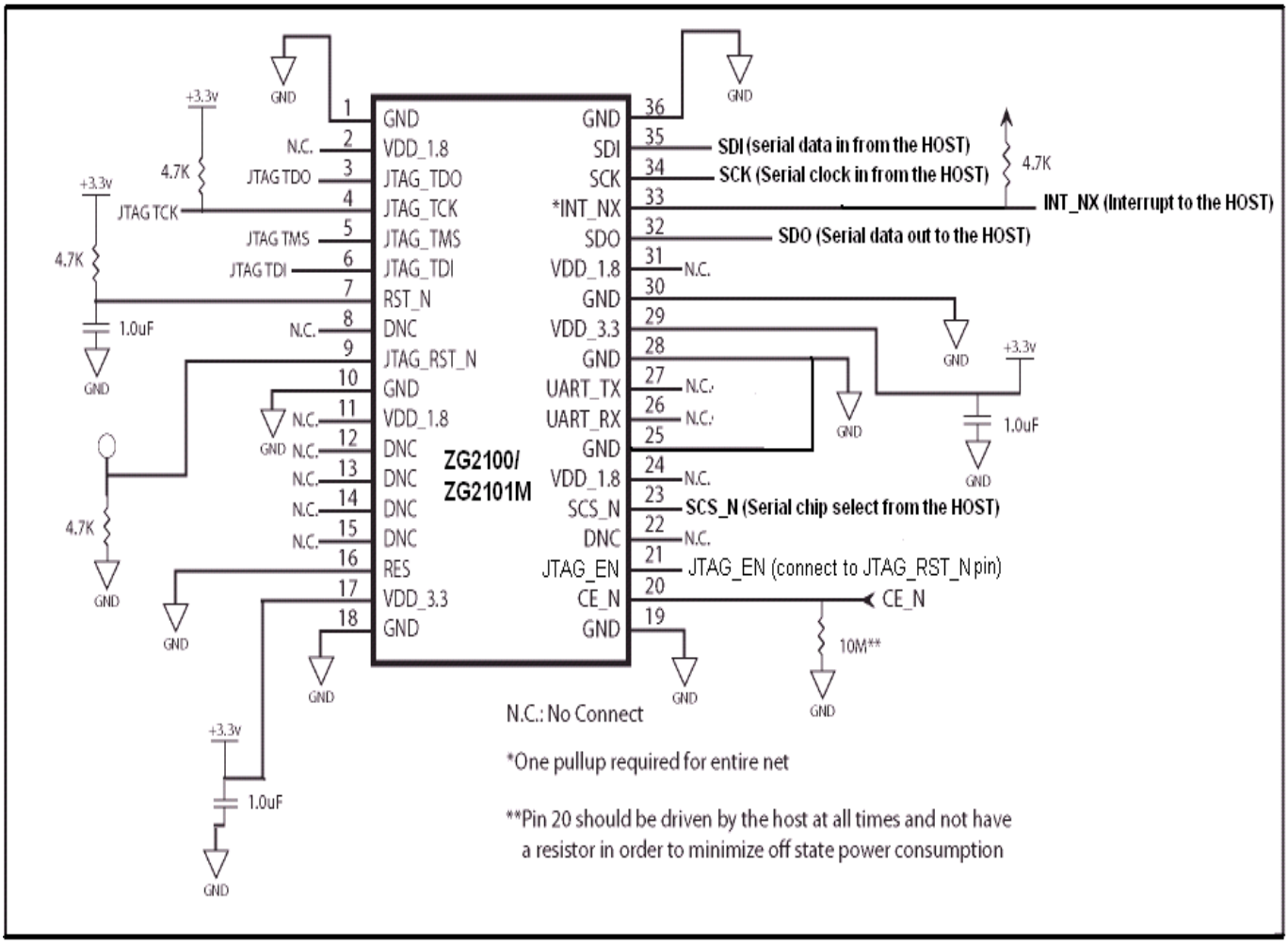


Figure 14: ZG2100M/ZG2101M Module Use Schematic.

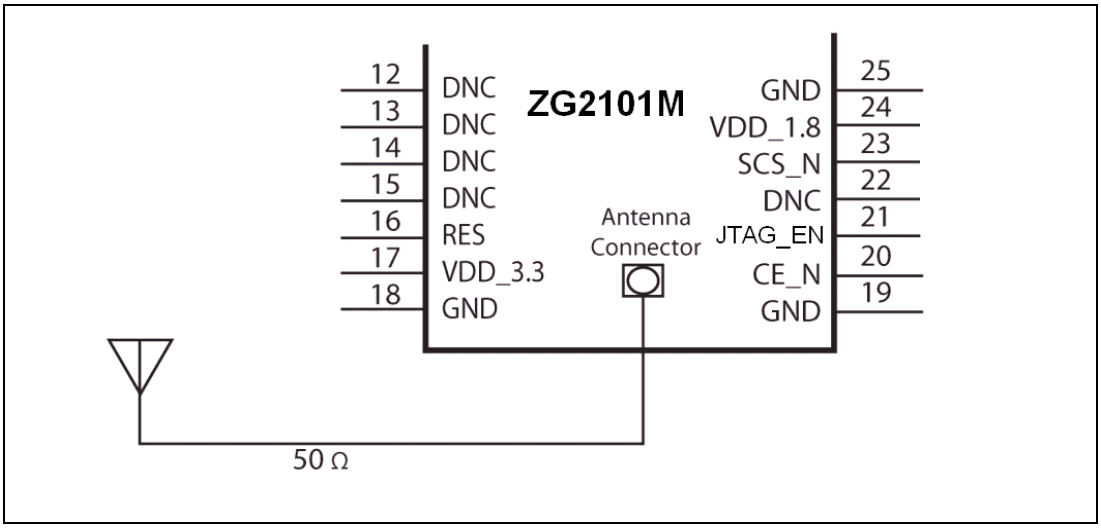


Figure 15: ZG2101M Antenna Connector/RF port diagram

Other Notes:

1. If RST_N is always driven by the HOST, the RC circuit is not needed on this pin.
2. RES is used as write-protect for the internal module SPI Flash. For production use, this pin should be pulled low. Host control will enable in-field FLASH updates.
3. It's recommended to connect UART_RX/TX (pins 26 and 27) to surface mount test points or header points, on the board, for optional connection to Hyperterminal for debugging purposes. Otherwise, they can be left as No Connects.
4. Ensure the HOST always drives the SPI port, even when not in use; otherwise, put 4.7K pull ups, to VDD_3.3, on SDI, SCK, and SCS_N.

5. Electrical Characteristics

Absolute Maximum Ratings:

Rating	Min	Max
Storage Temperature	-40C	+125C
3V supply (VDD_3.3)	0V	4.2V
VDD_3.3		0.5mSec
SDI, SCS_N, and SCK pins	-0.3 V	5.5 V

Recommended Operating Conditions:

Operating Condition	Min	Typ	Max
Ambient Temperature Range, commercial parts	0C		+70C
3V supply (VDD_3.3) – with FCC and IC cert	2.70V	3.3V	3.63V
3V supply (VDD_3.3) – for ETSI cert	2.80V	3.3V	3.63V
3V supply (VDD_3.3) – for Japan cert	2.97V	3.3V	3.63V

5.1 Power Consumption

Nominal conditions: 25C, VDD_3.3=3.3V

Power Conservation Modes	Min	Typ	Max	Unit
Hibernate, CE_N=3.3v		0.1		uA
Sleep		250		uA
Standby (transitional power state)		10		mA
Core Supply	**Min**	**Typ**	**Max**	**Unit**
Rx On, Receive Irx @ -83dBm with 2Mb/Sec. modulated signal input power at antenna port		85		mA
Tx On, Transmit Itx, +0dBm		115		mA
Tx On, Transmit Itx, +10dBm		154		mA

Electrical Characteristics Notes:

1. If VDD_3.3V supply takes longer than Maximum ramp up time, then CE_N or RST_N (held in active states; CE_N=3.3V or RST_N=0V) must be used to delay module boot up until VDD_3.3 is within operating conditions range.

2. For Rx On, RX chain is fully ON.

3. For Tx On, Pout= 0dBm (measured at antenna); 2Mb/Sec. modulated signal
4. For Tx On, Pout= +10dBm (measured at antenna); 2Mb/Sec. modulated signal
5. 3.3V Current Consumption values represent Typical Peak currents, and the measured currents conditions were done with 85% duty cycle modulated signal. WiFi applications typically operate in less than 85% TX duty cycle. Tx is dependent on such criteria as transmit power setting, and transmit data rate and bandwidth being used. Rx is affected by connectivity distance.
6. All characteristics in this specification are for commercial temperature rated parts only.
7. Operation in EU and/or Japan over extended voltage range of 2.7V to 3.6V will require additional certification testing by customer. The module is capable of this operation.
8. While 3.63V is the maximum operating voltage, the module will detect an overvoltage condition at 4.2V and disable the RF Transmit function. This is an RF Certification behavior pertaining to disabling transmission in unforeseen overvoltage conditions.
9. Listed Absolute Maximum Ratings are not meant for functional operation. Operation at these levels is not guaranteed, and may reduce the operating life of the component.

6. Radio Characteristics

Nominal conditions: 25C, VDD_3.3=3.3V

Frequency range	Min	Max	Unit
F_LO	2412	2484	MHz

6.1 Transmitter 2.4 GHz Band

Nominal conditions: 25C, VDD_3.3 =3.3V, Flo=2437MHz; 2Mb/Sec. modulated signal duty cycled at 95% measured at recommended single ended balun output (see Figure 8).

TX	Min	Typ	Max	Unit
Average Pout (Transmit spectrum mask Compliant)		+10		dBm
Average Pout gain step resolution from +5 to +10 dBm		0.5		dB
Average Pout gain step resolution from -5 to +5 dBm		1.0		dB
Average Pout settled variation	-0.5		0.5	dB

6.2 Receiver 2.4 GHz Band

Nominal conditions: 25C, VDD_3.3 =3.3V, Flo=2437MHz; measured at recommended single ended balun input (see Figure 8).

RX	Min	Typ	Max	Unit
RX Min Input Level Sensitivity, 1Mbps, 8% PER		-91		dBm
RX Min Input Level Sensitivity, 2Mbps, 8% PER		-88		dBm
RX Max Input Level (Power), 1Mbps, 8% PER		-4		dBm
RX Max Input Level (Power), 2Mbps,8% PER		-4		dBm