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Z8 GP™ Microcontrollers

ZGP323L OTP MCU Family

Preliminary Product Specification

PS023702-1004



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Table of Contents

Development Features	1
General Description	2
Pin Description	4
Absolute Maximum Ratings	10
Standard Test Conditions	10
DC Characteristics	11
AC Characteristics	14
Pin Functions	16
XTAL1 Crystal 1 (Time-Based Input)	16
XTAL2 Crystal 2 (Time-Based Output)	16
Port 0 (P07–P00)	16
Port 1 (P17–P10)	17
Port 2 (P27–P20)	18
Port 3 (P37–P30)	19
RESET (Input, Active Low)	23
Functional Description	23
Program Memory	23
RAM	23
Expanded Register File	24
Register File	28
Stack	29
Timers	30
Counter/Timer Functional Blocks	38
Expanded Register File Control Registers (0D)	64
Expanded Register File Control Registers (0F)	69
Standard Control Registers	73
Package Information	80
Ordering Information	89
Precharacterization Product	95



List of Figures

Figure 1. Functional Block Diagram	3
Figure 2. Counter/Timers Diagram	4
Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	5
Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	6
Figure 5. 40-Pin PDIP/CDIP* Pin Configuration	7
Figure 6. 48-Pin SSOP Pin Configuration	8
Figure 7. Test Load Diagram	10
Figure 8. AC Timing Diagram	14
Figure 9. Port 0 Configuration	17
Figure 10. Port 1 Configuration	18
Figure 11. Port 2 Configuration	19
Figure 12. Port 3 Configuration	20
Figure 13. Port 3 Counter/Timer Output Configuration	22
Figure 14. Program Memory Map (32K OTP)	24
Figure 15. Expanded Register File Architecture	26
Figure 16. Register Pointer	27
Figure 17. Register Pointer—Detail	29
Figure 18. Glitch Filter Circuitry	38
Figure 19. Transmit Mode Flowchart	39
Figure 20. 8-Bit Counter/Timer Circuits	40
Figure 21. T8_OUT in Single-Pass Mode	41
Figure 22. T8_OUT in Modulo-N Mode	41
Figure 23. Demodulation Mode Count Capture Flowchart	42
Figure 24. Demodulation Mode Flowchart	43
Figure 25. 16-Bit Counter/Timer Circuits	44
Figure 26. T16_OUT in Single-Pass Mode	45
Figure 27. T16_OUT in Modulo-N Mode	45
Figure 28. Ping-Pong Mode Diagram	47
Figure 29. Output Circuit	47
Figure 30. Interrupt Block Diagram	49
Figure 31. Oscillator Configuration	51
Figure 32. Port Configuration Register (PCON) (Write Only)	53
Figure 33. STOP Mode Recovery Register	55
Figure 34. SCLK Circuit	56



Figure 35. Stop Mode Recovery Source	57
Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)	59
Figure 37. Watch-Dog Timer Mode Register (Write Only)	60
Figure 38. Resets and WDT	61
Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)	64
Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)	65
Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)	67
Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)	68
Figure 43. Voltage Detection Register	69
Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)	70
Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)	71
Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)	72
Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)	73
Figure 48. Port 2 Mode Register (F6H: Write Only)	73
Figure 49. Port 3 Mode Register (F7H: Write Only)	74
Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)	75
Figure 51. Interrupt Priority Register (F9H: Write Only)	76
Figure 52. Interrupt Request Register (FAH: Read/Write)	77
Figure 53. Interrupt Mask Register (FBH: Read/Write)	77
Figure 54. Flag Register (FCH: Read/Write)	78
Figure 55. Register Pointer (FDH: Read/Write)	78
Figure 56. Stack Pointer High (FEH: Read/Write)	79
Figure 57. Stack Pointer Low (FFH: Read/Write)	79
Figure 58. 20-Pin CDIP Package	80
Figure 59. 20-Pin PDIP Package Diagram	81
Figure 60. 20-Pin SOIC Package Diagram	81
Figure 61. 20-Pin SSOP Package Diagram	82
Figure 62. 28-Pin CDIP Package	83
Figure 63. 28-Pin SOIC Package Diagram	84
Figure 64. 28-Pin PDIP Package Diagram	85
Figure 65. 28-Pin SSOP Package Diagram	86
Figure 66. 40-Pin CDIP Package	87
Figure 67. 40-Pin PDIP Package Diagram	87
Figure 68. 48-Pin SSOP Package Design	88



List of Tables

Table 1.	Features	1
Table 2.	Power Connections	3
Table 3.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification.	5
Table 4.	28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification.	6
Table 5.	40- and 48-Pin Configuration	8
Table 6.	Absolute Maximum Ratings	10
Table 7.	Capacitance	11
Table 8.	DC Characteristics	11
Table 9.	EPROM/OTP Characteristics	13
Table 10.	AC Characteristics	15
Table 11.	Port 3 Pin Function Summary	21
Table 12.	CTR0(D)00H Counter/Timer8 Control Register	31
Table 13.	CTR1(0D)01H T8 and T16 Common Functions.	33
Table 14.	CTR2(D)02H: Counter/Timer16 Control Register.	36
Table 15.	CTR3 (D)03H: T8/T16 Control Register	37
Table 16.	Interrupt Types, Sources, and Vectors	50
Table 17.	IRQ Register	50
Table 18.	SMR2(F)0DH:Stop Mode Recovery Register 2*	56
Table 19.	Stop Mode Recovery Source	58
Table 20.	Watch-Dog Timer Time Select	61
Table 21.	EPROM Selectable Options	62



Development Features

Table 1 lists the features of ZiLOG®'s Z8 GP™ OTP MCU Family family members.

Table 1. Features

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323L OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–3.6V

- Low power consumption—6mW (typical)
- T = Temperature
S = Standard 0° to +70°C
E = Extended -40° to +105°C
A = Automotive -40° to +125°C
- Three standby modes:
 - STOP—2μA (typical)
 - HALT—0.8mA (typical)
 - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
 - One programmable 8-bit counter/timer with two capture registers and two load registers
 - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
 - Programmable input glitch filter for pulse reception
- Six priority interrupts
 - Three external
 - Two assigned to counter/timers
 - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
 - Port 0: 0–3 pull-up transistors
 - Port 0: 4–7 pull-up transistors

- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

► **Note:** The mask option pull-up transistor has a *typical* equivalent resistance of 200 K Ω \pm 50% at $V_{CC}=3$ V and 450 K Ω \pm 50% at $V_{CC}=2$ V.

General Description

The Z8 GP™ OTP MCU Family is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z8 GP™ OTP MCU Family architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

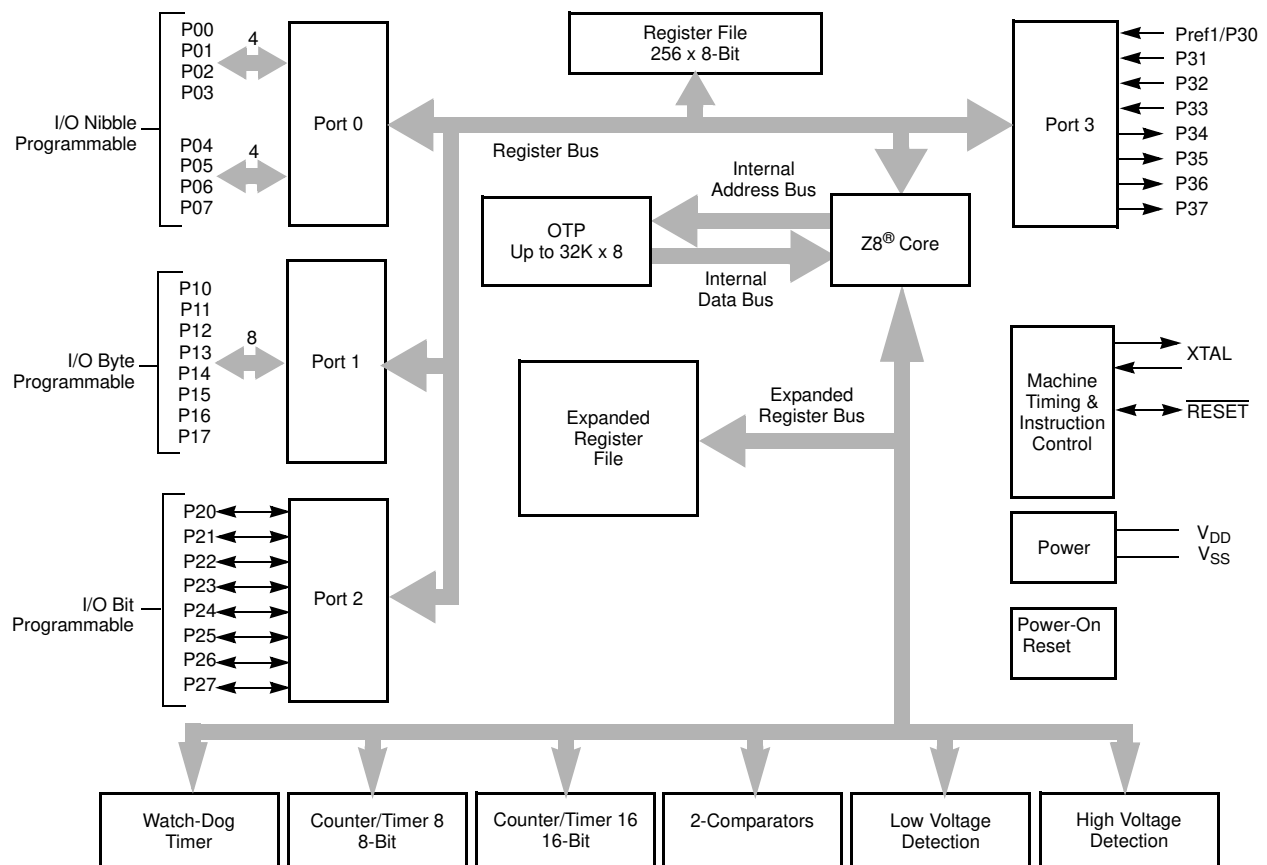
To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP MCU offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

► **Note:** All signals with an overline, “ $\bar{}$ ”, are active Low. For example, $\overline{B/W}$, in which WORD is active Low, and $\overline{B/W}$, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.

Table 2. Power Connections

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

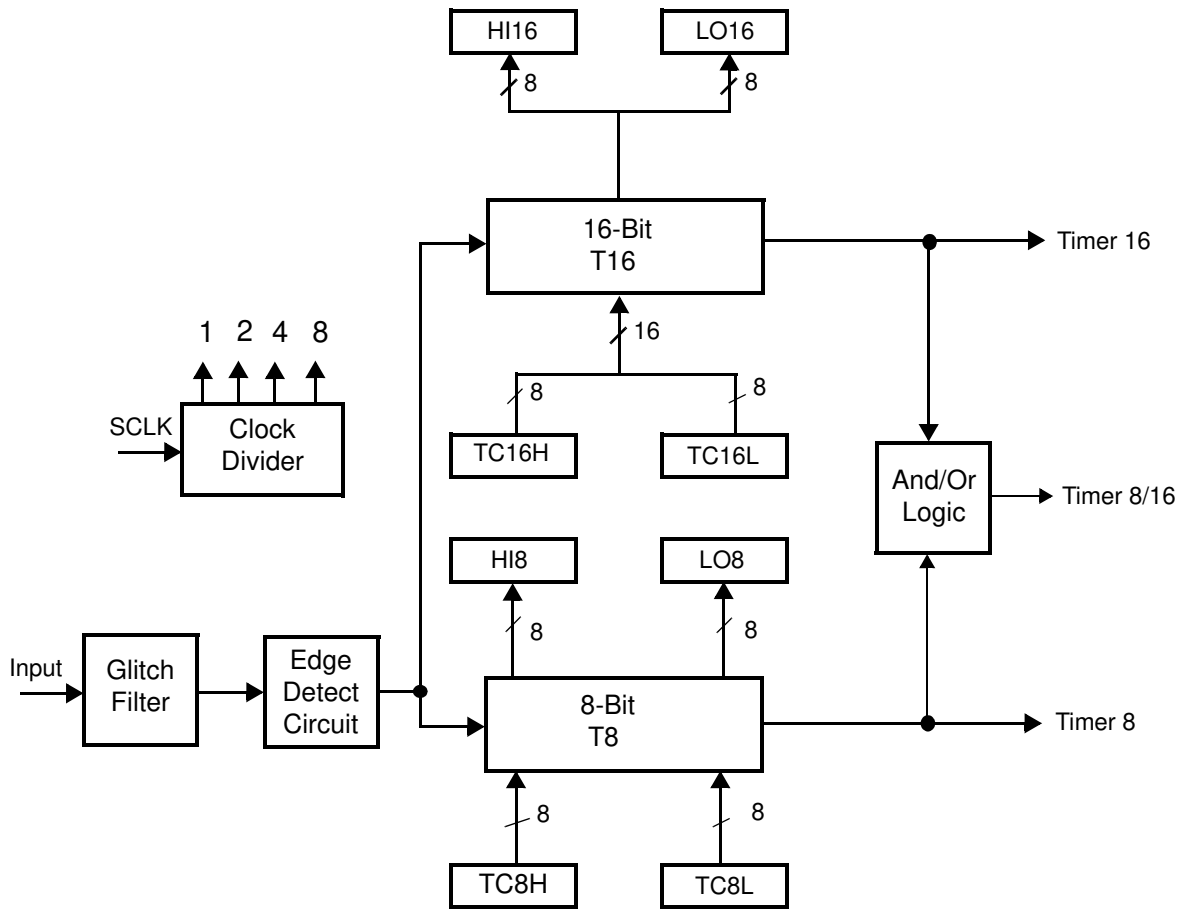


Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 5.

For customer engineering code development, a UV erasable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.

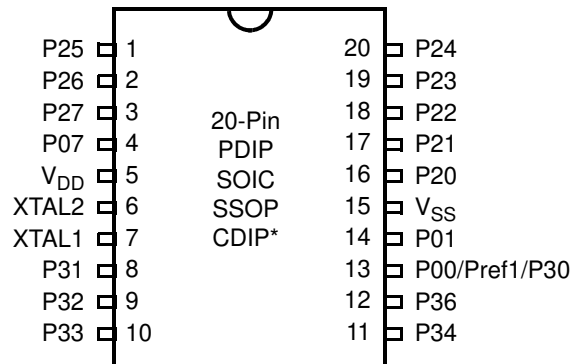


Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V _{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V _{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

► **Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

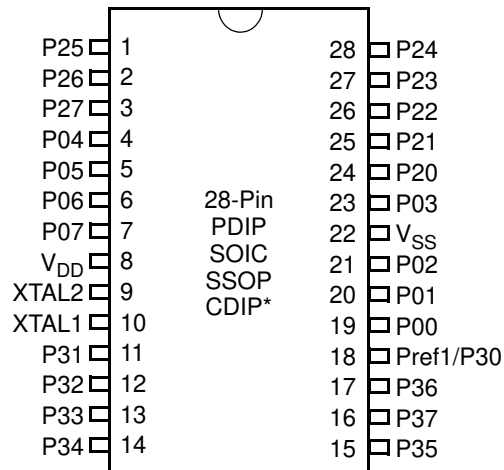


Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V _{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V _{CC} if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V _{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

► **Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

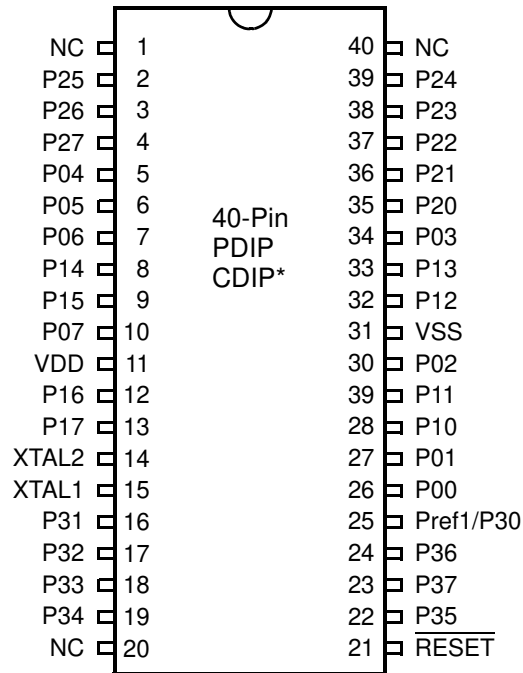


Figure 5. 40-Pin PDIP/CDIP* Pin Configuration

► **Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

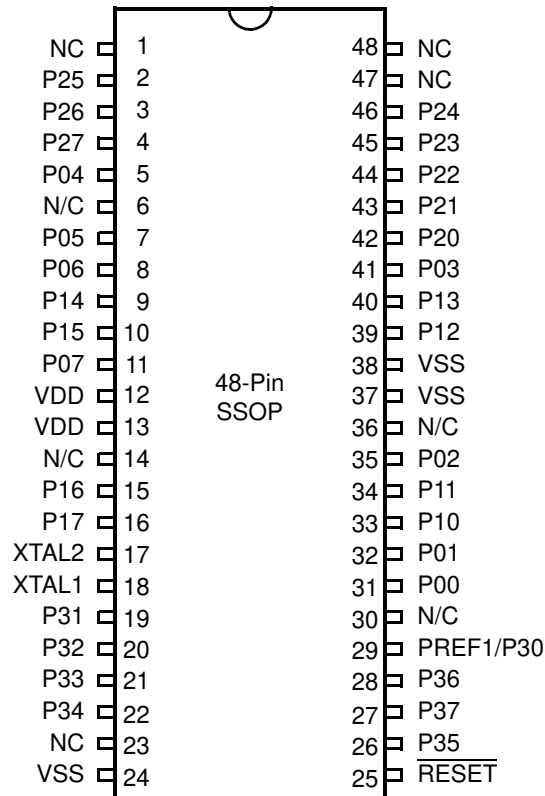


Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12



Table 5. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V _{DD}
31	24, 37, 38	V _{SS}
25	29	Pref1/P30
	48	NC

Absolute Maximum Ratings

Stresses greater than those listed in Table 7 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	0	+70	C	
Storage temperature	-65	+150	C	
Voltage on any pin with respect to V_{SS}	-0.3	+5.5	V	1
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μ A	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	

Notes:
This voltage applies to all pins except the following: V_{DD} , P32, P33 and $\overline{\text{RESET}}$.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).

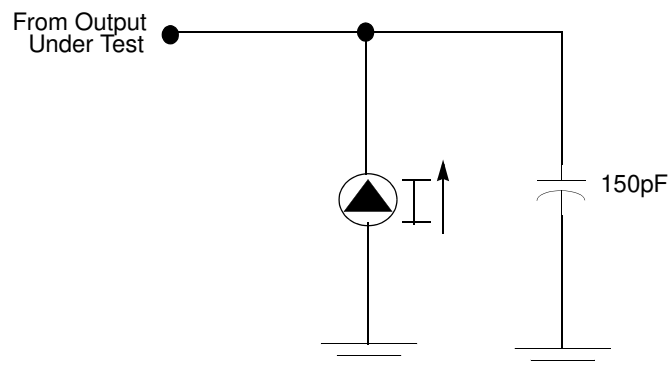


Figure 7. Test Load Diagram

Capacitance

Table 7 lists the capacitances.

Table 7. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF

Note: $T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{MHz}$, unmeasured pins returned to GND

DC Characteristics

Table 8. DC Characteristics

Symbol	Parameter	V_{CC}	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$			Units	Conditions	Notes
			Min	Typ	Max			
V_{CC}	Supply Voltage		2.0		3.6	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-3.6	0.8		$V_{CC}+0.3$	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		0.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-3.6	$0.7 V_{CC}$		$V_{CC}+0.3$	V		
V_{IL}	Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		$0.2 V_{CC}$	V		
V_{OH1}	Output High Voltage	2.0-3.6	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{mA}$	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	$V_{CC}-0.8$			V	$I_{OH} = -7\text{mA}$	
V_{OL1}	Output Low Voltage	2.0-3.6			0.4	V	$I_{OL} = 1.0\text{mA}$ $I_{OL} = 4.0\text{mA}$	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	$I_{OL} = 10\text{mA}$	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-3.6	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-3.6	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC} Pull-ups disabled	
I_{OL}	Output Leakage	2.0-3.6	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC}	
I_{CC}	Supply Current	2.0			10	mA	at 8.0 MHz	1, 2
		3.6			15	mA	at 8.0 MHz	1, 2

Table 8. DC Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A = 0°C to +70°C			Units	Conditions	Notes
			Min	Typ	Max			
I _{CC1}	Standby Current (HALT Mode)	2.0		3	mA	V _{IN} = 0V, V _{CC} at 8.0MHz	1, 2	
		3.6		5		Same as above	1, 2	
		2.0		2		Clock Divide-by-16 at 8.0MHz	1, 2	
		3.6		4		Same as above	1, 2	
I _{CC2}	Standby Current (Stop Mode)	2.0		8	μA	V _{IN} = 0 V, V _{CC} WDT is not Running	3	
		3.6		10	μA	Same as above	3	
		2.0		500	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3	
		3.6		800	μA	Same as above	3	
I _{LV}	Standby Current (Low Voltage)			10	μA	Measured at 1.3V	4	
V _{BO}	V _{CC} Low Voltage Protection			2.0	V	8MHz maximum Ext. CLK Freq.		
V _{LVD}	V _{CC} Low Voltage Detection			2.4	V			
V _{HVD}	V _{CC} High Voltage Detection			2.7	V			

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to the V_{DD} and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.



Table 9. EPROM/OTP Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	25			Cycles	1

Notes:

1. For windowed cerdip package only.
2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C.
Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

$$AF = \exp[(Ea/k) * (1/Tuse - 1/TStress)]$$

Where:

Ea is the intrinsic activation energy (eV; typ. 0.8)

k is Boltzman's constant (8.67 x 10⁻⁵ eV/°K)

°K = -273.16°C

Tuse = Use Temperature in °K

TStress = Stress Temperature in °K

3. At a stable UV Lamp output of 20mW/CM²

AC Characteristics

Figure 8 and Table 10 describe the Alternating Current (AC) characteristics.

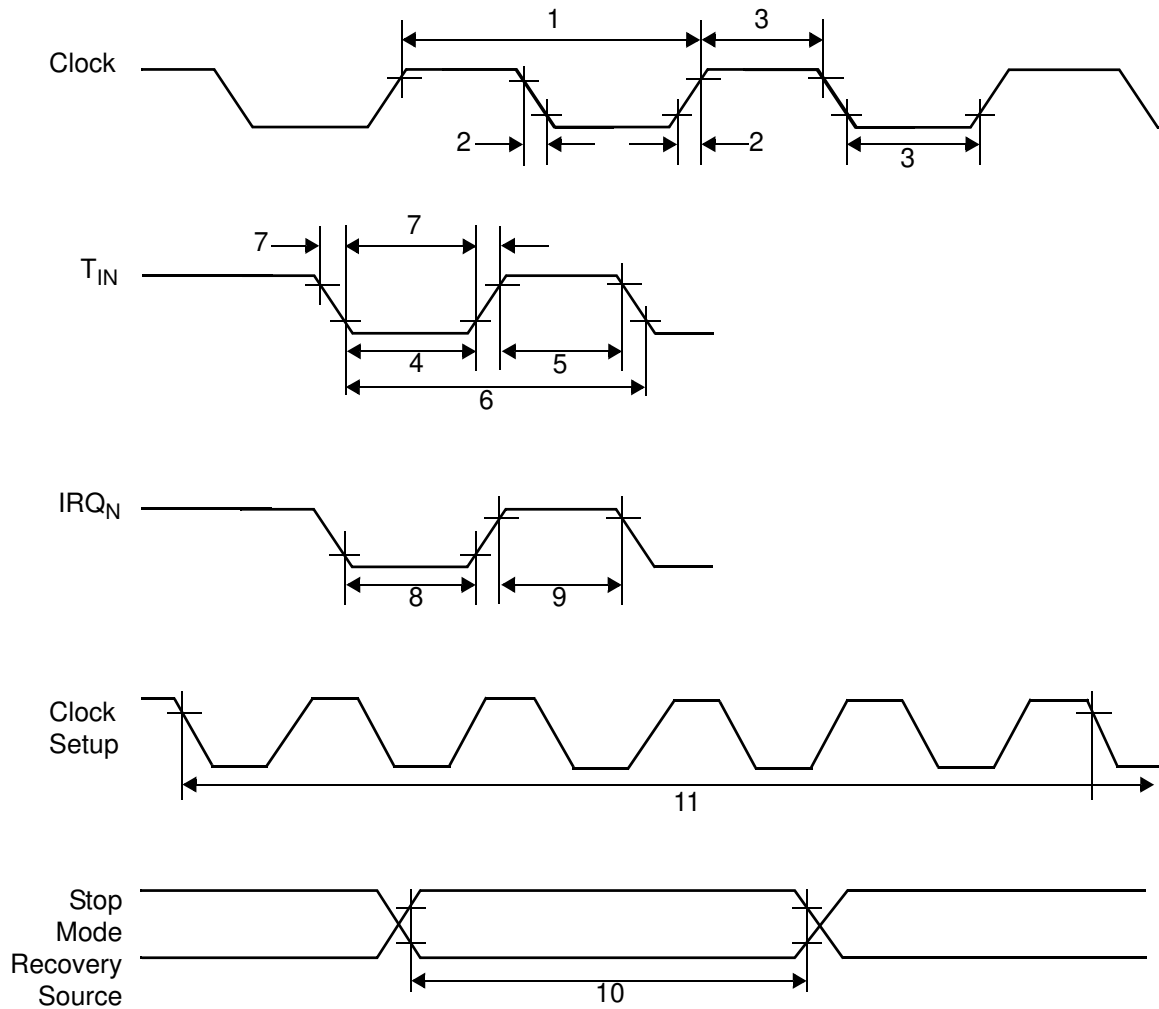


Figure 8. AC Timing Diagram



Table 10. AC Characteristics

No	Symbol	Parameter	V _{CC}	T _A =0°C to +70°C 8.0MHz		Units	Notes	Watch-Dog Timer Mode Register (D1, D0)
				Minimum	Maximum			
1	T _{pC}	Input Clock Period	2.0–3.6	121	DC	ns	1	
2	TrC, TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0–3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1	
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1	
7	TrTin, TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4	
12	Twdt	Watch-Dog Timer Delay Time	2.0–3.6	5 10 20 80		ms ms ms ms	0, 0 0, 1 1, 0 1, 1	
13	T _{POR}	Power-On Reset	2.0–3.6	2.5	10	ms		

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator output.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

- **Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

The Port 0 direction is reset to be input following an SMR.

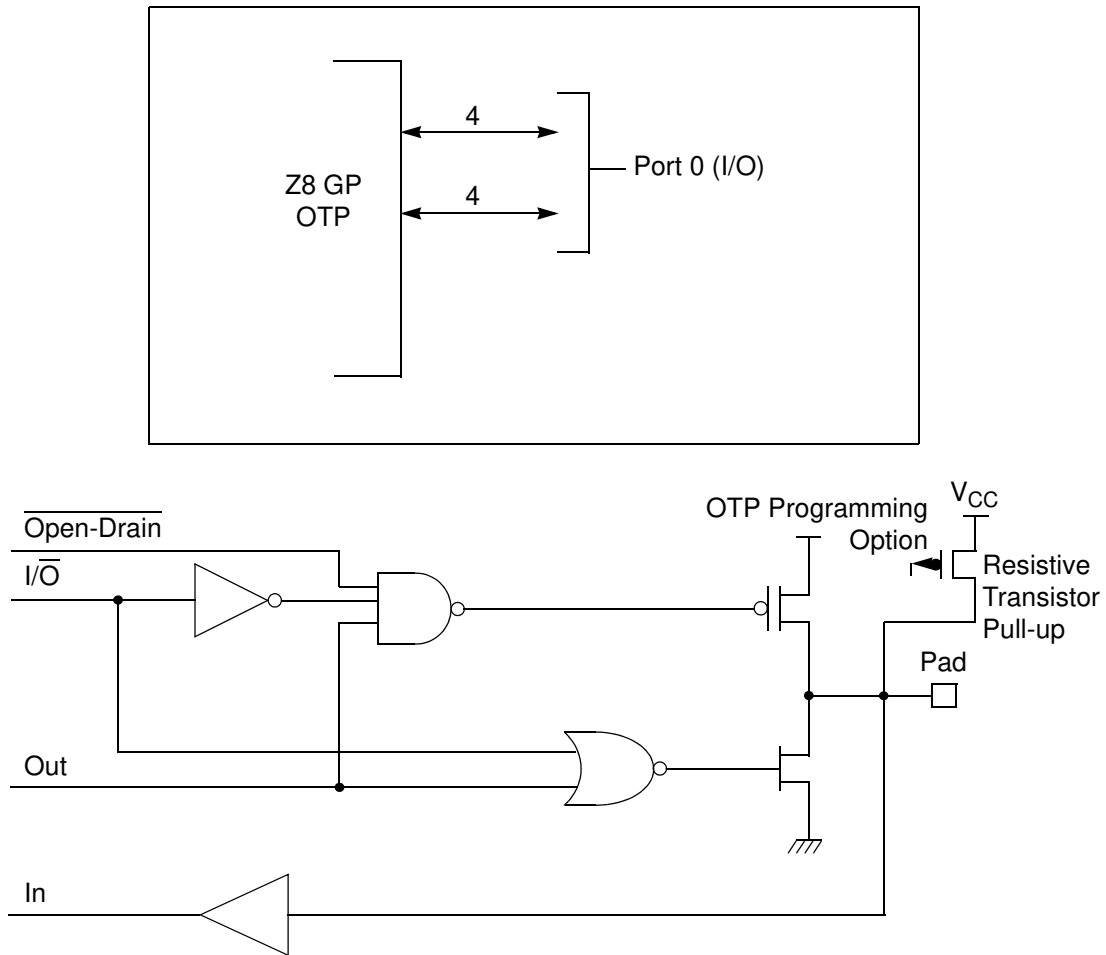


Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Note:** The Port 1 direction is reset to be input following an SMR.

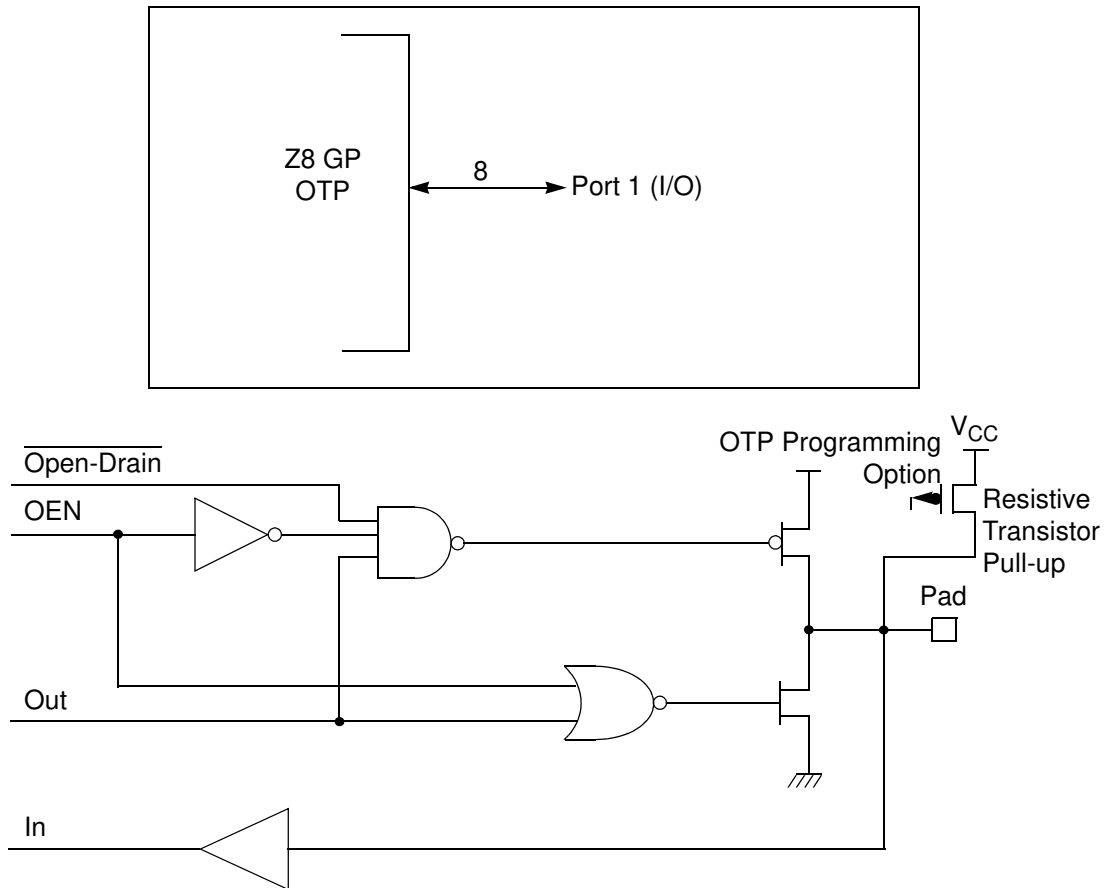


Figure 10. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.

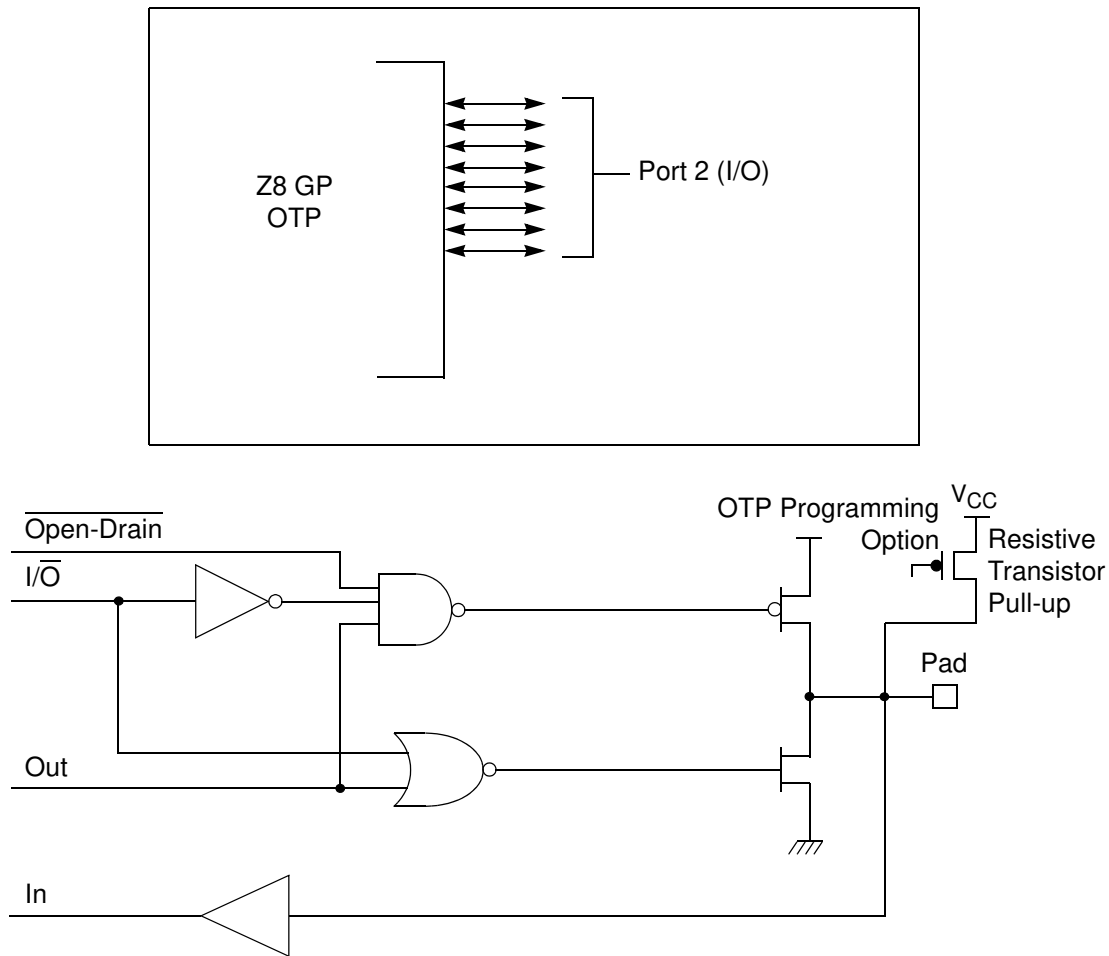


Figure 11. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.