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1   The ZIOL2xxx IC Family Overview

IDT provides a universal and IO-Link compatible cable driver IC by issuing the ZIOL2401 integrated circuit. The ZIOL2401 is highly configurable and suitable for a wide range of applications in process and factory automation. In order to fulfill the requirements of specific applications stripped down versions of the IC were required. The ZIOL2xxx IC family is derived from the ZIOL2401 by modification (elimination or disabling) of certain functional building blocks. In this combination the following building blocks or functions are affected:

- The transceiver channels COM and AUX
- The availability of the integrated DC/DC converter
- The activation of a read-only data access via the SPI interface

This datasheet describes the entire IC family ZIOL2xxx. Respective notes or footnotes describe the availability the above mentioned building blocks or functionality with respect to certain IC family members. Table 1.1 shows an overview concerning the ZIOL2xxx IC family and the used naming convention.

Table 1.1   ZIOL2xxx Product Matrix and Product Naming Convention

ZIOL2xxx Member	Transceiver Channel	DC/DC Converter	SPI Access	Remarks
ZIOL2401	COM + AUX	yes	r/w	Base type - released
ZIOL2201	COM	yes	r/w	released
ZIOL2101	AUX	yes	r/w	[1]
ZIOL2411	COM + AUX	no	r/w	released
ZIOL2211	COM	no	r/w	released
ZIOL2111	AUX	no	r/w	[1]
ZIOL2402	COM + AUX	yes	r	[1]
ZIOL2202	COM	yes	r	[1]
ZIOL2102	AUX	yes	r	[1]
ZIOL2412	COM + AUX	no	r	[1]
ZIOL2212	COM	no	r	[1]
ZIOL2112	AUX	no	r	[1]

[1]   For future product releases, please contact IDT's sales representative

Z I O L 2 x x x

SPI Access
1 = read/write
2 = read-only

DC/DC Converter
0 = available
1 = not available

Transceiver Channels
4 = Two Channels (COM and AUX)
2 = COM channel only
1 = AUX Channel only

2   Electrical Characteristics

2.1.   Absolute Maximum Ratings

Parameters apply in operation temperature range and without time limitations.

Table 2.1   Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Conditions
V_{DD_HV}	Supply voltage	-0.3	40	V	
V_{HV}	Voltage at HV pins	-0.3	V_{DD_HV}+0.3	V	
V_{LV}	Voltage at LV pins	-0.3	V_{DD_LV}+0.3	V	[2]
V_{imp}	Impulse voltage withstand	60		V	according to IEC 60947-5-2
V_{ESD}	Abs. ESD test voltage		2k	V	according to HBM
T_s	Junction temperature		125	°C	[1]
T_a	Storage temperature	-50	150	°C	
P_{tot}	Average total power dissipation		2.6	W	integration period < 10ms [3]

[1] Average die-temperature.

[2] Exceptions are the digital input pins (µC interface) which tolerate 5V logic signals (refer to Table 5.1).

[3] The allowed total power dissipation depends on the in the PCB design achieved thermal resistance R_{th} (package/ambient) and the ambient operation temperature as shown in Figure 2.1. In order to obtain optimal heat distribution (R_{th} < 35K/W) certain PCB layout rules shall be applied. Those rules are described in the application note for the used QFN package (refer to chapter 8, [4]).

Figure 2.1   Max. Total Power Dissipation
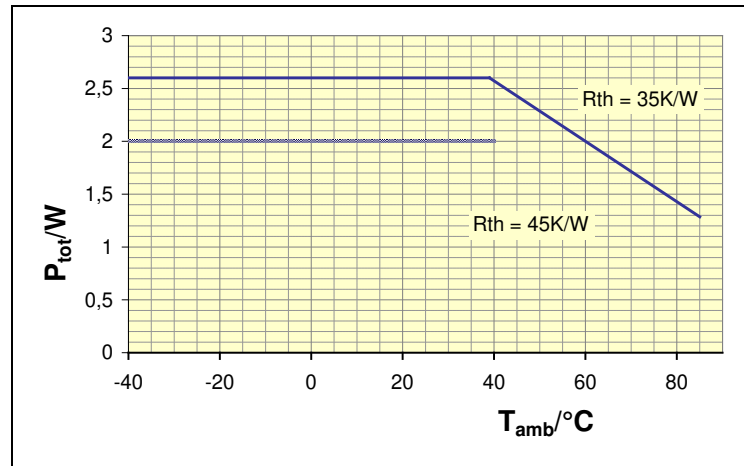
2.2. Operating Conditions

Table 2.2 Operating Conditions

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
V_{DD_HV}	Supply voltage	8.0	24	36	V	
V_{in}	Linear regulator input voltage	4.75		36	V	LR_IN can be connected to V_{DD_HV} or DC/DC output voltage.
V_{DD_LV}	Linear regulator output voltage	3.0	3.3	3.6	V	Voltage LR_OUT → GND pin
I_{out}	Linear regulator output current			10	mA	LR_OUT provides supply current for external applications. [2]
$t_{startup}$	Startup timing @ V_{DD_HV} = 8V			5	ms	Time for system start up including loading of configuration registers from EEPROM
T_{amb}	Operating ambient temperature	-40		+85	°C	
f_{osc}	Internal oscillator frequency	4.5		5.5	MHz	Internal clock is not available externally. All digital circuit timing parameters of the IC are derived from the internal clock.

[1] The mentioned typical values of IC properties are provided for information only.
[2] While start-up (until the voltage at LR_OUT has reached 1V) the output current may be limited to 5mA.

2.3. Electrical Parameters

All parameter values are valid under operating conditions specified in chapter 2.2 if no other conditions are mentioned.

Table 2.3   Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
Transmitter Output Stages (COM[1]/AUX[2])						
I_{DAL_0}	Alarm level threshold corresponding to configurable output current limitation [2]	50		I_{Dout_0}	mA	Dual mode
I_{DAL_1}		100		I_{Dout_1}	mA	The active setting is defined in the configuration registers
I_{DAL_2}	Dual Driver Mode	200		I_{Dout_2}	mA	
I_{DAL_3}		250		I_{Dout_3}	mA	
I_{MAL_0}	Alarm level threshold corresponding to configurable output current limitation [2]	100		I_{Mout_0}	mA	Tandem mode
I_{MAL_1}		200		I_{Mout_1}	mA	The active setting is defined in the configuration registers.
I_{MAL_2}	Tandem Driver Mode	400		I_{Mout_2}	mA	
I_{MAL_3}		500		I_{Mout_3}	mA	
I_{Dout_0}	Configurable output current limit[2]	56		95	mA	Dual mode
I_{Dout_1}	Dual Driver Mode	112		180	mA	The active setting is defined in the configuration registers.
I_{Dout_2}		224		330	mA	
I_{Dout_3}		280		410	mA	
I_{Mout_0}	Configurable output current limit[2]	112		180	mA	Tandem mode
I_{Mout_1}	Tandem Driver Mode	224		360	mA	The active setting is defined in the configuration registers.
I_{Mout_2}		448		660	mA	
I_{Mout_3}		560		820	mA	
SR_{38}	Slew rate [3]	6	10	14[5]	V/µs	referring to IO-Link Spec.: 38,4kBaud (COM2),
SR_{230}		40	60	80[5]	V/µs	referring to IO-Link Spec.: 230.4kBaud (COM3)
$t_{TLHdelayCOM3}$	Propagation delay L-H edge			250	ns	Time from LV L-H edge till HV edge begins to rise (COM3 baud rate)
$t_{THLdelayCOM3}$	Propagation delay H-L edge			250	ns	Time from LV H-L edge till HV edge begins to fall (COM3 baud rate)
$t_{TLHdelayCOM2}$	Propagation delay L-H edge			700	ns	Time from LV L-H edge till HV edge begins to rise (COM2 baud rate)

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[1] The COM transmitter is only available inside the products ZIOL24xx/22xx
[2] The AUX transmitter is only available inside the products ZIOL24xx/21xx

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
$t_{THLdelayCOM2}$	Propagation delay H-L edge			700	ns	Time from LV H-L edge till HV edge begins to fall (COM2 baud rate)
Receiver Input Channels (COM[1]/AUX[2])						
V_{ih1}	IO-Link specific threshold, High	10.75		12.75	V	
V_{il1}	IO-Link specific threshold, Low	8.75		10.75	V	
V_{ihyst1}	IO-Link specific thresholds, Hysteresis	1.5		2.5	V	
V_{ih2}	Ratiometric threshold, High	52		57	$\% * V_{DD\_HV}$	
V_{il2}	Ratiometric threshold, Low	43		47.7	$\% * V_{DD\_HV}$	
V_{ihyst2}	Ratiometric thresholds, Hysteresis	7		11.6	$\% * V_{DD\_HV}$	
R_{in}	Input resistance	150			kOhms	
C_{in}	Input capacitance			20	pF	
t_{Rdelay}	Propagation delay without filtering			80 100 200	ns ns ns	No filter within signal path. Input edge with: >30V/µs (COM3) >5V/µs (COM2) >0.75V/µs (COM1)
$t_{FRdelay}$	Propagation delay with analog filtering	750	850	950	ns	@V_{DD_HV} = 24V, Input edge with: >30V/µs (COM3)
t_{Rpulse}	Minimal propagated pulse width without filtering		25		ns	
$t_{FRpulse}$	Minimal propagated pulse width with analog filtering		1.1		µs	
$t_{DIGdelay}$	Additional propagation delay with digital filtering	180		440	ns	
f_{cut}	Input filter – cut off frequency (-3dB) COM and AUX channel	100		250	kHz	filter characteristic: 1st order
I_{sink1}	Sink strength 1	2	2.5	3	mA	Line input voltage >5V
I_{sink2}	Sink strength 2	5	6	7	mA	According to IO-Link Specification
R_{pull}	Configurable pull-up/pull-down resistor @ COM_O/AUX_O	100k		250k	Ohms	

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[1] The COM receiver is only available inside the products ZIOL24xx/22xx
[2] The AUX receiver is only available inside the products ZIOL24xx/21xx

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
WURQ Detection						
t_{wurqL}	Lower pulse width limit of signal evaluated as IO-Link wake-up	60	68	75	µs	Refer to chapter 3.3.4
t_{wurqU}	Upper pulse width limit of signal evaluated as IO-Link wake-up	85	94	109	µs	Refer to chapter 3.3.4
DC/DC converter [1]						
V_{OUT}	Output voltage Range[6]	3		15	V	@ $V_{DD\_HV} > V_{out} + 2V$ (step down function only)
I_{LOAD}	Output load current	5[4]		50	mA	Current that flows to the application and the R-Divider
I_{PK}	Over current limit for output transistor		240		mA	Averaged current over complete short at DCDC converter output
f_{osc}	Operating frequency	2.25		2.75	MHz	
V_{ref}	Reference/feedback Voltage		1.225		V	at FB pin in steady state
ΔV_{OUT_Line}	DC Output Line Regulation		8		mV/V	@V_{out}=5V, I_{LOAD} = 5mA Filter: C=10µF, L=10µH
ΔV_{OUT_Load}	DC Output Load Regulation				mV/mA	Filter: C=10µF, L=10µH V_{OUT} = 5V
	@Vout=3.3V	0.7		1.4		
	@Vout=15V	3.3		6.9		
V_{ripple}	Ripple of Output Voltage				mV_{PP}	Filter: C=10µF, L=10µH V_{OUT} = 5V
	@ VDD_HV >= 24V		65[7]			
	@ VDD_HV < 24V		25[7]			
t_{strt}	Settling time after POR is released		1		ms	For C=10µF, L=10µH Higher C may result in higher t_{strt}
t_{DLY}	digital delay for DC_RDY signal	45	50	55	ms	If enabled in configuration
η	Efficiency	8]			%	Filter: C=10µF, L=10µH

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[1] The DC/DC converter is only available inside the products ZIOL2401/2402/2201/2202/2101/2102

Symbol	Parameter		Min	Typ[1]	Max	Unit	Conditions
Microcontroller Interface [9]							
V_{LIH}	Voltage range for input "high" level		2.5		5.5	V	@ V_{DD_LV} = 3.6V, otherwise $V_{LIH-min}$ = 0.7 * V_{DD_LV}
V_{LIL}	Voltage range for input "low" level		-0.3		0.9	V	@ V_{DD_LV} = 3.0V, otherwise $V_{LIL-max}$ = 0.3 * V_{DD_LV}
I_{LIH}	Logic "high" input current	@ pins without pull-up/pull-down resistors: INT_L, WURQ_L	-1		1	µA	@ V_{LIH} = V_{DD_LV}
I_{LIL}	Logic "low" input current		-1		1	µA	@ V_{LIL} = 0V
I_{LIH_PD}	Logic "high" input current	@ pins with pull-down resistors: TX_EN/SPI_CLK, TX/MOSI, AUX_EN, AUX_TX, DC_RDY	-300		-150	µA	@ V_{LIH} = V_{DD_LV-max} = 3.6V @ V_{LIH} = 5.5V, V_{DD_LV-max} = 3.6V
I_{LIL_PD}	Logic "low" input current		-1		1	µA	@ V_{LIL} = 0V, V_{DD_LV-max} = 3.6V @ V_{LIL} = 0V, V_{DD_LV-max} = 3.0V
I_{LIH_PU}	Logic "high" input current	@ pins with pull-up resistors: RST_L, SPI_EN_L	-1		1	µA	@ $V_{LIH-min}$ = V_{DD_LV-max} = 3.0V @ $V_{LIH-max}$ = V_{DD_LV-max} = 3.6V
I_{LIL_PU}	Logic "low" input current		-150		250	µA	@ V_{LIL} = 0V, V_{DD_LV-max} = 3.6V @ V_{LIL} = -0.3V, V_{DD_LV-max} = 3.6V
V_{LOL}	Logic "high" output voltage	@ output pins: RX/MISO, AUX_RX	0		5	%*V_{DD_LV}	@ I_{LIL} = 1mA
V_{LOH}	Logic "high" output voltage		95		100	%*V_{DD_LV}	@ I_{LIH} = -1mA
Internal Current Consumption [10]							
I_{VDD}	Current into VDD			1.7	2.5	mA	SPI_EN=3.3V
I_{LR_IN}	Current into LR_IN			2.2	3.4	mA	SPI_EN=3.3V

[1] The mentioned typical values of IC properties are provided for information only and shall not be considered as statistical guaranteed mean values. Typical values are not subject for measurement while the electrical test of each IC – they are correct by design.

[2] If the output current exceeds the configured current limit, the IC will raise an overload signal which causes up-counting of the overload counter (if configured) and which definitely limits the output current. However, the current limit will be performed after a certain settling time in order to ensure the configured slope of the output signal.

[3] Absolute edge rise and fall times are proportional to V_{DD_HV}

[4] A minimum of the output current must be provided by the application circuit. Otherwise the DC/DC converter shall be unused by interconnecting the FB pin with the LR_OUT pin. The required voltage divider (refer to Figure 3.21) may provide this current partly or in full.

[5] Slew-rate measured after settlement time of the output signal

[6] Configurable with an external voltage divider (refer to chapter 3.5)

[7] The ripple on the output voltage depends significantly on both the external components and the PCB layout. Reference PCB layouts are available from IDT. The layouts used in the application kits are shown in Figure 4.4; detailed layout data of the application kits are available from IDT upon request.

[8] The efficiency of the DC/DC converter is depending on the external components and the used PCB layout. Moreover, there is an influence from several operational conditions which is illustrated in the diagram of Figure 2.2

[9] Microcontroller interface pins are : RST_L, SPI_EN_L, INT_L, WURQ_L, TX_EN/SPI_CLK, TX/MOSI, RX/MISO, AUX_EN, AUX_TX, AUX_RX, DC_RDY

[10] Current consumption is measured by applying the maximum supply voltage at the supply pins VDD and LR_IN (V_{VDD_HV}=36V, V_{in}=36V) and using a decoupling cap of 10µF between LR_OUT and ground. Both VDD and both VSS pins are interconnected, respectively. Pins TX_EN/SPI_CLK, AUX_TX, TX_EN, AUX_EN, PFD, COM_I, AUX_I are connected to ground.

Figure 2.2   Efficiency of the DC/DC[1] converter for VOUT=5V, C=10µF and L=10µH
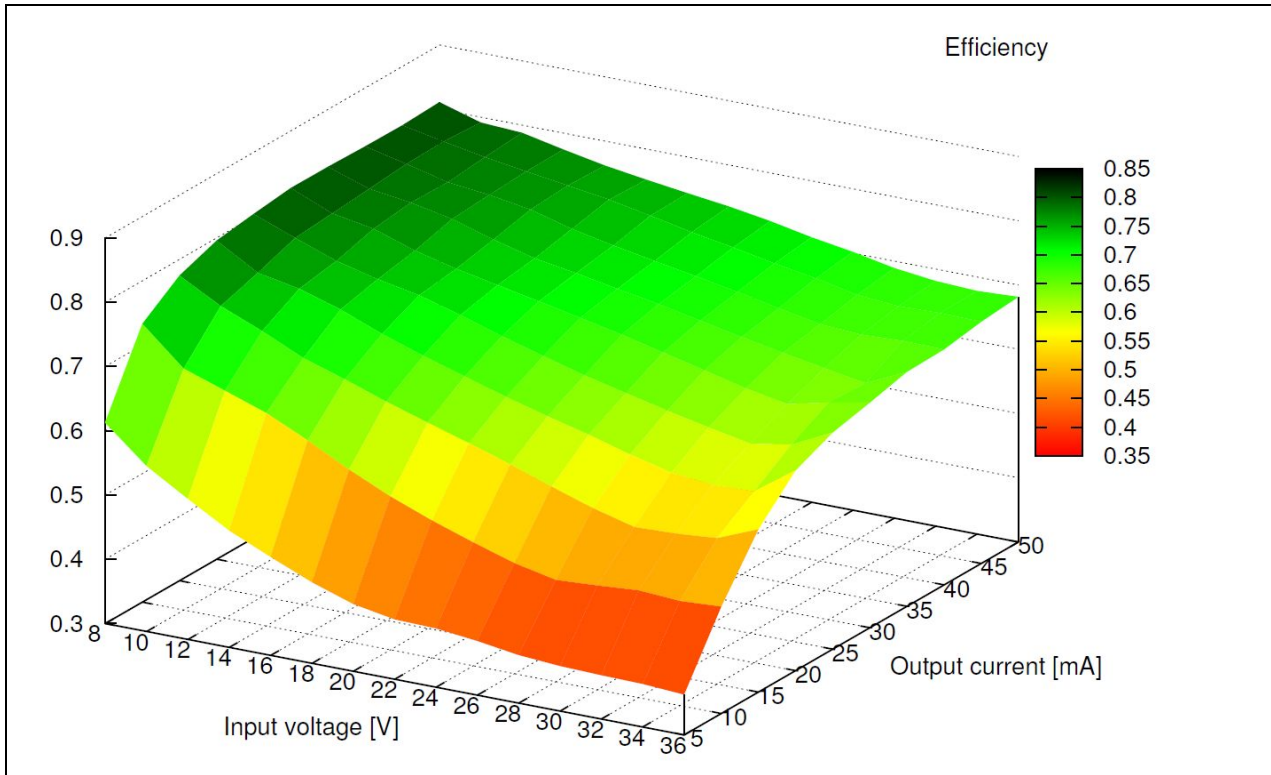
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[1] The DC/DC converter is only available inside the products ZIOL2401/2402/2201/2202/2101/2102

3 Detailed Description

3.1. Block schematic

Figure 3.1   Functional Block Diagram of the ZIOL2xxx
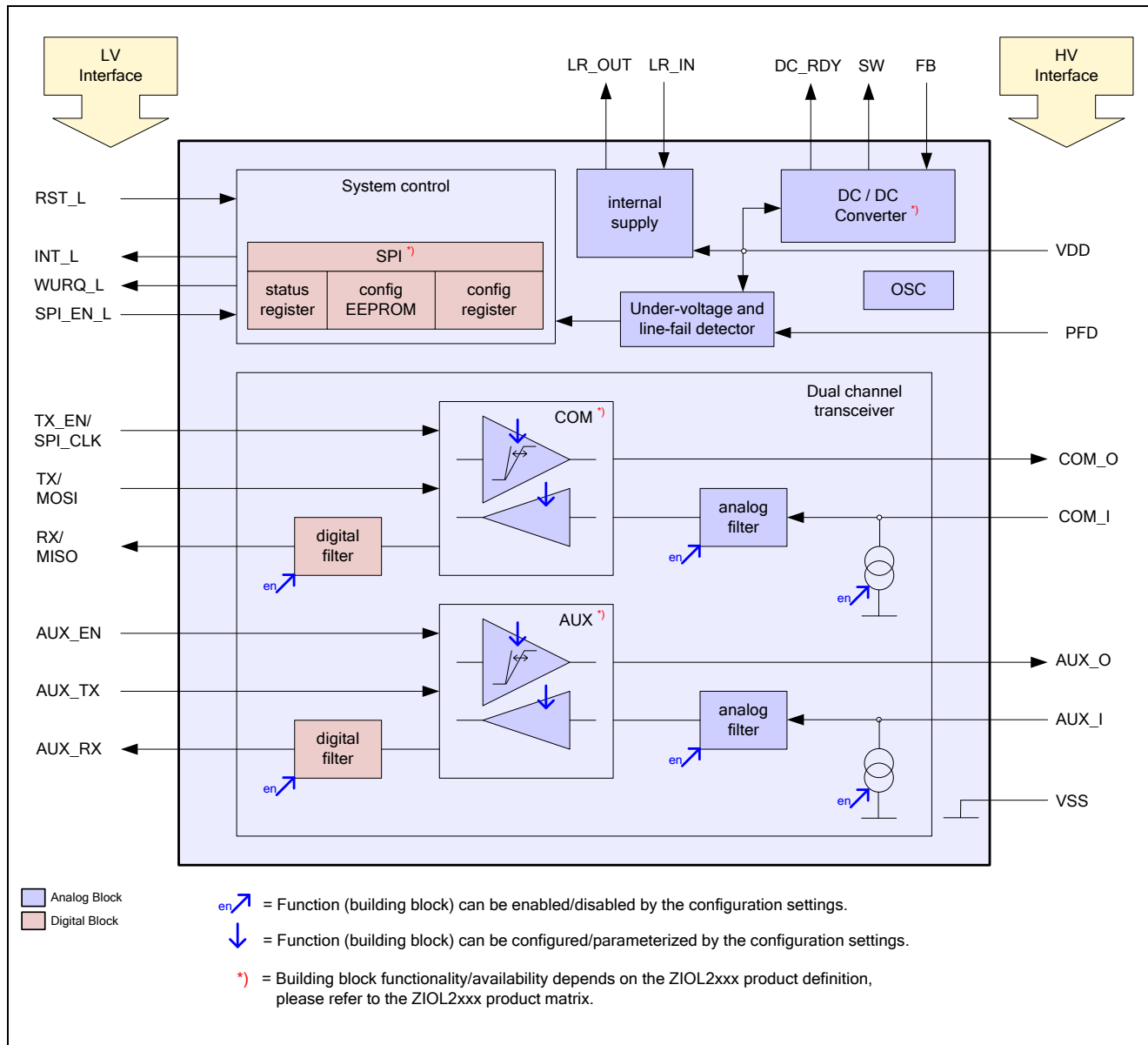
3.2.   Dual Channel Transceiver

3.2.1.   IC Data Path Configuration

The ZIOL2xxx ICs contains one (ZIOL22xx/21xx) or two (ZIOL24xx) transceiver channels. The channels inside the product versions with two channels can work independently in the "Dual Mode" or coordinated in "Tandem Mode". The data path of the ZIOL24xx Ics is illustrated in Figure 3.2. Both channels, which are designed identically, are widely configurable. Due to configuration and the range of supported supply voltages the Ics can be used in a broad field of applications. Example applications can be level shifter for standard sensor applications or driver for resistive, capacitive or inductive loads.

Figure 3.2   ZIOL24xx Transceiver Data Path in Principle
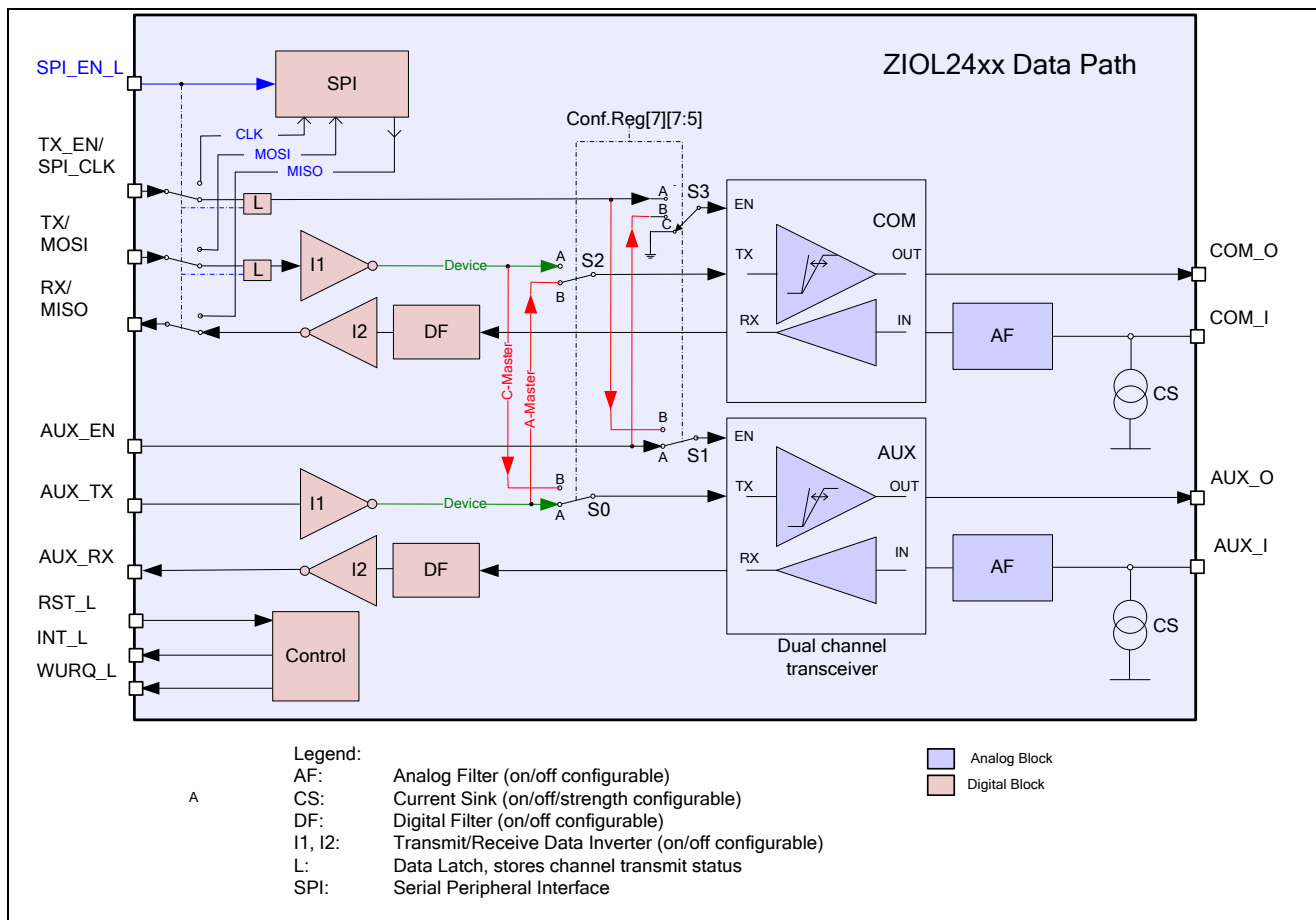
Maximum driver capability of minimum 500mA can be achieved by combining both drivers. In this case the drivers work in parallel (Tandem Mode).

In order to gain optimal EMC behavior the slew rate of the output signals of both drivers can be adjusted. The input threshold levels of the receiver can be set to ratiometric or to IO-Link conform levels, which enables the IC to be used in applications having a wide supply voltage range.

The configuration of the transceiver can be changed during operation. After power-on this configuration is automatically loaded from the on-chip EEPROM.

Driver and receiver are kept totally separated, so full duplex mode in data communication systems is supported. The ability to enable/disable the drivers output also enables applications in half duplex mode, where output and input are connected. Having the I/O-pins separated also enables additional external input filtering.

The COM channel send and receive signals (TX_EN, TX, RX) are multiplexed with the signals of the SPI functional unit of the IC (SPI_CLK, MOSI, MISO) as shown in Figure 3.2. The SPI unit is used for IC configuration and diagnostic purposes (refer to chapter 3.3.8). As long the SPI unit is active (SPI_EN_L = low), the send status of the COM channel is kept (for information refer to chapter 3.3.8 and Figure 3.10).

Figure 3.3   ZIOL22xx Transceiver Data Path in Principle
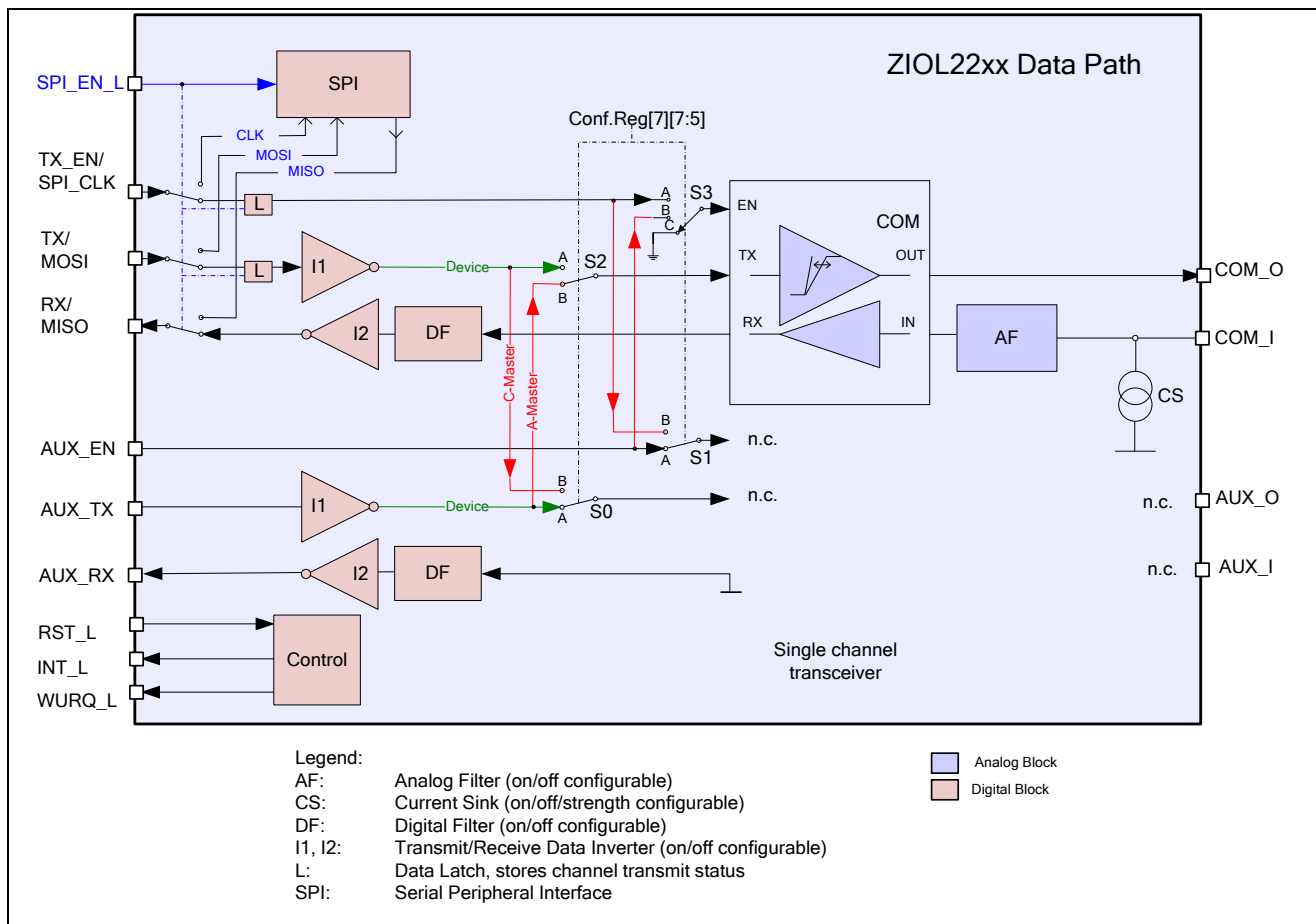
The (stripped down) IC versions ZIOL22xx/21xx contain only one channel. Figure 3.3 and Figure 3.4 show the data path of the ZIOL22xx versions and ZIOL21xx versions, respectively. The following chapters regarding details of the transmitter and receiver apply to IC versions with two channels (ZIOL24xx). The in the following described functionality applies to IC versions with one channel (ZIOL22xx/21xx) correspondingly. With the implicit understanding that one channel IC versions cannot perform tandem (master) mode operations or coordinated transceiver operations no explicit statement in the following chapters will reflect this.

Figure 3.4   ZIOL21xx Transceiver Data Path in Principle
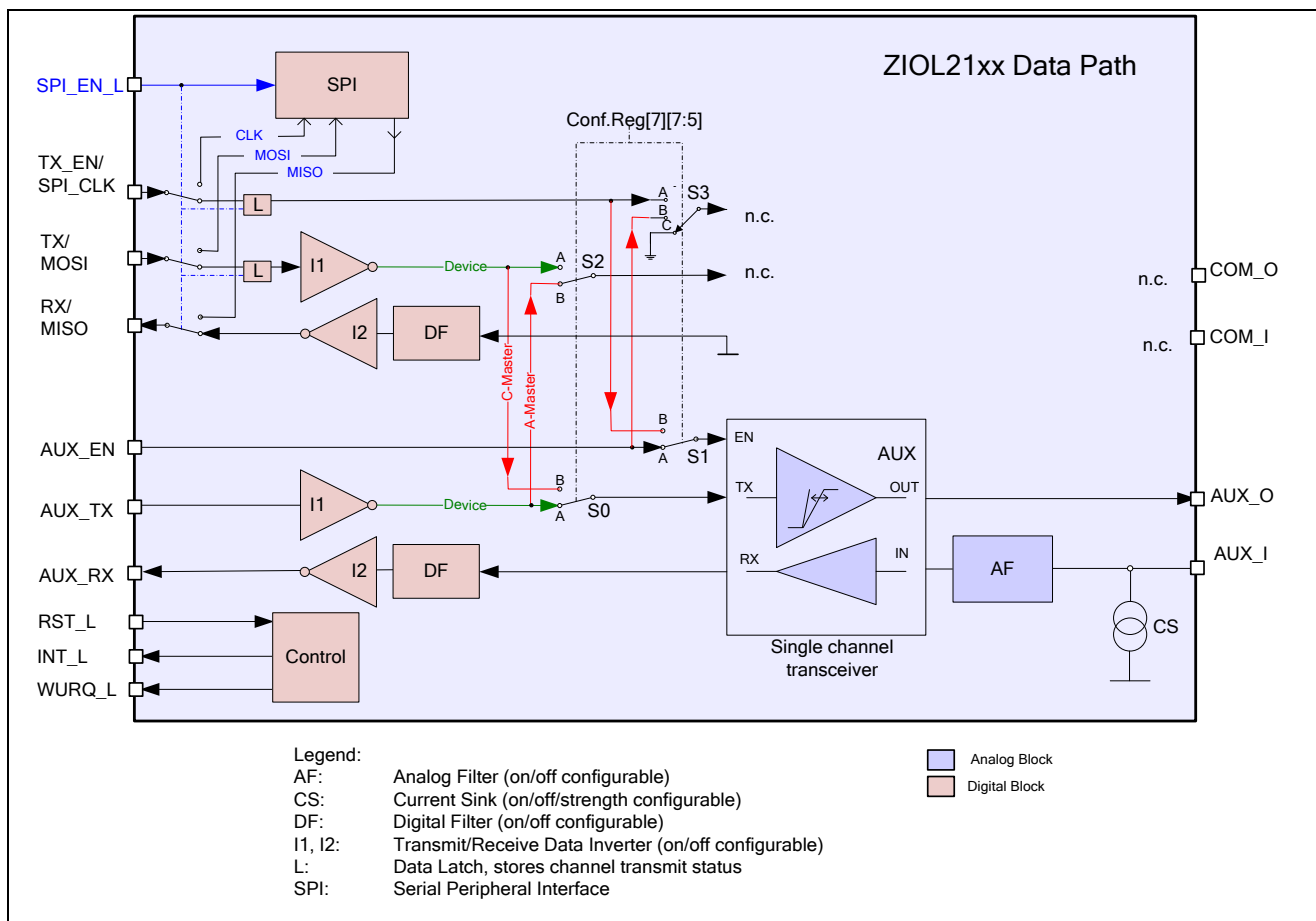
The master mode configuration flags MASTER_MODE, EN_FOLLOW_PRIM_CH and PRIMARY_MASTER_CH located in the MASTER_SENS_CTRL configuration register (refer to Table 3.7) control the switches S0, S1, S2 and S3 (Figure 3.2, Figure 3.3 and Figure 3.4) thus they control the actually used data path. In principle, the ZIOL2xxx IC family supports five data path types which are mentioned in Table 3.1. In case the MASTER_MODE flag is cleared (=0), the IC operates in device mode. For more information about the operation in device/master mode, please refer to chapter 3.2.2.1.

Table 3.1   Master-Device-Mode Function Table

Data Path Configuration		MASTER_SENS _CTRL[7:5] [7] = MASTER_MODE [6] = EN_FOLLOW_PRIM_CH [5] = PRIMARY_MASTER_CH	Data Path Switch Position				Receiver available [1]	RX/ MISO State control	REMARKS
Type	Global IC Function		S0	S1	S2	S3			
0	Device Mode	0 X X	A	A	A	A	COM[2] AUX	push/ pull	Equivalent to IC Rev A Device Mode
1	Master Mode, COM = prim channel, AUX enable not following prim-ch	1 0 0	B	A	A	A	COM[2] AUX	push/ pull	Equivalent to IC Rev A Master Mode
2	Master Mode, COM = prim channel, AUX enable is following prim-ch [1]	1 1 0	B	B	A	A	COM[2] AUX	push/ pull	Saves one interconnection wire (AUX_EN) to µC
3	Master Mode, AUX = prim channel, COM enable is following prim-ch [3]	1 1 1	A	A	B	B	AUX	push/ pull high-Z if SPI_EN_L = high	Process (IO-Link) and Service (SPI) data separation – SPI pin bus wiring!
4	Master Mode, AUX = prim channel, COM is disabled [4]	1 0 1	A	A	B	C			

[1] If AUX_EN is permanently wired to GND, the total driver strength can be controlled by toggling the MASTER_SENS_CTRL[6] bit (0: AUX disabled using just COM/ 1: AUX enabled if COM is enabled = double strength). → Switching between type 1 and 2 via SPI access.
[2] The logic value of the COM receiver output (RX) is available if the SPI communication is disabled (SPI_EN_L = 1).
[3] Driver strength is "double" – "WAKE_UP_MODE". The total driver strength can be decreased by switching to type 4 (single strength).
[4] Driver strength is "single". The total driver strength can be increased by switching to type 3 (double strength)

3.2.2. Transmitter

3.2.2.1. General functionality

The IC versions ZIOL24xx consists of two[1] independent driver stages. Each driver (COM/AUX) is configurable as regards the parameter

- Output current limitation
- Output slew rate
- Driver function (push, pull, pull ups/downs)

Several Modes of operation are supported – as independent or as combined driver outputs.

3.2.2.2. Modes of operation (IO-Link specific Operation)

Operating both on-chip drivers independently or in parallel ensures the IC utilization in a wide range of applications. An example can be the different requirements of driver capability in master or device mode regarding the IO-Link specification (refer also to chapter 3.3.2). Both modes are supported by the ZIOL2xxx Ics. The active mode is defined in the configuration register [7] bit 7. The chosen mode influences the IC's driver behavior as well as the handling of overload exceptions. Both input channels do not depend on the operational mode.

In master mode[2] the data inputs (TX) of both drivers are connected internally. As regards their functionality both drivers work in parallel. Therefore, the driver outputs have to be interconnected externally in master mode.

In device mode both drivers are working independently. A respective current overload signal will be generated if at one or at both drivers the output current exceeds the set current limit for longer than the configured amount of time.

Figure 3.5 shows a simplified application circuit including ZIOL24xx Ics in device and in master mode, respectively. Although both drivers are controlled by the same "TX" signal in master mode, the driver strength can be influenced with the COM_EN and AUX_EN signal thus the resulting driver strength can be reduced in this mode.

Starting with Rev B of the IC the MASTER_MODE flag (configuration register MASTER_SENS_CTRL[7] replaces the formerly used control via an input pin. Summarizing the above, the MASTER_MODE flag controls:

- The Data path; it controls whether both channels use an individual or common TX signal
- The current sinks at the receiver's inputs in the IO-Link sink mode (refer to Table 3.4)

For more information about the data path configuration of the IC in device and in mode master, please refer to chapter 3.2.1.

---

[1] Note: The IC versions ZIOL22xx/21xx have just one channel. With respect to those IC versions the statements concerning the existence of two channels shall be ignored or interpreted analogously.
[2] Not applicable for the IC versions ZIOL22xx/21xx

Figure 3.5   ZIOL24xx in Device and Master Mode Application
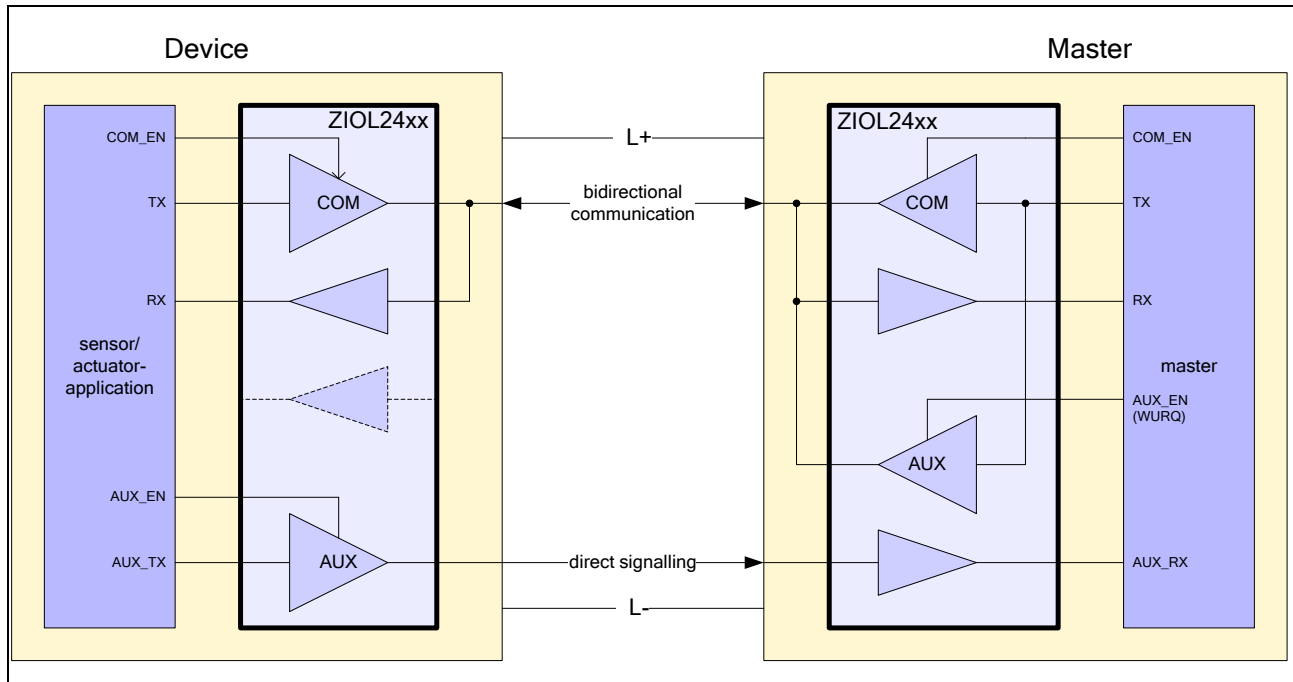
The illustration in Figure 3.5 shows the principal way of using the ZIOL2xxx integrated circuit in master and device mode. Figure 3.5 does not include all required electronic components of the application circuit which are mentioned in chapter 4 (Figure 4.1 and Figure 4.2).

3.2.2.3.   Configuration

The COM and AUX drivers are built identically. Their features can be configured in a wide range. The behavior of the output stages can be set to push, pull or push/pull. Current limitation and the overload timing can be set individually. In order to improve the EMC system behavior the slew rate of the output signal is controlled and can be set according to the needs of the application. The following table gives an overview of the possible configurations for the COM and AUX driver in master and device mode, respectively.

Table 3.2   Driver configurations

Parameter	Config.-Register	Reg.-Addr.	Bit-Field	Ranges & Coding		Unit	Remarks[1]
COM and AUX driver output current limitation	COM_PARAM, AUX_PARAM	2 4	4:2	0b000: 0b010: 0b100: 0b110: 0bxx1:	50 100 200 250 limitation off[2]	mA mA mA mA	IC in Device mode: both drivers work independently
Combined driver output current limitation	COM_PARAM, AUX_PARAM	2 4	4:2	0b000: 0b010: 0b100: 0b110: 0bxx1:	100 200 400 500 limitation off[2]	mA mA mA mA	IC in Master mode: both drivers work in parallel Both drivers shall be set to identical driver capability.
Slew Rate Control	COM_CTRL, AUX_CTRL	1 3	4:3	0b00: 0b10: 0b01: 0b11:	10 60 slow control off fast control off	V/µs V/µs	Limitation of maximal edge steepness. Limitation turned off! Limitation turned off!
Output characteristic	COM_CTRL, AUX_CTRL	1 3	1:0	0b00: 0b01: 0b10: 0b11:	off pull push push+pull		
Overload time base – COM, AUX	COM_MON_CTRL, AUX_MON_CTRL	11 13	6:5	0b00: 0b01: 0b10: 0b11:	0.2 1000 8000 16000	µs	Defines the clock frequency for COM/AUX overload counters
Overload counter compare value – COM, AUX	COM_ASSERT_TIME, AUX_ASSERT_TIME	10 12	7:0	Byte			If overload counter value equals compare value an overload will be asserted
Pull up/down enable – COM, AUX	COM_PARAM, AUX_PARAM	2 4	6:5	Bit 6: Bit 5:	pull-up pull-down		Enables resistor of typical 150kOhms
[1] For a summary of all configuration registers, please refer to Table 3.7. [2] Not recommended due to chance of overheating							

3.2.3.   Receiver

3.2.3.1.   General Functionality

In principle, the ZIOL2xxx IC family has two[1] identical input channels with a configurable feature set. The input threshold levels can be set ratiometric or absolute. The absolute values are compatible with definition of Type 1 digital inputs in IEC61131-2 and conform to the IO-Link specification. The ratiometric levels[2] are proportional to the HV power supply voltage. The ratiometric level configuration allows the input channels to function down to a

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[1] Note: The IC versions ZIOL22xx/21xx have only one receiver.
[2] Note: Ripple on the supply voltage may have influence to the trip-point of the input stage. Another influence to be considered is that an enabled analog input filter is reducing the ripple on the on the received signal.

supply voltage of 8V. For each input channel an analog and a digital filter are implemented, which can separately be enabled.

3.2.3.2. Configuration

The following table gives an overview of the possible configurations for the COM and AUX input channels.

Table 3.3   Receiver configurations

Parameter	Config.-Register	Reg.-Addr.	Bit-Field	Setting / Range		Unit	Remarks[1]
Threshold level for COM and AUX	COM_CTRL, AUX_CTRL	1 3	5	0b0: 0b1:	absolute ratiometric		Absolute = IO-Link compliant thresholds
Analogue filter	COM_CTRL, AUX_CTRL	1 3	2	0b0: 0b1:	disabled enabled		
Digital filter	COM_CTRL, AUX_CTRL	1 3	7	0b0: 0b1:	disabled enabled		
I_{sink}, sink strength	COM_PARAM, AUX_PARAM	2 4	7	0b0: 0b1:	2 – 3 5 – 7	mA	
Sink mode	COM_PARAM, AUX_PARAM	2 4	1:0	0b00: 0b01: 0b10: 0b11:	off IO-Link follow driver on		Following driver: if driver is enabled then sink = off if driver is disabled then sink = on

[1] For a summary of all configuration registers, please refer to Table 3.7.

3.2.3.3. Sink Modes

The IO-Link standard defines a possible configuration option, in which the device drives the signal line only with a high side driver thus the logic low level will be generated with a current sink on the master side (Figure 3.6). The ZIOL2xxx supports the current sinks in different modes on master side (for details refer to Table 3.4).

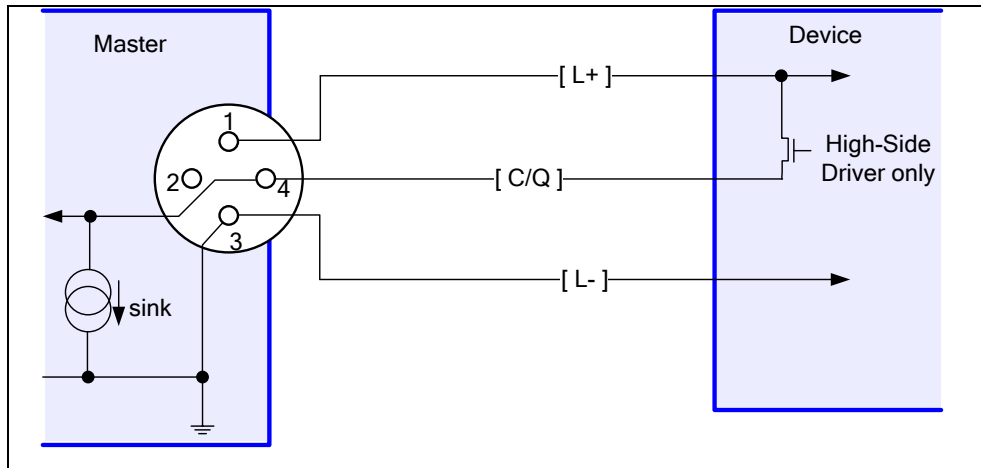*Figure 3.6   Typical IO-Link Device Configuration with HS driver only*

Table 3.4   Sink Mode Configuration in Detail

Register[2][1:0] Register[4][1:0]	Mode	Sink enabling	Remark
00	n.a.	Sink steady disabled	OFF
01	Device Mode [1]	Sink steady disabled	Typical application mode for the IO-Link channel: **device**: no sink **master**: sink enabled contrary to the corresponding driver enable signal
	Master Mode [2]	Sink enabled if: • TX_EN/SPI_CLK = low (COM) • AUX_EN = low (AUX)	
10	n.a.	Sink enabled if: • TX_EN/SPI_CLK = low (COM) • AUX_EN = low (AUX)	Enabling contrary to the driver enable signal; sink is only enabled while the driver is disabled. (helps to reduce the system's power dissipation)
11	n.a.	steady enabled	ON

[1] MASTER_MODE flag (configuration register MASTER_SENS_CTRL[7] is cleared (=0).
[2] MASTER_MODE flag (configuration register MASTER_SENS_CTRL[7] is set (=1).

3.3.   System Control

3.3.1.   General

The system control provides device configuration, status signaling and SPI data transfer functionality. Implemented are several register areas which contain configuration data and which provide status information. In order to gain read/write access to these register areas, the standard serial peripheral interface (SPI) is implemented. Since the pin count of the package is limited to 24 pins, the SPI specific pins (CLK, MOSI, and MISO) are multiplexed with IO-pins of the COM driver. A dedicated pin SPI_EN_L is used to switch between SPI

(logic low) and COM transceiver functionality (logic high). The low voltage (LV) interface works with 3.3V supply voltage (refer to Figure 3.1). The LV outputs drive 3.3V as high level, the inputs are 5V tolerant.

If the SPI communication channel of the ZIOL2xxx Ics is active (SPI_EN_L = low), the status of the COM channel drivers is kept. This means while SPI_EN_L = low the output driver status (driving low, driving high, or high-z) is the same as defined by the pins TX_EN/SPI_CLK and TX/MOSI at the point of time of the SPI_EN_L high-low transition. The AUX channel is not affected by the activity of the SPI communication. For more information, please refer to chapter 3.3.8 and Figure 3.10.

3.3.2. IO-Link Master[1] and Device Mode

The IC architecture is suitable for both IO-Link application cases, the physical layer transceiver at an IO-Link master port and at an IO-Link device port. In the first case the IC shall operate in its "master mode" which is the case if configuration register [7] bit 7 is set (=1). If the IC shall operate in "device mode", configuration register [7] bit 7 shall be cleared (=0). Details regarding the control of both driver channels are described in chapter 3.2.1, 3.2.2.2 and 3.2.3.3.

The IO-Link specific WURQ detection (detection of an IO-Link master's wake-up request, refer to IO-Link Communication Specification – chapter 8, [2]) works only in device mode.

3.3.3. Internal Exceptions

Depending on the IC configuration the ZIOL2xxx can detect several critical situations and rise internal exceptions accordingly. Also depending on the IC configuration an occurred internal exception can be indicated externally by changing the logic level of the INT-L pin to "low". The situations that cause an internal exception are channel locks (channel driver protection), detected IO-Link specific Wake-Up pulses and several issues concerning the internal EEPROM as described in chapter 3.3.10.

3.3.4. IO-Link specific Wake-Up (WURQ)

In device mode the IC can detect the IO-Link specific wake-up request (WURQ) of the IO-Link master and can therefore help to save resources in the microcontroller of IO-Link device. As regards the IO-Link specific "Wake-Up (WURQ)" specification, please refer to the IO-Link Communication Specification issued by the IO-Link consortium (refer to chapter 8, [2]).

The WURQ can be detected on the COM or on the AUX channel. The chosen channel is defined in a configuration register (IRQ_WURQ_CTRL, refer to chapter 3.3.9).

In order to establish an IO-Link specific communication, the master will generate the WURQ event. In this case the master overdrives the devices output level for a determined period. The ZIOL2xxx can detect that event which physically occurs in two ways:

- A current overload in the drivers output for a certain period
- A contradiction of the TX and RX lines of the device for a certain period

The IC configuration register (IRQ_WURQ_CTRL, refer to chapter 3.3.9) defines if the "overload" or the "contradiction" or both events shall be chosen for the WURQ detection. Both ways of detection can be enabled

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[1] Not applicable for the IC versions ZIOL22xx/21xx.

independently. If at least one of both events appears for a specific time, the incident will be regarded as WURQ request from master side and the IC will generate an internal exception (issue an interrupt) in order to signal this to the interconnected µC. Besides the configurable signaling on the INT_L pin (refer to chapter 3.3.10.1) this special exception will be displayed on the therefore dedicated WURQ_L pin. Details of the signaling via the WURQ_L and/or the INT_L pin and the pin driver configuration of the WURQ_L pin can be defined in the configuration registers which are described in detail in chapter 3.3.9.

The logic level of the WURQ_L pin (a wake-up causes logic low) or the stored WURQ event will be reset as soon as the drivers direction is set to input (TX_EN=0), which equals the WURQ acknowledge from the IO-Link device side.

The on logic level based WURQ detection works only for level-changes which are driven by the master. That means a WURQ will not be detected if a level change has been initiated by the device itself, even if the signal timing is equivalent to a WURQ event. This prevents the in SIO mode operating IO-Link device to misinterpret the situation caused for instance by capacitive loads.

If the ZIOL2xxx operates in master mode (physical interface for IO-Link master port) and a Wake-Up pulse (WURQ) shall be issued, the µC has to control the required driver strength by activating both channels (via COM_EN and AUX_EN, refer to Figure 3.5) and has to provide the correct timing.

Figure 3.7   Wake-Up Signal Recognition
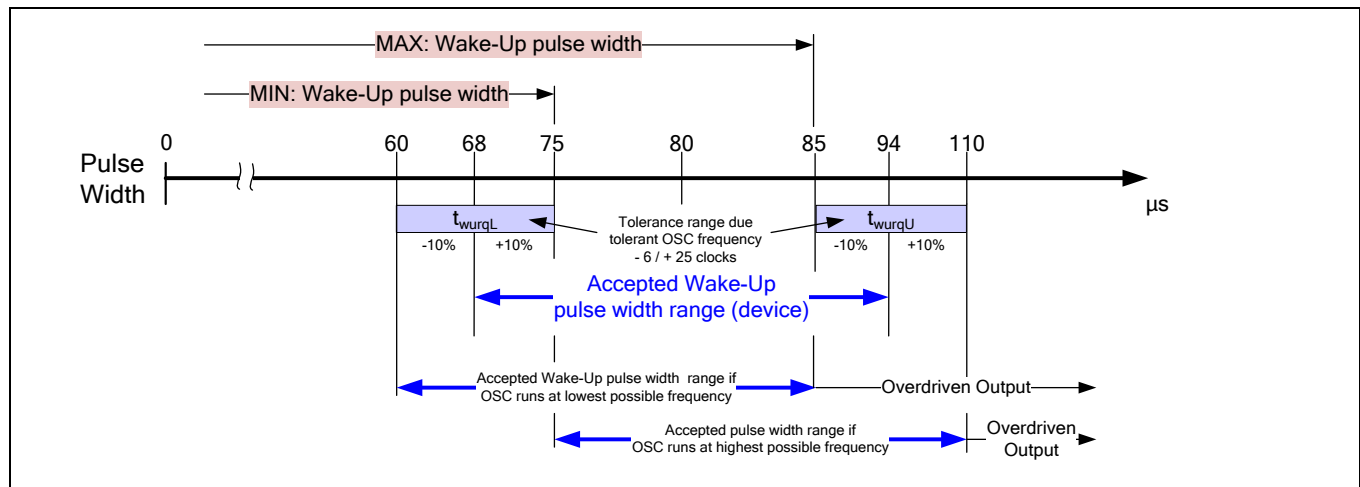
The WURQ pulse recognition of the ZIOL2xxx in device mode is – in contrast to that – based on a time base derived from the internal oscillator (OSC). Therefore the as WURQ recognized pulse width range of an received Wake-Up signal is dependent on the frequency tolerance of the internal oscillator as illustrated in Figure 3.7. A Wake-Up signal (pulse width according to the IO-Link Communication Specification, refer to chapter 8, [2]) shall have a pulse width between 75µs and 85µs (variation 10µs). The ZIOL2xxx Wake-Up signal detection will always recognize such a signal securely considering a frequency tolerance of the internal oscillator of ±10% (refer to parameter f_{osc} in Table 2.3).

3.3.5. IC Self-Protection – Lock Mode

In order to prevent serious IC damage due to overloaded or overheated driver transistors, the IC has a build-in protection mechanism. If a critical situation occurs for a certain configurable time, the IC can protect itself in transferring its control in a special mode, called lock mode, in which the driver of the related channel is turned-off in case of over-current, or in case of over-temperature the drivers of both channels are turned-off, respectively.

Figure 3.8 shows the basic scheme of the IC self protection. In principle, this scheme is five times implemented in order to tread:

- Over-current situations separately at the high side and at the low side switch of the COM channel as described in Figure 3.15
- Over-current situations separately at the high side and at the low side switch of the AUX channel as described in Figure 3.16
- Over-temperature situations of the silicon die as described in Figure 3.17

In case of an over-current or over-temperature situation occurs (in the following called overload) the related over-current/over-temperature counter (overload counter) will count up. Since the overload counter counts down to zero in case of no overload is existent, the circuit performs an integrator function. This integrator function makes sure that overloads which temporarily occur are not accumulated thus will not lead to an unwanted driver locks.

If the overload counter has reached the (in the related configuration register) defined maximum value, the IC will generate an internal exception. This exception will lock the associated channel or both channels in case of an over-temperature situation. The "assert Time" (refer to Figure 3.8) which is the elapsed time in until reaching the configured maximum of the overload counter depends on the used clock period for the overload counter. This clock period can be defined separately for the lock control circuit of each channel (Figure 3.15, Figure 3.16) and the temperature lock control circuit (Figure 3.17) in the associated configuration register.

To each overload counter is a peak register associated. The value of the overload counters can not be retrieved via the SPI port. However, the value of the overload counter will be copied in the related peak register if the value of the overload counter is greater than the value of the peak register. The peak registers can be read via the SPI port. The content of the peak register will be cleared after each read access. However, within the next cycle of the IC control circuit the peak register will be set to the overload counter value again if this value is greater than zero.

The above described peak register update is only performed if an overload situation is present. In case of overload situation the peak register is an important instrument to perform an IC diagnostic. For more information about techniques to operate the peak, please refer to Appendix A.

A due to an overload raised internal exception will cause in case of over-current a lock of the related channel or a lock of both channels in case of a over-temperature situation. There are three signals (displayed in status register[20] which indicate the lock activator. The other five bits of this status register indicate what IC sensor has detected an over-current or if the configured maximum of the die temperature has been exceeded.