Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

intersil | Zilker Labs
Data Sheet December 16, 2011 FN6849.3

NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ZL6100

Digital-DC™ Controller with Drivers and POLA/DOSA Trim

Description

The ZL2005P is an innovative mixed-signal power conversion and management IC that combines a compact, efficient, synchronous DC-DC buck controller, adaptive drivers and key power and thermal management functions in one IC, providing flexibility and scalability while decreasing board space requirements and design complexity. Zilker Labs Digital-DC technology enables a unique blend of performance and features not available in either traditional analog or newer digital approaches, resolving the issues associated with providing multiple low-voltage power domains on a single PCB.

The ZL2005P is designed to be configured either as a standard ZL2005 or as POLA/DOSA compatible device.

All operating features can be configured by simple pin-strap selection, resistor selection or through the on-board serial port. The PMBus™-compliant ZL2005P uses the SMBus™ serial interface for communication with other Digital-DC products or a host controller.

Features Power Conversion

- Efficient synchronous buck controller
- 3 V to 14 V input range
- 0.54 V to 5.5 V output range (with margin)
- Optional output voltage setting with VADJ pin
- ± 1% output accuracy
- Internal 3 A drivers support >40 A power stage
- Fast load transient response
- Phase interleaving
- RoHS compliant (6 x 6 mm) QFN package

Power Management

- Digital soft start/stop
- Precision delay and ramp-up
- Voltage tracking, sequencing and margining
- Voltage/current/temperature monitoring
- I^2C/SMBus communication
- Output overvoltage and overcurrent protection
- Internal non-voltatile memory (NVM)
- PMBus compliant

Applications

- Servers/storage equipment
- Telecom/datacom equipment
- Power supplies (memory, DSP, ASIC, FPGA)

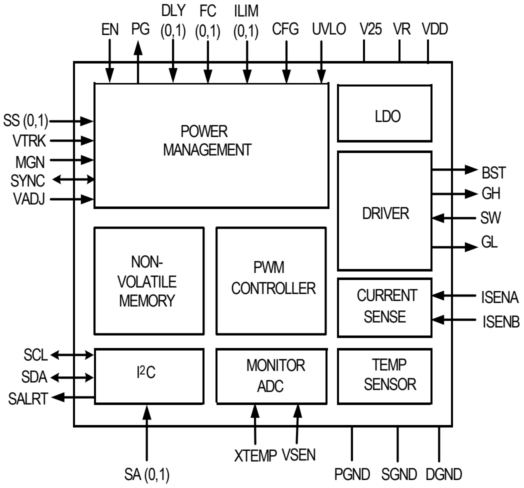


Figure 1. Block Diagram

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Copyright Intersil Americas Inc. 2009-2011. All Rights Reserved
Intersil (and design) is a trademark owned by Intersil Corporation or one of its subsidiaries.
All other trademarks mentioned are the property of their respective owners.

Table of Contents

1 Electrical Characteristics

Table 1. Absolute Maximum Ratings

Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty. Unless otherwise specified, all voltages are measured with respect to SGND.

Parameter	Pin(s)	Value	Unit
DC supply voltage	VDD	-0.3 to 17	V
Logic I/O voltage	DLY(0,1), EN, ILIM(0,1), MGN, PG, SA(0,1), SALRT, SCL, SDA, SS(0,1), SYNC, VADJ, UVLO, V(0,1)	-0.3 to 6.5	V
Analog input voltages	ISENB, VSEN, VTRK, ISENA, XTEMP	-0.3 to 6.5	V
MOSFET drive reference	VR	-0.3 to 6.5	V
Logic reference	V25	-0.3 to 3	V
High-side supply voltage	BST	-0.3 to +30	V
High-side drive voltage	GH	(V_{SW} - 0.3) to (V_{BST}+0.3)	V
Low-side drive voltage	GL	(PGND-0.3) to (VR+0.3+PGND)	V
Boost to switch differential voltage (V_{BST} - V_{SW})	BST, SW	-0.3 to 8	V
Switch node continuous	SW	(PGND-0.3) to 30	V
Switch node transient (<100 ns)	SW	(PGND-5) to 30	V
Ground voltage differential (V_{DGND}-V_{SGND}), (V_{PGND}-V_{SGND})	DGND, SGND, PGND	-0.3 to +0.3	V
Junction temperature	–	-55 to 150	^oC
Storage temperature range	–	-55 to 150	^oC
Lead temperature (soldering, 10s)	–	300	^oC

Table 2. Recommended Operating Conditions and Thermal Information

Parameter	Symbol	Min	Typ	Max	Unit
Input Supply Voltage Range, V_{DD}	V_R tied to V_{DD} (Figure 9)	3.0	–	5.5	V
	V_R floating (Figure 9)	4.5	–	14	V
Output Voltage Range	V_{OUT} (RDSON sensing)	0.54		5.5	V
Output Voltage Range	V_{OUT} (DCR sensing)	0.6		3.6^3	V
Operating Junction Temperature Range	T_J	-40	–	125	°C
Junction to Ambient Thermal Impedance[1]	Θ_{JA}	–	35	–	°C/W
Junction to Case Thermal Impedance[2]	Θ_{JC}	–	5	–	°C/W

NOTES:

1. Θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For Θ_{JC}, the "case" temperature is measured at the center of the exposed metal pad.
3. With margin

Table 3. Electrical Specifications Unless otherwise specified V_{DD} = 12 V, T_A = -40°C to +85°C. Typical values are at T_A = 25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

Parameter	Condition	Min (Note 6)	Typ	Max (Note 6)	Unit
Input and Supply Characteristics					
Supply current (I_{DD}) (No load on GH and GL)	f_{SW} = 200 kHz	–	16	**30**	mA
	f_{SW} = 1,000 kHz	–	25	**50**	mA
Standby supply current (I_{DD})	EN = Low no I^2C/SMBus activity	–	2	**5**	mA
VR reference voltage (V_R)	$V_{DD} \geq 6$ V $I_{VR} < 50$ mA	**4.5**	5.2	**5.5**	V
V25 reference voltage (V_{25})	$V_R \geq 3$ V $I_{V25} < 50$ mA	**2.25**	2.5	**2.75**	V
Output Characteristics					
Output voltage adjustment range		**0.6**	–	**5.5**	V
Output voltage setpoint resolution	Set using resistors on V(0,1) Set using resistor on VADJ	–	10 Table 8	–	mV
	Set using I^2C/SMBus	–	±0.025	–	% of F.S.[1]
Output voltage accuracy	Over line and load	**-1**		**1**	%
VSEN input bias current	VSEN = 5.5 V	**–**	110	**200**	µA
Current sense differential input voltage (ground referenced)	$V_{ISENA} - V_{ISENB}$	**-100**	–	**100**	mV
Current sense differential input voltage (V_{OUT} referenced)	$V_{ISENA} - V_{ISENB}$	**-50**	–	**50**	mV
Current sense input bias current	Ground referenced	**-100**	–	**100**	µA
Current sense input bias current (V_{OUT} referenced, V_{OUT} <= 3.6V)	ISENA	**-1**	–	**1**	µA
	ISENB	**-100**	–	**100**	µA
Soft start delay duration range[5]	Configurable via I^2C/SMBus	**0.007**	–	**500**	s

Table 3. Electrical Specifications Unless otherwise specified V_{DD} = 12 V, T_A = -40°C to +85°C. Typical values are at T_A = 25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.** (Continued)

Parameter	Condition	Min (Note 6)	Typ	Max (Note 6)	Unit
Soft start delay duration accuracy		–	6	–	ms
Soft start ramp duration range[5]	Configurable via I^2C/SMBus	**0**	–	**200**	ms
Soft start ramp duration accuracy		–	100	–	μs
Logic Input/Output Characteristics					
Logic input leakage current	Push-pull logic	**-250**	–	**250**	nA
Logic input low threshold (V_{IL})		–	–	**0.8**	V
Logic input OPEN (N/C)	Multi-mode logic pins	–	1.4	–	V
Logic input high threshold (V_{IH})		**2**	–	–	V
Logic output low (V_{OL})	I_{OL} <= 4 mA	–	–	**0.4**	V
Logic output high (V_{OH})	I_{OH} >= - 2 mA	**2.25**	–	–	V
Oscillator and Switching Characteristics					
Switching frequency range		**200**	–	**1400**	kHz
Switching frequency setpoint accuracy	Predefined settings (See Table 13)	**-5**	–	**5**	%
Maximum PWM duty cycle	Factory default	**95**	–	–	%
Minimum SYNC pulse width[5]		**150**	–	–	ns
Input clock frequency drift tolerance	External clock signal	**-13**	–	**13**	%
Gate Drivers					
High-side driver voltage (V_{BST} - V_{SW})		–	4.5	–	V
High-side driver peak gate drive current (pull down)[5]	(V_{BST} - V_{SW}) = 4.5 V	**2**	3	–	A
High-side driver pull-up resistance[5]	(V_{BST} - V_{SW}) = 4.5 V, (V_{BST} - V_{GH}) = 50 mV	–	0.8	**2**	Ω
High-side driver pull-down resistance[5]	(V_{BST} - V_{SW}) = 4.5 V, (V_{GH} - V_{SW}) = 50 mV	–	0.5	**2**	Ω
Low-side driver peak gate drive current (pull-up)[5]	V_R = 5 V	–	2.5	–	A
Low-side driver peak gate drive current (pull-down)[5]	V_R = 5 V	–	1.8	–	A
Low-side driver pull-up resistance[5]	V_R = 5 V, (V_R - V_{GL}) = 50 mV	–	1.2	**2**	Ω
Low-side driver pull-down resistance[5]	V_R = 5 V, (V_{GL} - PGND) = 50 mV	–	0.5	**2**	Ω
Switching timing					
GH rise and fall time[5]	(V_{BST} - V_{SW}) = 4.5 V, C_{LOAD} = 2.2 nF	–	5	**20**	ns
GL rise and fall time[5]	V_R = 5 V, C_{LOAD} = 2.2 nF	–	5	**20**	ns
Tracking					
VTRK input bias current	VTRK = 5.5 V	–	110	**200**	μA

Table 3. Electrical Specifications Unless otherwise specified V_{DD} = 12 V, T_A = -40°C to +85°C. Typical values are at T_A = 25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.** (Continued)

Parameter	Condition	Min (Note 6)	Typ	Max (Note 6)	Unit
VTRK tracking threshold[5]	VTRK >= 0.3 V	**– 100**		**100**	mV
Fault Protection Characteristics					
UVLO threshold range		**2.85**	–	**16**	V
UVLO setpoint accuracy	ZL2005P configuration	**-3**	–	**3**	%
UVLO hysteresis	Factory default	–	3	–	%
	Configurable via I^2C/SMBus	**0**	–	**100**	%
UVLO delay		–	–	**2.5**	µs
Power good V_{OUT} low threshold	Factory default	–	90	–	% V_{OUT}
Power good V_{OUT} high threshold	Factory default	–	115	–	% V_{OUT}
Power good V_{OUT} hysteresis	Factory default	–	5	–	%
Power good delay range[5]	Configurable via I^2C/SMBus	**0**	–	**500**	s
VSEN undervoltage threshold	Factory default		85	–	% V_{OUT}
	Configurable via I^2C/SMBus[5]	**0**	–	**110**	% V_{OUT}
VSEN overvoltage threshold	Factory default		115	–	% V_{OUT}
	Configurable via I^2C/SMBus[5]	**0**	–	**115**	% V_{OUT}
VSEN undervoltage/overvoltage fault response time	Factory default	–	16	–	µs
	Configurable via I^2C/SMBus[5]	**5**	–	**60**	µs
Current limit setpoint accuracy (V_{OUT} referenced)		–	±10	–	% F.S.[1]
Current limit setpoint accuracy[2] (Ground referenced)	$\lvert V_{ISENA} - V_{ISENB} \rvert > 12$ mV	–	±10	–	% F.S.
Current limit protection delay	Factory default	–	5	–	t_{SW}[3]
	Configurable via I^2C/SMBus[5]	**1**	–	**32**	
Temperature compensation of current limit protection threshold	Factory default	–	4400	–	ppm/°C
	Configurable via I^2C/SMBus[5]	**100**	–	**12700**	
Thermal protection threshold	Factory default	–	125	–	°C
	Configurable via I^2C/SMBus[5]	**- 40**	–	**125**	°C
Thermal protection hysteresis		–	15	–	°C

NOTES:

1. Percentage of Full Scale (F.S.) with temperature compensation applied.
2. T_A = 0°C to +85°C
3. $t_{SW} = 1/f_{SW}$, f_{SW} switching frequency
4. Automatically set to same value as soft start ramp time.
5. Limits established by characterization and not production tested.
6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

2 Pin Descriptions

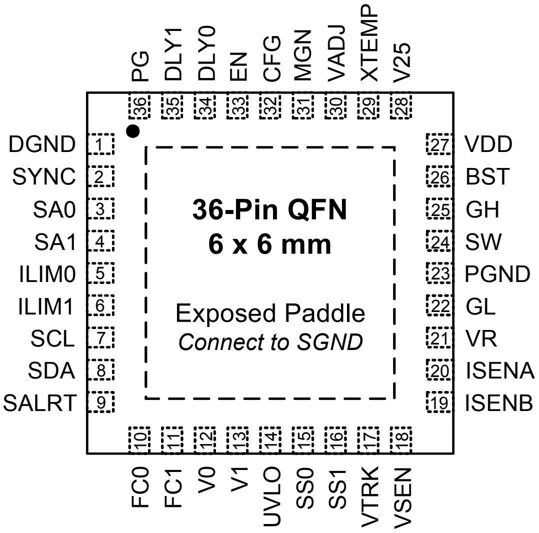


Figure 2. Pin Assignments (top view)

Table 4. Pin Descriptions

Pin	Label	Type[1]	Description
1	DGND	PWR	Digital ground. Connect to low impedance ground plane.
2	SYNC	I/O, M[2]	Clock synchronization input. Used to set the frequency of the internal switch clock, to sync to an external clock or to output internal clock.
3	SA0	I, M	Serial address select pins. Used to assign unique address for each individual device or to enable certain management features.
4	SA1		
5	ILIM0	I, M	Current limit select. Sets the overcurrent threshold voltage for ISENA, ISENB.
6	ILIM1		
7	SCL	I/O	Serial clock. Connect to external host and/or to other ZL2005s.
8	SDA	I/O	Serial data. Connect to external host and/or to other ZL2005s.
9	SALRT	O	Serial alert. Connect to external host if desired.
10	FC0	I	Loop compensation selection pins.
11	FC1	I	
12	V0	I, M	Output voltage selection pins. Used to set V_{OUT} setpoint and V_{OUT} max.
13	V1		
14	UVLO	I, M	Undervoltage lockout selection. Sets the minimum value for V_{DD} voltage to enable V_{OUT}.
15	SS0	I, M	Soft start pins. Set the output voltage ramp time during turn-on and turn-off.
16	SS1		
17	VTRK	I	Tracking sense input. Used to track an external voltage source.

NOTES:

1. I = Input, O = Output, PWR = Power or Ground, M = Multi-mode pin (refer to Section 4.5, “Multi-mode Pins,”)
2. The SYNC pin can be used as a logic pin, a clock input or a clock output.
3. V_{DD} is measured internally and the value is used to modify the PWM loop gain.

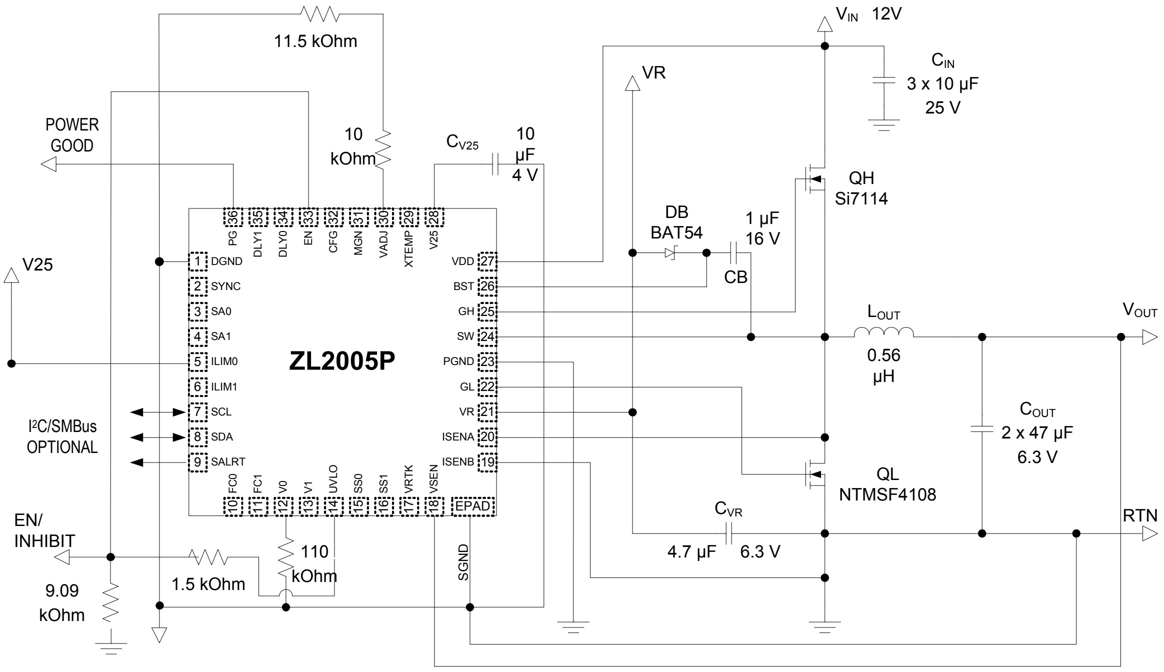
Table 4. Pin Descriptions (Continued)

Pin	Label	Type[1]	Description
18	VSEN	I	Output voltage feedback. Connect to output regulation point.
19	ISENB	I	Differential voltage input for current limit.
20	ISENA	I	Differential voltage input for current limit. High voltage tolerant.
21	VR	PWR	Internal 5V reference used to power internal drivers.
22	GL	O	Low side FET gate drive.
23	PGND	PWR	Power ground. Connect to low impedance ground plane.
24	SW	PWR	Drive train switch node.
25	GH	O	High-side FET gate drive.
26	BST	PWR	High-side drive boost voltage.
27	VDD[3]	PWR	Supply voltage.
28	V25	PWR	Internal 2.5 V reference used to power internal circuitry.
29	XTEMP	I	External temperature sensor input. Connect to external 2N3904 diode connected transistor.
30	VADJ	I	Output voltage setting pin (POLA/DOSA mapping)
31	MGN	I	Digital V_{OUT} margin control
32	CFG	I	Configuration pin. Used to control the switching phase offset, sequencing and other management features.
33	EN	I	Enable. Active signal enables PWM switching.
34	DLY0	I, M	Softstart delay select. Sets the delay from when EN is asserted until the output voltage starts to ramp.
35	DLY1		
36	PG	O	Power good output.
ePad	SGND	PWR	Exposed thermal pad. Connect to low impedance ground plane. Internal connection to SGND.

NOTES:

1. I = Input, O = Output, PWR = Power or Ground, M = Multi-mode pin (refer to Section 4.5, “Multi-mode Pins,”)
2. The SYNC pin can be used as a logic pin, a clock input or a clock output.
3. V_{DD} is measured internally and the value is used to modify the PWM loop gain.

3 Typical Application Example



Notes:

1. Conditions: V_{IN} = 12 V, V_{OUT} = 1.2 V, Freq = 400 kHz, I_{OUT} = 20 A
2. The I^2C/SMBus requires pullup resistors. Please refer to the I^2C/SMBus specifications for more details.

Figure 3. Typical Application Circuit POLA

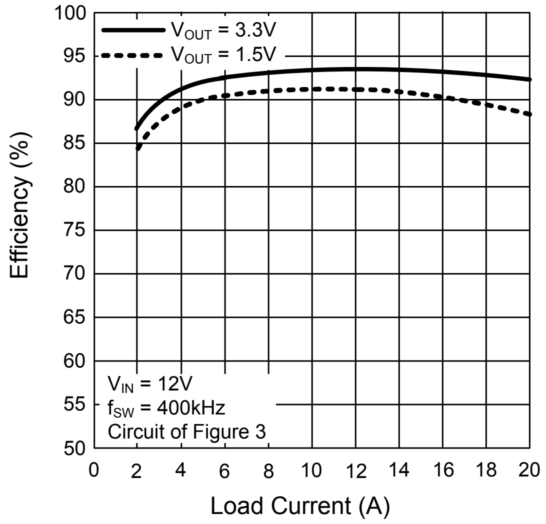


Figure 4. Typical Efficiency Curves

4 ZL2005P Overview

4.1 Digital-DC Architecture

The ZL2005P is an innovative mixed-signal power conversion and power management IC based on Zilker Labs' patented Digital-DC technology that provides an integrated, high performance step-down converter for a wide variety of power supply applications. Its unique digital PWM loop utilizes an innovative mixed-signal topology to enable precise control of the power conversion process with no software required, resulting in a very flexible device that is also easy to use. An extensive set of power management functions is fully integrated and can be configured using simple pin connections or via the I^2C/SMBus hardware interface using standard PMBus commands. The user configuration can be saved in an on-chip non-volatile memory (NVM), allowing ultimate flexibility.

Once enabled, the ZL2005P is immediately ready to regulate power and perform power management tasks with no programming required. The ZL2005P can be configured by simply connecting its pins according to the tables provided in this document. Advanced configuration options and real-time configuration changes are available via the I^2C/SMBus interface if desired, and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated sub-regulation circuitry enables single supply operation from any supply between 3V and 14V with no secondary bias supplies needed.

Zilker Labs provides a comprehensive set of on-line tools and application notes to assist with power supply design and simulation. An evaluation board is also available to help the user become familiar with the device. This board can be evaluated as a stand-alone platform using pin configuration settings. Additionally, a Windows™-based GUI is provided to enable full configuration and monitoring capability via the I^2C/SMBus interface using an available computer and the included USB cable.

Please refer to www.intersil.com/zilkerlabs/ for access to the most up-to-date documentation and the PowerPilot™ simulation tool, or call your local Zilker Labs' sales office to order an evaluation kit.

4.2 ZL2005 - ZL2005P

By default, the ZL2005P is configured as a standard ZL2005 device.

The main differences between the ZL2005P configured as a ZL2005P and the initial ZL2005 are the following:

- TACH pin is not used (reserved for ZL2005P POLA configuration).
- VADJ pin to adjust voltage through an external resistor, similar to POLA method.
- Additional configuration option for Synchronization.
- DEFAULT STORE only

4.3 Power Conversion Overview

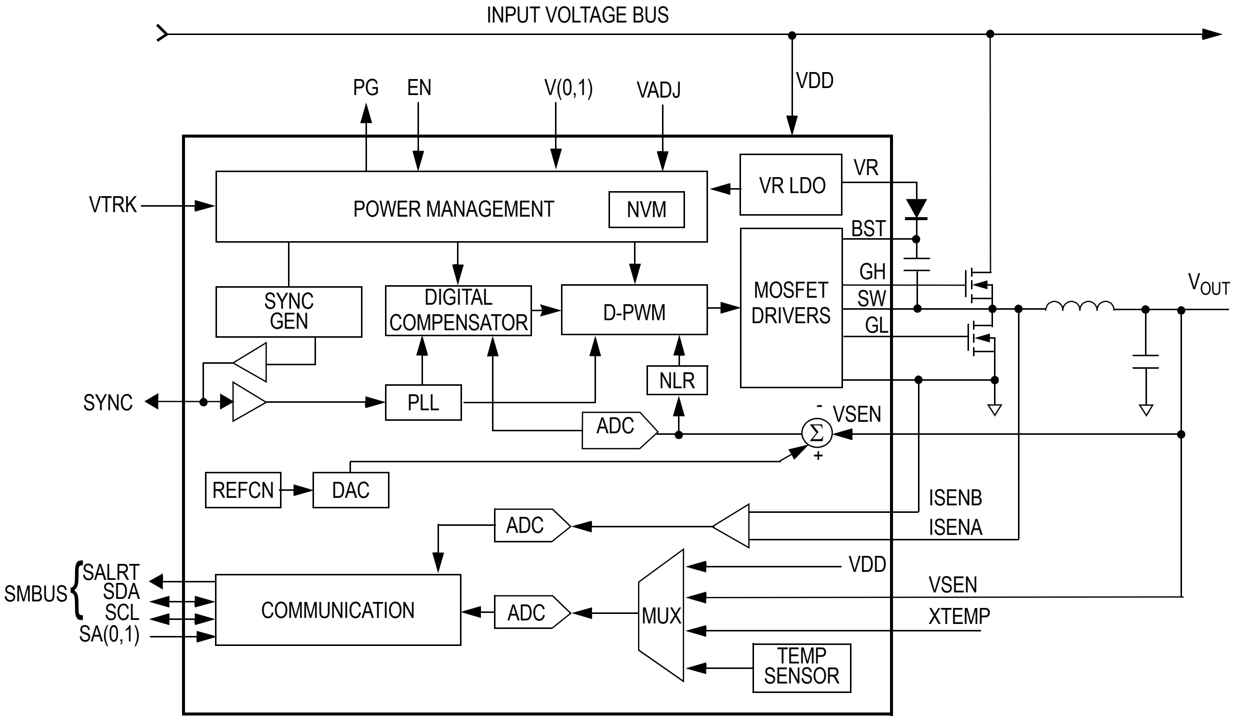


Figure 5. ZL2005P Detailed Block Diagram

The ZL2005P operates as a voltage-mode, synchronous buck converter with a selectable, constant frequency Pulse Width Modulator (PWM) control scheme that uses external MOSFETs, inductor and capacitors to perform power conversion.

Figure 6 illustrates the basic synchronous buck converter topology showing the primary power train components. This converter is also called a step-down converter, as the output voltage must always be lower than the input voltage.

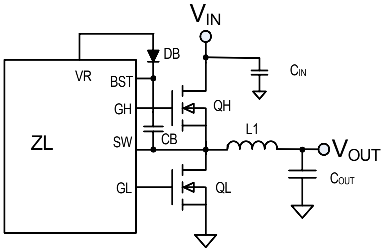


Figure 6. Synchronous Buck Converter

In its most simple configuration, the ZL2005P requires two external N-channel power MOSFETs, one for the top control MOSFET (QH) and one for the bottom synchronous MOSFET (QL). The amount of time that QH is on as a fraction of the total switching period is known as the duty cycle *D*, which is described by the following equation:

$$D \approx \frac{VOUT}{VIN}$$

During time D, QH is on and $V_{IN} - V_{OUT}$ is applied across the inductor. The current ramps up as shown in Figure 7.

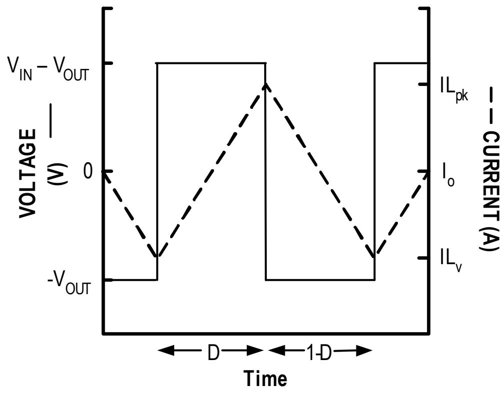


Figure 7. Inductor Waveform

When QH turns off (time 1-D), the current flowing in the inductor must continue to flow from the ground up through QL, during which the current ramps down. Since the output capacitor C_{OUT} exhibits a low impedance at the switching frequency, the AC component of the inductor current is filtered from the output voltage so the load sees nearly a DC voltage.

Typically, buck converters specify a maximum duty cycle that effectively limits the maximum output voltage that can be realized for a given input voltage. This duty cycle limit ensures that the low-side MOSFET is allowed to turn on for a minimum amount of time during each switching cycle, which enables the bootstrap capacitor (CB in Figure 6) to be charged up and provide adequate gate drive voltage for the high-side MOSFET. See Section 5.2, “High-side Driver Boost Circuit,” for more details.

In general, the size of components L1 and C_{OUT} as well as the overall efficiency of the circuit are inversely proportional to the switching frequency, f_{SW}. Therefore, the highest efficiency circuit may be realized by switching the MOSFETs at the lowest possible frequency; however, this will result in the largest component size. Conversely, the smallest possible footprint may be realized by switching at the fastest possible frequency but this gives a somewhat lower efficiency. Each user should determine the optimal combination of size and efficiency when determining the switching frequency for each application.

The block diagram for the ZL2005P is illustrated in Figure 5. In this circuit, the target output voltage is regulated by connecting the VSEN pin directly to the output regulation point. The VSEN signal is then compared to a reference voltage that has been set to the desired output voltage level by the user. The error signal derived from this comparison is converted to a digital value with a low-resolution analog to digital (A/D) converter. The digital signal is applied to an adjustable digital compensation filter, and the compensated signal is used to derive the appropriate PWM duty cycle for driving the external MOSFETs in a way that produces the desired output.

The ZL2005P also incorporates a non-linear response (NLR) loop to reduce the response time and output deviation in response to a load transient. The ZL2005P has an efficiency optimization circuit that continuously monitors the power converter’s operating conditions and adjusts the turn-on and turn-off timing of the high-side and low-side MOSFETs to optimize the overall efficiency of the power supply.

4.4 Power Management Overview

The ZL2005P incorporates a wide range of configurable power management features that are simple to implement with no external components. Additionally, the ZL2005P includes circuit protection features that continuously safeguard the load from damage due to unexpected system faults. The ZL2005P can continuously monitor input voltage, output voltage/current, internal temperature, and the temperature of an external thermal diode. A Power Good output signal is provided to enable power-on reset functionality for an external processor.

All power management functions can be configured using either simple pin configuration techniques (Figure 8) or via the I^2C/SMBus interface. Monitoring parameters can be pre-configured to provide alerts for specific conditions. See Application Note AN2013 for more details on SMBus monitoring.

4.5 Multi-mode Pins

In order to simplify circuit design, the ZL2005P incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device without requiring the user to program the IC. For the ZL2005P only a few of the power management features can be configured using these pins. The multi-mode pins can respond to four different connections as shown in Table 5. Any combination of connections is allowed among the multi-mode pins. These pins are sampled when power is applied or by issuing a PMBus Restore command (See Application Note AN2013).

Table 5. Multi-mode Pin Configuration

Pin Tied To	Value
GND (Logic low)	$< 0.8\ V_{DC}$
OPEN (N/C)	No connection
HIGH (Logic high)	$> 2.0\ V_{DC}$
Resistor to SGND	Set by resistor value

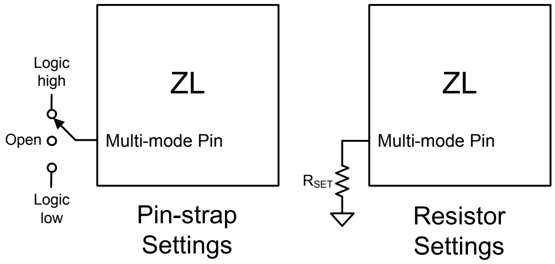


Figure 8. Pin-strap and Resistor Setting Examples

Pin-strap Settings: This is the simplest implementation method, as no external components are required. Using this method, each pin can take on one of three possible states: GND, OPEN, or HIGH. These pins can be connected to the VR or V25 pins for logic HIGH settings, as either pin provides a regulated voltage greater than 2V. Using a single pin, the user can select one of three settings, and using two pins, the user can select one of nine settings.

Resistor Settings: This method allows a greater range of adjustability when connecting a finite valued resistor (in a specified range) between the multi-mode pin and SGND. Standard 1% resistor values are used, and only every fourth E96 resistor value is used so that the device can reliably recognize the value of resistance connected to the pin while eliminating the errors associated with the resistor accuracy. A total of 25 unique selections are available using a single resistor.

I^2C/SMBus Settings: Almost any ZL2005P function can be configured via the I^2C/SMBus interface using standard PMBus commands. Additionally, any value that has been configured using the pin-strap or resistor setting methods can also be re-configured and/or verified via the I^2C/SMBus. See Application Note AN2013 for details.

The SMBus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set via the I^2C/SMBus. the device address is set using the SA0 and SA1 pins. The VOUT_MAX is determined as 10% greater than the voltage set by the V0/V1 pins or VADJ pin.

5 Power Conversion Functional Description

5.1 Internal Bias Regulators and Input Supply Connections

The ZL2005P employs two internal low dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

VR: The VR LDO provides a regulated 5V bias supply for the MOSFET driver circuits. It is powered from the VDD pin and can supply up to 100 mA output current. A 4.7 µF filter capacitor is required at the VR pin.

V25: The V25 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from an internal 5V node and can supply up to 50 mA output current. A 10 µF filter capacitor is required at the V25 pin.

Note: The internal bias regulators are designed for powering internal circuitry only. Do not attach external loads to any of these pins. The multi-mode pins may be connected to the VR or V25 pins for logic HIGH settings.

When the input supply (V_{DD}) is higher than 5.5V, the VR pin should not be connected to any other pin. It should only have a filter capacitor attached as shown in Figure 9. Due to the dropout voltage associated with the VR bias regulator, the VDD pin must be connected to the VR pin for designs operating from a VDD supply from 3.0V to 5.5V. Figure 9 illustrates the required connections for both cases. For input supplies between 4.5V and 5.5V, either method can be used.

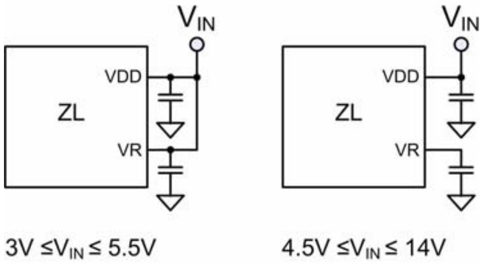


Figure 9. Input Supply Connections

5.2 High-side Driver Boost Circuit

The gate drive voltage for the upper MOSFET driver is generated by a floating bootstrap capacitor, CB (see Figure 3). When the lower MOSFET (QL) is turned on, the SW node is pulled to ground and the capacitor is charged from the internal VR bias regulator through diode DB. When QL turns off and the upper MOSFET (QH) turns on, the SW node is pulled up to V_{DD} and the voltage on the BST pin is boosted approximately 5V above V_{IN} to provide the necessary voltage for the high-side driver. A Schottky diode should be used for DB to maximize the high-side drive voltage.

5.3 Output Voltage Selection

Standard Mode (ZL2005)

The output voltage may be set to any voltage between 0.6V and 5.0V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification. By connecting the V0 and V1 pins to logic high, logic low, or leaving them floating, V_{OUT} can be set to any of nine standard voltages as shown in Table 6.

Table 6. Pin-strap Output Voltage Settings

		V0		
		LOW	**OPEN**	**HIGH**
V1	**LOW**	0.6V	0.8V	1.0V
	OPEN	1.2V	1.5V	1.8V
	HIGH	2.5V	3.3V	5.0V

If an output voltage other than those in Table 6 is desired, the resistor setting method can be used. Using this method, resistors R0 and R1 are selected to produce a specific voltage between 0.6V and 5.0V in 10 mV steps. Resistor R1 provides a coarse setting and R0 a fine adjustment, thus eliminating the additional errors associated with using two 1% resistors in a standard analog implementation (this typically adds 1.4% error using two 1% resistors).

To set V_{OUT} using resistors, follow the steps below to calculate an index value and then use Table 7 to select the resistor that corresponds to the calculated index value as follows:

1. Calculate Index1:
   Index1 = 4 x V_{OUT}
2. Round the result down to the nearest whole number.
3. Select the value for R1 from Table 7 using the Index1 rounded value from step 2.
4. Calculate Index0 using equation
   Index0 = 100 x V_{OUT} - 25 x Index1
5. Select the value for R0 from Table 7 using Index0 from step 4.

Table 7. Resistors for Setting Output Voltage

Index	R0 or R1
0	10 kΩ
1	11 kΩ
2	12.1 kΩ
3	13.3 kΩ
4	14.7 kΩ
5	16.2 kΩ
6	17.8 kΩ
7	19.6 kΩ
8	21.5 kΩ
9	23.7 kΩ
10	26.1 kΩ
11	28.7 kΩ
12	31.6 kΩ
13	34.8 kΩ
14	38.3 kΩ
15	42.2 kΩ
16	46.4 kΩ
17	51.1 kΩ
18	56.2 kΩ
19	61.9 kΩ
20	68.1 kΩ
21	75 kΩ
22	82.5 kΩ
23	90.9 kΩ
24	100 kΩ

Example:

For V_{OUT} = 1.33V:

Index1 = 4 x 1.33V = 5.32 (5);

From Table 7, using Index = 5
R1 = 16.2 kΩ

Index0 = (100 x 1.33V) - (25 x 5) = 8;
From Table 7; R0 = 21.5 kΩ

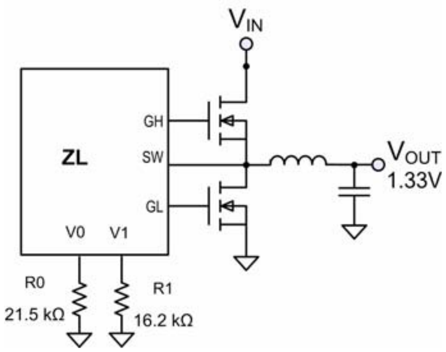


Figure 10. Output Voltage Resistor Setting

The output voltage may also be set to any value between 0.6V and 5.0V using the I^2C/SMBus interface. The maximum voltage that can be set is limited to 110% of the pin-strap value. See Application Note AN2013 for details.

POLA/DOSA Trim Method

The output voltage can also be set using the VADJ pin to map the standard analog resistor method. This mode is activated by setting the PMBus private command POLA_VADJ_CONFIG to 1.

The POLA/DOSA mode can also be set up by pinstrap using a resistor on V0.

A 110 kΩ resistor on V0 will set to POLA mode 1.

A 120 kΩ resistor on V0 will set to POLA mode 2.

In POLA mode 1 and 2, V0 and V1 pins are inactive, and the ZL2005P uses the following table to set the output voltage with the VADJ pin.

Table 8. Resistors for Setting POLA Output Voltage with VADJ

V_{OUT}	R_{SET} (kΩ) Min / Typ / Max	V_{OUT}	R_{SET} (kΩ) Min / Typ / Max
0.700V	155 / 159 / 169	0.991V	21.38 / 21.6 / 21.82
0.752V	109.89 / 111 / 112.11	1.000V	18.51 / 18.7 / 18.89
0.758V	99 / 100 / 101	1.100V	15.94 / 16.1 / 16.26
0.765V	89.1 / 90 / 90.9	1.158V	13.56 / 13.7 / 13.84
0.772V	80.09 / 80.9 / 81.71	1.200V	11.39 / 11.5 / 11.62
0.790V	64.35 / 72.5 / 73.23	1.250V	9.5 / 9.6 / 9.7
0.800V	57.52 / 58.1 / 58.68	1.500V	7.72 / 7.8 / 7.88
0.821V	51.38 / 51.9 / 52.42	1.669V	6.14 / 6.2 / 6.26
0.848V	40.69 / 41.1 / 41.51	1.800V	4.65 / 4.7 / 4.75
0.880V	36.04 / 36.4 / 36.76	2.295V	3.27 / 3.3 / 3.33
0.899V	31.88 / 32.2 / 32.52	2.506V	2.08 / 2.1 / 2.12
0.919V	28.02 / 28.3 / 28.58	3.300V	0.99 / 1 / 1.01
0.965V	24.55 / 24.8 / 25.05	5.000V	0 / 0 / 0.05

The standard method for adjusting output voltage used in a POLA module is defined by the below equation:

$R_{set} = 10k\Omega \times 0.69V/(V_{OUT} - 0.69V) - 1.43k\Omega$

Rset is an external resistor.

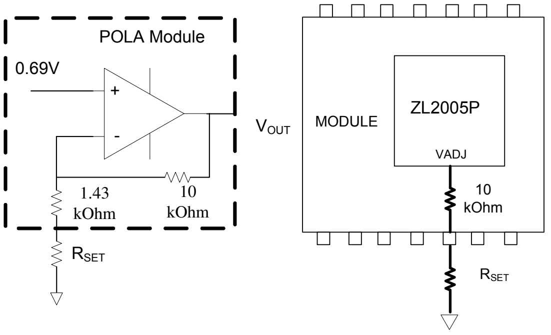


Figure 11. Output Voltage Resistor Setting POLA - ZL2005P

To stay compatible with existing methods for adjusting output voltage, the module manufacturer can add a 10 kΩ resistor on the module.

$R_{VADJ} = R_{SET} + 10\ k\Omega$

By adding this additional resistor, the resistor values shown in Table 8 can be used to set the output voltage of a ZL2005P module. These values are close to the analog POLA values and are compatible with the pin-strap resistor detection methodology of the ZL2005P.

DOSA Voltage Trim Method

For DOSA output voltage selection, a 8.66 kΩ resistor needs to be used in place of the 10 kΩ resistor. This will allow setting the output voltage with resistor values close to the DOSA equation result:

$R_{set} = 6900/(V_{OUT} - 0.69V)$.

Table 9. Resistors for Setting DOSA Output Voltage with VADJ

V_{OUT}	R_{SET} (kΩ) Min / Typ / Max	V_{OUT}	R_{SET} (kΩ) Min / Typ / Max
0.700V	156 / 160 / 170	0.991V	22.71 / 22.94 / 23.17
0.752V	111.22 / 112.34 / 113.46	1.000V	19.84 / 20.04 / 20.24
0.758V	100.33 / 101.34 / 102.35	1.100V	17.27 / 17.44 / 17.61
0.765V	90.43 / 91.34 / 92.25	1.158V	14.89 / 15.04 / 15.19
0.772V	81.42 / 82.24 / 83.06	1.200V	12.71 / 12.84 / 12.97
0.790V	65.68 / 73.84 / 74.58	1.250V	10.83 / 10.94 / 11.05
0.800V	58.85 / 59.44 / 60.03	1.500V	9.05 / 9.14 / 9.23
0.821V	52.71 / 53.24 / 53.77	1.669V	7.46 / 7.54 / 7.62
0.848V	42.02 / 42.44 / 42.86	1.800V	5.98 / 6.04 / 6.10
0.880V	37.36 / 37.74 / 38.12	2.295V	4.59 / 4.64 / 4.69
0.899V	33.20 / 33.54 / 33.88	2.506V	3.41 / 3.44 / 3.47
0.919V	29.34 / 29.64 / 29.94	3.300V	2.32 / 2.34 / 2.36
0.965V	25.88 / 26.14 / 26.40	5.000V	1.33 / 1.34 / 1.35

UVLO (POLA Mode)

In POLA mode 1 and 2, undervoltage threshold (UVLO) is set following POLA standard methodology.

In the POLA standard, a resistor on the UVLO pin sets the corresponding voltage value.

For a module supplier, a 1.5 kΩ 1% pull-up resistor from EN to UVLO is required to be compatible with the POLA Inhibit/UVLO features (Figure 12). EN must be driven by an open collector/drain driver, and will default to Enabled unless pulled low. The driver must remain open after a transition for a minimum of 1 ms to allow the measurement of the resistor on the UVLO pin.

By default UVLO is set to 4.5V.

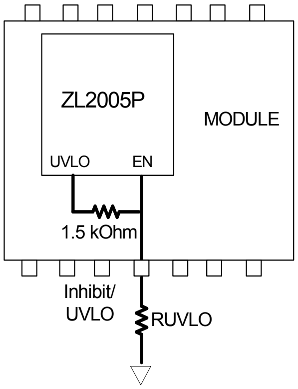


Figure 12. UVLO Circuit

Figure 12 shows how to select UVLO based on an external resistor R_{SET}.

R_{UVLO} maps the POLA equation to set the UVLO threshold:

R_{UVLO} = (9690 - (137*V_{IN}))/(137*V_{IN}-585) in kΩ

Table 10 shows a chart of standard resistor values for R_{UVLO}:

Table 10. Resistors for Setting UVLO with R_{UVLO}

UVLO	R_{UVLO} in series with 1.5 kΩ resistor
4.3V	162 kΩ
4.5V	121 kΩ
4.87V	110 kΩ
4.93V	100 kΩ
4.99V	90.9 kΩ
5.07V	82.5 kΩ
5.15V	75.0 kΩ
5.23V	68.1 kΩ
5.33V	61.9 kΩ
5.43V	56.2 kΩ
5.55V	51.1 kΩ
5.67V	46.4 kΩ
5.81V	42.2 kΩ
6.20V	38.3 kΩ
6.60V	28.7 kΩ
6.96V	23.7 kΩ
7.22V	21.5 kΩ
7.50V	19.6 kΩ
7.81V	17.8 kΩ
8.13V	16.2 kΩ
8.50V	14.7 kΩ
8.92V	13.3 kΩ
9.34V	12.1 kΩ
9.81V	11.0 kΩ
10.86V	9.09 kΩ
11.46V	8.25 kΩ

For a POLA module, the Inhibit feature is combined with UVLO.

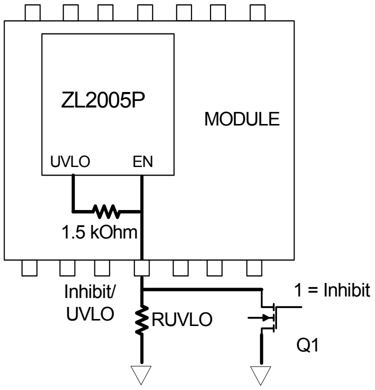


Figure 13. INHIBIT Circuit

Figure 13 shows the typical application of the Inhibit function. The inhibit input has its own internal pull-up. An open-drain transistor is recommended for control.

Flexible pin

When POLA_VADJ_CONFIG is set to mode 2, the ZL2005P uses the VADJ pin for output voltage setting and it also disables the SYNC pin. In this mode, the ZL2005P is not checking the SYNC pin for synchronization to an external signal. Otherwise the resistor measurement may not be accurate. This configuration allows a module supplier to connect both VADJ and SYNC pin to a common pin on the module (Flex pin). A single module pin can then be used for one or the other function.

In this mode UVLO will also follow the POLA method.

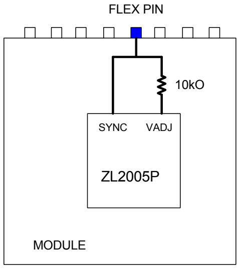


Figure 14. Output Voltage Resistor Setting Example

5.4 Start-up Procedure

The ZL2005P follows a specific internal start-up procedure after power is applied to the VDD pin. Table 11 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock must be stable prior to asserting the EN pin. The device requires approximately 10-20 ms to check for specific values stored in its internal memory.

If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the I^2C/SMBus interface and the device is ready to be enabled. Once enabled, the device requires approximately 6 ms before its output voltage may be allowed to start its ramp-up process. If a soft start delay period less than 6 ms has been configured (using the DLY (0,1) pins), the device will default to a 6 ms delay period. If a delay period of 6 ms or higher is configured, the device will wait for the configured delay period before starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the pre-configured soft-start ramp time.

Table 11. ZL2005P Start-up Sequence

Step #	Step Name	Description	Time Duration
1	Power Applied	Input voltage is applied to the ZL2005P's VDD pin	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approx 10-20 ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by multi-mode pins.	
4	Device Ready	The device is ready to accept an ENABLE signal.	—
5	Pre-ramp Delay	The device requires approximately 6 ms following an enable signal and prior to ramping its output. Additional pre-ramp delay may be configured using the Delay pins.	Approx. 6 ms

5.5 Soft Start Delay and Ramp Times

In some system applications, it may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its nominal value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its nominal value after the delay period has expired. The ZL2005P gives the system designer several options for precisely and independently controlling both the delay and ramp time periods for V_{OUT}. These features may be used as part of an overall in-rush current management strategy or to precisely control how fast a load IC is turned on.

The soft start delay period begins when the Enable pin is asserted and ends when the delay time expires. The soft-start delay period is set via the I^2C/SMBus interface.The soft start ramp enables a controlled ramp to the nominal V_{OUT} value that begins once the delay period has timed out. The ramp-up is guaranteed monotonic and its slope may be precisely set by setting the soft-start ramp time using the SS (0,1) pins.

The soft start delay and ramp times can be set to standard values according to Table 12 and Table 13 respectively.

Table 12. Soft Start Delay Settings

		DLY0		
		LOW	**OPEN**	**HIGH**
DLY1	**LOW**	0 ms[1]	Reserved	
	OPEN	5 ms[1]	10 ms	20 ms
	HIGH	50 ms	100 ms	200 ms

NOTE:

1. When the device is set to 0 ms or 5 ms delay, it will begin its ramp up after the internal circuitry has initialized (approx. 6 ms).

Table 13. Soft Start Ramp Settings

		SS0		
		LOW	**OPEN**	**HIGH**
SS1	**LOW**	0 ms[1]	1 ms	2 ms
	OPEN	5 ms	10 ms	20 ms
	HIGH	50 ms	100 ms	200 ms

NOTE:

1. When the soft start ramp is set to zero, the device will ramp up as quickly as the internal circuitry and output load capacitance will allow.

If the desired soft start delay and ramp times are not one of the values listed in Table 11 and Table 12, the times can be set to a custom value by connecting a resistor from the DLY0 or SS0 pin to SGND using the appropriate resistor value from Table 14. The value of this resistor is measured upon start-up or Restore and will not change if this resistor is varied after power has been applied to the ZL2005. See Figure 15 for typical connections using resistors.

Note: Do not connect a resistor to the DLY1 or SS1 pin. These pins are not utilized for setting soft-start delay and ramp times. Connecting an external resistor to these pins may cause conflicts with other device settings.

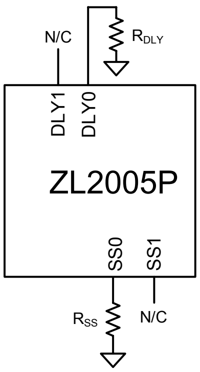


Figure 15. DLY and SS Pin Resistor Connections

Table 14. DLY and SS Resistor Values

DLY or SS	R_{DLY} or R_{SS}	DLY or SS	R_{DLY} or R_{SS}
0 ms	10 kΩ	110 ms	28.7 kΩ
10 ms	11 kΩ	120 ms	31.6 kΩ
20 ms	12.1 kΩ	130 ms	34.8 kΩ
30 ms	13.3 kΩ	140 ms	38.3 kΩ
40 ms	14.7 kΩ	150 ms	42.2 kΩ
50 ms	16.2 kΩ	160 ms	46.4 kΩ
60 ms	17.8 kΩ	170 ms	51.1 kΩ
70 ms	19.6 kΩ	180 ms	56.2 kΩ
80 ms	21.5 kΩ	190 ms	61.9 kΩ
90 ms	23.7 kΩ	200 ms	68.1 kΩ
100 ms	26.1 kΩ		

The soft start delay and ramp period can be set to custom values via the I^2C/SMBus interface. When the soft start delay is set to 0 ms, the device will begin its ramp up after the internal circuitry has initialized (approx. 6ms).

5.6 Power Good

The ZL2005P provides a Power Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within -10% to +15% of the target voltage These limits may be changed via the I^2C/SMBus interface. See Application Note AN2013 for details.

A PG delay period is defined as the time from when all conditions within the ZL2005P for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL2005P PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 10 ms, the PG delay will be set to 10 ms. The PG delay may be set independently of the soft-start ramp using the I^2C/SMBus as described in Application Note AN2013.

5.7 Switching Frequency and PLL

The ZL2005P incorporates an internal phase locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an internal oscillator or driven from an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock output for use by other devices. The SYNC pin is a unique pin that can perform multiple functions depending on how it is configured. The CFG pin is used to select the operating mode of the SYNC pin as shown in Table 15. Figure 16 illustrates the typical connections for each mode.

Table 15. SYNC Pin Function Selection

CFG Pin	SYNC Pin Function
LOW	SYNC is configured as an input
OPEN	Auto Detect mode
HIGH	SYNC is configured as an output f_{SW} = 400 kHz (default)

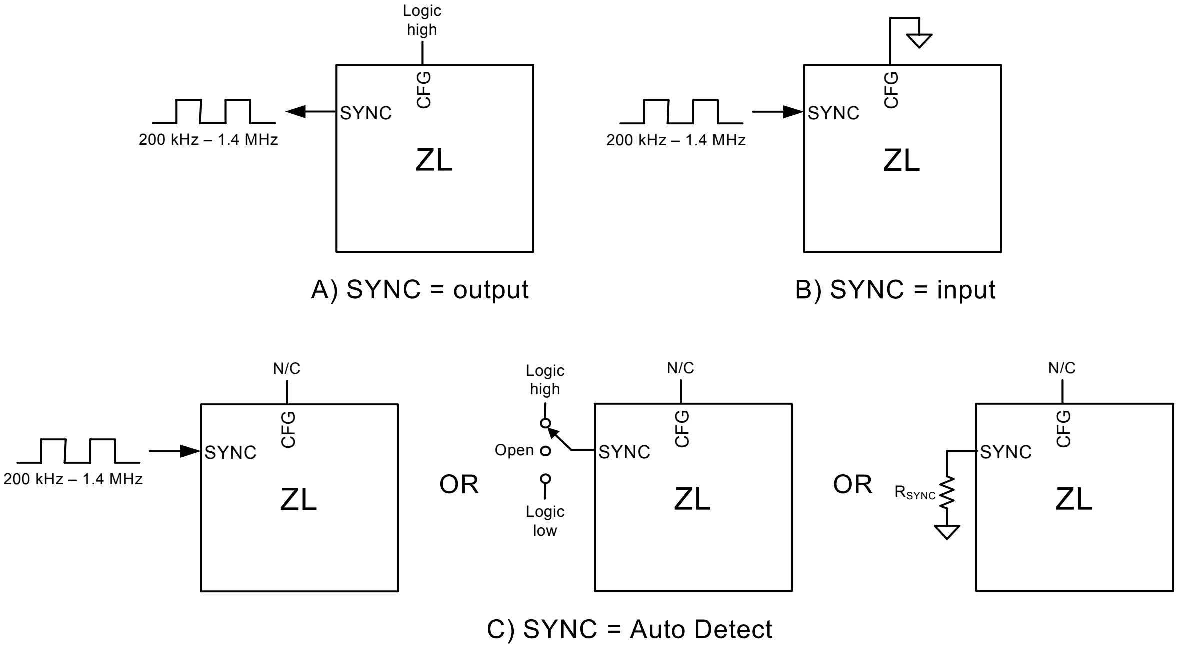


Figure 16. SYNC Pin Configurations

Configuration A: SYNC OUTPUT

When the SYNC pin is configured as an output (CFG pin is tied HIGH), the device will operate from its internal oscillator and will drive the resulting internal oscillator signal (preset to 400 kHz) onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this configuration.

Configuration B: SYNC INPUT

When the SYNC pin is configured as an input (CFG pin is tied LOW), the device will automatically check for a clock signal on the SYNC pin each time EN is asserted. The ZL2005P's oscillator will then synchronize with the rising edge of external clock.

The incoming clock signal must be in the range of 200 kHz to 1.4 MHz and must be stable when the enable pin is asserted. The clock signal must also exhibit the necessary performance requirements (see Table 3). In the event of a loss of the external clock signal, the output voltage may show transient over/undershoot.

If this happens, the ZL2005P will turn off the power FETs (QH and QL in Figure 4) typically within 10 µS. Users are discouraged from removing an external SYNC clock while the ZL2005P is operating with Enable asserted.

Configuration C: SYNC AUTO DETECT

When the SYNC pin is configured in auto detect mode (CFG pin is left OPEN), the device will automatically check for a clock signal on the SYNC pin after enable is asserted.

If a clock signal is present, The ZL2005P's oscillator will then synchronize the rising edge of the external clock. Refer to SYNC INPUT description.

If no incoming clock signal is present, the ZL2005P will configure the switching frequency according to the state of the SYNC pin as listed in Table 16. In this mode, the ZL2005P will only read the SYNC pin connection during the start-up sequence. Changes to SYNC pin connections will not affect f_{SW} until the power (VDD) is cycled off and on.

Table 16. Switching Frequency Selection

SYNC Pin Setting	Frequency
LOW	200 kHz
OPEN	400 kHz
HIGH	1 MHz
Resistor	See Table 17

If the user wishes to run the ZL2005P at a frequency other than those listed in Table 16, the switching frequency can be set using an external resistor, R_{SYNC}, connected between SYNC and SGND using Table 17.

Table 17. R_{SYNC} Resistor Values

f_{SW}	R_{SYNC}
200 kHz	10 kΩ
222 kHz	11 kΩ
242 kHz	12.1 kΩ
267 kHz	13.3 kΩ
296 kHz	14.7 kΩ
320 kHz	16.2 kΩ
364 kHz	17.8 kΩ
400 kHz	19.6 kΩ
421 kHz	21.5 kΩ
471 kHz	23.7 kΩ

f_{SW}	R_{SYNC}
533 kHz	26.1 kΩ
571 kHz	28.7 kΩ
615 kHz	31.6 kΩ
667 kHz	34.8 kΩ
727 kHz	38.3 kΩ
889 kHz	46.4 kΩ
1000 kHz	51.1 kΩ
1143 kHz	56.2 kΩ
1333 kHz	68.1 kΩ

The switching frequency can also be set to any value between 200 kHz and 1.4 MHz using the I^2C/SMBus interface. The available frequencies are bounded by the relation f_{sw} = 8 MHz/N, (with 6<= N <= 40). See Application Note AN2013 for details on configuring the switching frequency using the I^2C/SMBus interface.

If multiple ZL2005Ps are used together, connecting the SYNC pins together will force all devices to synchronize to one another. The CFG pin of one device must have its SYNC pin set as an output and the remaining devices must have their SYNC pins set as an input or all devices must be driven by the same external clock source.

Note: The switching frequency read back using the appropriate PMBus command will differ slightly from the selected value in Table 17. The difference is due to hardware quantization.

5.8 Selecting Power Train Components

The ZL2005P is a synchronous buck controller that uses external MOSFETs, inductor and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance. Zilker Labs offers an online circuit design and simulation tool, PowerPilot, to assist designers in this task.

Please visit www.intersil.com/zilkerlabs/ to access PowerPilot. For more detailed guidelines regarding component selection, please refer to Application Note AN2011.

To select the appropriate power stage components for a set of desired performance goals, the power supply requirements listed in Table 18 must be known.

Table 18. Power Supply Requirements Example

Parameter	Range	Example Value
Input voltage (V_{IN})	3.0 – 14.0 V	12 V
Output voltage (V_{OUT})	0.6 – 5.0 V	1.2 V
Output current (I_{OUT})	0 to ~25 A	20 A
Output voltage ripple (V_{orip})	< 3% of V_{OUT}	1% of V_{OUT}
Output load step (I_{ostep})	< Io	50% of I_o
Output load step rate	—	10 A/µS
Allowable output deviation due to load step	—	± 50 mV
Maximum PCB temp.	120°C	85°C
Desired efficiency	—	85%
Other considerations	Various	Optimize for small size

Design Trade-offs

The design of a switching regulator power stage requires the user to consider trade-offs between cost, size and performance. For example, size can be optimized at the expense of efficiency. Additionally, cost can be optimized at the expense of size. For a detailed description of circuit trade-offs, refer to Application Note AN2011.

To start a design, select a switching frequency (f_{SW}) based on Table 19. This frequency is a starting point and may be adjusted as the design progresses.

Table 19. Circuit Design Considerations

Frequency Range	Efficiency	Circuit Size
200 – 400 kHz	Highest	Larger
400 – 800 kHz	Moderate	Smaller
800 – 1400 kHz	Lower	Smallest

Inductor Selection

The output inductor selection process will include several trade-offs. A high inductance value will result in a low ripple current (I_{opp}), which will reduce the output capacitance requirement and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be struck between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple current (I_{opp}) equal to the expected load transient step magnitude (I_{ostep}):

$$I_{opp} = I_{ostep} \quad (3)$$

Now the output inductance can be calculated using the following equation:

$$L_{OUT} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INM}}\right)}{f_{sw} \times I_{opp}} \quad (4)$$

where V_{INM} is the maximum input voltage.

The average inductor current is equal to the maximum output current. The peak inductor current (IL_{pk}) is calculated using the following equation where I_{OUT} is the maximum output current:

$$IL_{pk} = I_{OUT} + \frac{I_{opp}}{2} \quad (5)$$

Select an inductor rated for the average DC current with a peak current rating above the peak current computed above.

In over-current or short-circuit conditions, the inductor may have currents greater than 2X the normal maximum rated output current. It is desirable to use an inductor that is not saturated at these conditions to protect the load and the power supply MOSFETs from damaging currents.

Once an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's datasheet.

$$P_{LDCR} = DCR \times I_{Lrms}^{\ 2} \quad (6)$$

I_{Lrms} is given by:

$$I_{Lrms} = \sqrt{I_{OUT}^{\ 2} + \frac{I_{opp}^{\ 2}}{12}} \quad (7)$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor's datasheet. Add the core loss and the DCR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

Output Capacitor Selection

Several trade-offs also must be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up to the new steady state output current value.

As a starting point, allocate one-half of the output voltage ripple to the capacitor ESR and the other half to its capacitance, as shown in the following equations:

$$C_{OUT} = \frac{I_{opp}}{8 \times f_{sw} \times \frac{V_{orip}}{2}} \quad (8)$$

$$ESR = \frac{V_{orip}}{2 \times I_{opp}} \quad (9)$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using the following equation:

$$V_{orip} = I_{opp} \times ESR + \frac{I_{opp}}{8 \times f_{sw} \times C_{OUT}} \quad (10)$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

For more information on the performance of the power supply in response to a transient load, refer to Application Note AN2011.

Input Capacitor

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5 or 12 V “bulk” supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This input ripple (I_{CINrms}) can be determined from the following equation:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1 - D)} \qquad (11)$$

Please refer to Application Note AN2011 for detailed derivation including efficiency and ripple current.

Without capacitive filtering near the power supply input circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2X the ripple current calculated above to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage are recommended.

Bootstrap Circuit Component Selection

The high-side driver boost circuit utilizes an external Schottky diode (DB) and an external bootstrap capacitor (CB) to supply sufficient gate drive for the high-side MOSFET driver. DB should be a 20 mA, 30 V Schottky diode or equivalent device and CB should be a 1 µF ceramic type rated for at least 6.3V.

QL Selection

The bottom MOSFET should be selected primarily based on the device’s $R_{DS(ON)}$ and secondarily based on its gate charge. To choose QL, use the following equation and allow 2–5% of the output power to be dissipated in the $R_{DS(ON)}$ of QL (lower output voltages and higher step-down ratios will be closer to 5%):

$$P_{QL} = 0.05 \times V_{OUT} \times I_{OUT} \qquad (12)$$

Calculate the RMS current in QL as follows:

$$I_{botrms} = I_{Lrms} \times \sqrt{1 - D} \qquad (13)$$

Calculate the desired maximum $R_{DS(ON)}$ as follows:

$$R_{DS(ON)} = P_{QL}/I_{botrms}^{2} \qquad (14)$$

Note that the $R_{DS(ON)}$ given in the manufacturer’s datasheet is measured at 25°C. The actual $R_{DS(ON)}$ in the end-use application will be much higher. For example, a Vishay Si7114 MOSFET with a junction temperature of 125°C has an $R_{DS(ON)}$ 1.4 times higher than the value at 25°C.

Select a candidate MOSFET, and calculate the required gate drive current as follows:

$$I_g = f_{sw} \times Q_g \qquad (15)$$

Keep in mind that the total allowed gate drive current for both QH and QL is 80 mA.

MOSFETs with lower $R_{DS(ON)}$ tend to have higher gate charge requirements, which increases the current and resulting power required to turn them on and off. Since the MOSFET gate drive circuits are integrated in the ZL2005P, this power is dissipated in the ZL2005P according to the following equation:

$$P_{QL} = f_{sw} \times Q_g \times V_{INM} \qquad (16)$$

QH Selection

In addition to the $R_{DS(ON)}$ loss and gate charge loss, QH also has switching loss. The procedure to select QH is similar to the procedure for QL. First, assign 2–5% of the output power to be dissipated in the $R_{DS(ON)}$ of QH using the equation for QL above. As was done with QL, calculate the RMS current as follows:

$$I_{toprms} = I_{Lrms} \times \sqrt{D} \qquad (17)$$

Calculate a starting $R_{DS(ON)}$ as follows, in this example using 5%:

$$P_{QH} = 0.05 \times V_{OUT} \times I_{OUT} \qquad (18)$$

$$R_{DS(ON)} = P_{QH} / I_{toprms}^{2} \qquad (19)$$

Select a MOSFET and calculate the resulting gate drive current. Verify that the combined gate drive current from QL and QH does not exceed 80 mA.

Next, calculate the switching time using:

$$t_{sw} = \frac{Q_g}{I_{gdr}} \qquad (20)$$

where Q_g is the gate charge of the selected QH and I_{gdr} is the peak gate drive current available from the ZL2005P.

Although the ZL2005P has a typical gate drive current of 3 A, use the minimum guaranteed current of 2 A for a conservative design. Using the calculated switching time, calculate the switching power loss in QH using

$$P_{swtop} = V_{INM} \times t_{sw} \times I_{OUT} \times f_{sw} \qquad (21)$$

The total power dissipated by QH is given by the following equation:

$$P_{QHtot} = P_{QH} + P_{swtop} \qquad (22)$$

MOSFET Thermal Check

Once the power dissipations for QH and QL have been calculated, the MOSFET's junction temperature can be estimated. Using the junction-to-case thermal resistance (R_{th}) given in the MOSFET manufacturer's datasheet and the expected maximum printed circuit board temperature, calculate the junction temperature as follows:

$$T_{j\,\max} = T_{pcb} + P_Q \times R_{th} \qquad (23)$$

Current Sensing Components

Once the current sense method has been selected (Refer to Section 5.9, "Current Limit Threshold Selection,"), the procedure to select the component is the following:

When using the inductor DCR sensing method, the user must also select an R/C network comprised of R1 and CL (see Figure 17).

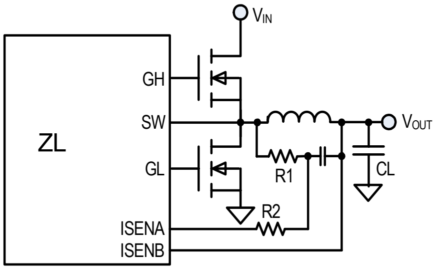


Figure 17. DCR Current Sensing

These components should be selected according to the following equation:

$$\tau_{RC} = L / DCR \qquad (24)$$

R1 should be in the range of 500 Ω to 5 kΩ in order to minimize the power dissipation through it. The user should make sure the resistor package size is appropriate for the power dissipated. Once R1 has been calculated, the value of R2 should be selected based on the following equation:

$$R2 = 5 \times R1 \qquad (25)$$

If $R_{DS(ON)}$ is being used the external low side MOSFET will act as the sensing element as indicated in Figure 18.

5.9 Current Limit Threshold Selection

It is recommended that the user include a current limiting mechanism in their design to protect the power supply from damage and prevent excessive current from being drawn from the input supply in the event that the output is shorted to ground or an overload condition is imposed on the output. Current limiting is accomplished by sensing the current flowing through the circuit during a portion of the duty cycle.

Output current sensing can be accomplished by measuring the voltage across a series resistive sensing element according to equation 26.

$$V_{LIM} = I_{LIM} \times R_{SENSE} \qquad (26)$$

Where:

I_{LIM} is the desired maximum current that should flow in the circuit

R_{SENSE} is the resistance of the sensing element

V_{LIM} is the voltage across the sensing element at the point the circuit should start limiting the output current.