Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ZL6100

Data Sheet | December 15, 2010 | FN6850.1

Adaptive Digital DC-DC Controller with Drivers and Current Sharing

Description

The ZL2006 is a digital DC-DC controller with integrated MOSFET drivers. Current sharing allows multiple devices to be connected in parallel to source loads with very high current demands. Adaptive performance optimization algorithms improve power conversion efficiency across the entire load range. Zilker Labs Digital-DC™ technology enables a blend of power conversion performance and power management features.

The ZL2006 is designed to be a flexible building block for DC power and can be easily adapted to designs ranging from a single-phase power supply operating from a 3.3 V input to a multi-phase supply operating from a 12 V input. The ZL2006 eliminates the need for complicated power supply managers as well as numerous external discrete components.

All operating features can be configured by simple pin-strap/resistor selection or through the SMBus™ serial interface. The ZL2006 uses the PMBus™ protocol for communication with a host controller and the Digital-DC bus for communication between other Zilker Labs devices.

Features

Power Conversion

- Efficient synchronous buck controller
- Adaptive light load efficiency optimization
- 3 V to 14 V input range
- 0.54 V to 5.5 V output range (with margin)
- ±1% output voltage accuracy
- Internal 3 A MOSFET drivers
- Fast load transient response
- Current sharing and phase interleaving
- *Snapshot*™ parameter capture
- RoHS compliant (6 x 6 mm) QFN package

Power Management

- Digital soft start / stop
- Precision delay and ramp-up
- Power good / enable
- Voltage tracking, sequencing, and margining
- Voltage / current / temperature monitoring
- I^2C/SMBus interface, PMBus compatible
- Output voltage and current protection
- Internal non-volatile memory (NVM)

Applications

- Servers / storage equipment
- Telecom / datacom equipment
- Power supplies (memory, DSP, ASIC, FPGA)

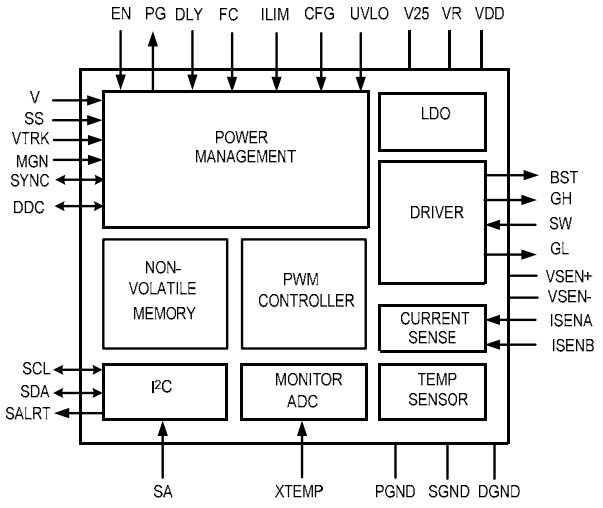


Figure 1. Block Diagram

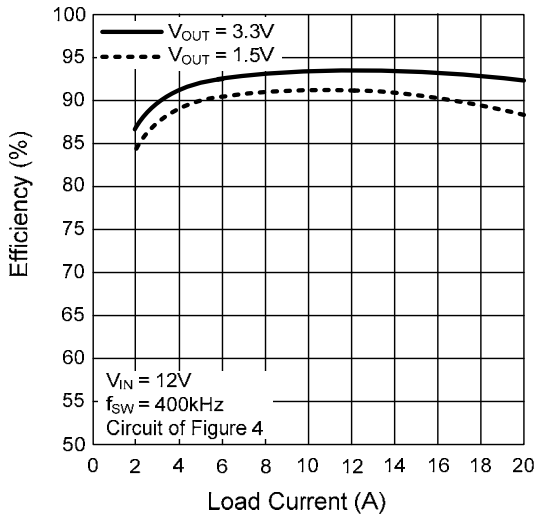


Figure 2. Efficiency vs. Load Current

Table of Contents

1. Electrical Characteristics 3
2. Pin Descriptions 7
3. Typical Application Circuit 9
4. ZL2006 Overview 10
   - 4.1 Digital-DC Architecture 10
   - 4.2 Power Conversion Overview 11
   - 4.3 Power Management Overview 12
   - 4.4 Multi-mode Pins 13

5. Power Conversion Functional Description 14
   - 5.1 Internal Bias Regulators and Input Supply Connections 14
   - 5.2 High-side Driver Boost Circuit 14
   - 5.3 Output Voltage Selection 14
   - 5.4 Start-up Procedure 17
   - 5.5 Soft Start Delay and Ramp Times 17
   - 5.6 Power Good 18
   - 5.7 Switching Frequency and PLL 19
   - 5.8 Power Train Component Selection 20
   - 5.9 Current Limit Threshold Selection 24
   - 5.10 Loop Compensation 27
   - 5.11 Adaptive Compensation 28
   - 5.12 Non-linear Response (NLR) Settings 28
   - 5.13 Efficiency Optimized Driver Dead-time Control 28
   - 5.14 Adaptive Diode Emulation 29
   - 5.15 Adaptive Frequency Control 29

6. Power Management Functional Description 30
   - 6.1 Input Undervoltage Lockout 30
   - 6.2 Output Overvoltage Protection 30
   - 6.3 Output Pre-Bias Protection 31
   - 6.4 Output Overcurrent Protection 32
   - 6.5 Thermal Overload Protection 32
   - 6.6 Voltage Tracking 32
   - 6.7 Voltage Margining 33
   - 6.8 I^2C/SMBus Communications 34
   - 6.9 I^2C/SMBus Device Address Selection 34
   - 6.10 Digital-DC Bus 35
   - 6.11 Phase Spreading 35
   - 6.12 Output Sequencing 36
   - 6.13 Fault Spreading 36
   - 6.14 Temperature Monitoring Using the XTEMP Pin 37
   - 6.15 Active Current Sharing 37
   - 6.16 Phase Adding/Dropping 38
   - 6.17 Monitoring via I^2C/SMBus 39
   - 6.18 *Snapshot*™ Parameter Capture 39
   - 6.19 Non-Volatile Memory and Device Security Features 40

7. Package Dimensions 41
8. Ordering Information 42
9. Related Tools and Documentation 42
10. Revision History 43

1. Electrical Characteristics

Table 1. Absolute Maximum Ratings

Operating beyond these limits may cause permanent damage to the device. Functional operation beyond the Recommended Operating Conditions is not implied. Voltage measured with respect to SGND.

Parameter	Pin	Value	Unit
DC supply voltage	VDD	- 0.3 to 17	V
MOSFET drive reference	VR	- 0.3 to 6.5	V
		120	mA
2.5 V logic reference	V25	- 0.3 to 3	V
		120	mA
Logic I/O voltage	CFG, DLY(0,1), DDC, EN, FC(0,1), ILIM(0,1), MGN, PG, SA(0,1), SALRT, SCL, SDA, SS, SYNC, UVLO, V(0,1)	- 0.3 to 6.5	V
Analog input voltages	ISENB, VSEN, VTRK, XTEMP	- 0.3 to 6.5	V
	ISENA	- 1.5 to 30	V
High side supply voltage	BST	- 0.3 to 30	V
Boost to switch voltage	BST - SW	- 0.3 to 8	V
High side drive voltage	GH	(V_{SW}-0.3) to (V_{BST}+0.3)	V
Low side drive voltage	GL	(PGND-0.3) to (VR+0.3)	V
Switch node continuous	SW	(PGND-0.3) to 30	V
Switch node transient (<100ns)	SW	(PGND-5) to 30	V
Ground differential	DGND – SGND, PGND - SGND	- 0.3 to 0.3	V
Junction temperature	–	- 55 to 150	°C
Storage temperature	–	- 55 to 150	°C
Lead temperature (Soldering, 10 s)	All	300	°C

Table 2. Recommended Operating Conditions and Thermal Information

Parameter	Symbol	Min	Typ	Max	Unit
Input supply voltage range, V_{DD} (See Figure 9)	V_{DD} tied to V_R	3.0	–	5.5	V
	V_R floating	4.5	–	14	V
Output voltage range[1]	V_{OUT}	0.54	–	5.5	V
Operating junction temperature range	T_J	- 40	–	125	°C
Junction to ambient thermal impedance[2]	Θ_{JA}	–	35	–	°C/W
Junction to case thermal impedance[3]	Θ_{JC}	–	5	–	°C/W

Notes:

1. Includes margin limits
2. Θ_{JA} is measured in free air with the device mounted on a multi-layer FR4 test board and the exposed metal pad soldered to a low impedance ground plane using multiple vias.
3. For Θ_{JC}, the “case” temperature is measured at the center of the exposed metal pad

Table 3. Electrical Specifications

V_{DD} = 12 V, T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Parameter	Conditions	Min (Note 10)	Typ	Max (Note 10)	Unit
Input and Supply Characteristics					
I_{DD} supply current at f_{SW} = 200 kHz I_{DD} supply current at f_{SW} = 1.4 MHz	GH, GL no load; MISC_CONFIG[7] = 1	– –	16 25	30 50	mA mA
I_{DDS} shutdown current	EN = 0 V No I^2C/SMBus activity	–	6.5	8	mA
VR reference output voltage	V_{DD} > 6 V, I_{VR} < 50 mA	4.5	5.2	5.5	V
V25 reference output voltage	V_R > 3 V, I_{V25} < 50 mA	2.25	2.5	2.75	V
Output Characteristics					
Output voltage adjustment range[1]	$V_{IN} > V_{OUT}$	0.6	–	5.0	V
Output voltage set-point resolution	Set using resistors	–	10	–	mV
	Set using I^2C/SMBus	–	±0.025	–	% FS[2]
Output voltage accuracy[3]	Includes line, load, temp	- 1	–	1	%
VSEN input bias current	VSEN = 5.5 V	–	110	200	µA
Current sense differential input voltage (ground referenced)	V_{ISENA} - V_{ISENB}	- 100	–	100	mV
Current sense differential input voltage (V_{OUT} referenced) (V_{OUT} must be less than 4.0 V)	V_{ISENA} - V_{ISENB}	- 50	–	50	mV
Current sense input bias current	Ground referenced	- 100	–	100	µA
Current sense input bias current (V_{OUT} referenced, V_{OUT} < 4.0 V)	ISENA	- 1	–	1	µA
	ISENB	- 100	–	100	µA
Soft start delay duration range[4]	Set using DLY pin or resistor	2	–	200	ms
	Set using I^2C/SMBus	0.002	–	500	s
Soft start delay duration accuracy	Turn-on delay (precise mode) [4,5] Turn-on delay (normal mode) [6] Turn-off delay [6]	– – –	±0.25 -0.25/+4 -0.25/+4	– – –	ms ms ms
Soft start ramp duration range	Set using SS pin or resistor	0	–	200	ms
	Set using I^2C	0	–	200	ms
Soft start ramp duration accuracy		–	100	–	µs

Notes:
1. Does not include margin limits.
2. Percentage of Full Scale (FS) with temperature compensation applied.
3. V_{OUT} measured at the termination of the VSEN+ and VSEN- sense points.
4. The device requires a delay period following an enable signal and prior to ramping its output. Precise timing mode limits this delay period to approx 2 ms, where in normal mode it may vary up to 4 ms.
5. Precise ramp timing mode is only valid when using EN pin to enable the device rather than PMBus enable.
6. The devices may require up to a 4 ms delay following the assertion of the enable signal (normal mode) or following the de-assertion of the enable signal.

Table 3. Electrical Characteristics (continued)

V_{DD} = 12 V, T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Parameter	Conditions	Min (Note 10)	Typ	Max (Note 10)	Unit
Logic Input/Output Characteristics					
Logic input bias current	EN,PG,SCL,SDA,SALRT pins	- 10	–	10	µA
MGN input bias current		- 1	–	1	mA
Logic input low, V_{IL}		–	–	0.8	V
Logic input OPEN (N/C)	Multi-mode logic pins	–	1.4	–	V
Logic input high, V_{IH}		2.0	–	–	V
Logic output low, V_{OL}	$I_{OL} \leq 4$ mA	–	–	0.4	V
Logic output high, V_{OH}	$I_{OH} \geq -2$ mA	2.25	–	–	V
Oscillator and Switching Characteristics					
Switching frequency range		200	–	1400	kHz
Switching frequency set-point accuracy	Predefined settings (See Table 16)	- 5	–	5	%
Maximum PWM duty cycle	Factory default	95	–	–	%
Minimum SYNC pulse width		150	–	–	ns
Input clock frequency drift tolerance	External clock source	- 13	–	13	%
Gate Drivers					
High-side driver voltage (V_{BST} - V_{SW})		–	4.5	–	V
High-side driver peak gate drive current (pull down)	(V_{BST} - V_{SW}) = 4.5 V	2	3	–	A
High-side driver pull-up resistance	(V_{BST} - V_{SW}) = 4.5 V, (V_{BST} - V_{GH}) = 50 mV	–	0.8	2	Ω
High-side driver pull-down resistance	(V_{BST} - V_{SW}) = 4.5 V, (V_{GH} - V_{SW}) = 50 mV	–	0.5	2	Ω
Low-side driver peak gate drive current (pull-up)	V_R = 5 V	–	2.5	–	A
Low-side driver peak gate drive current (pull-down)	V_R = 5 V	–	1.8	–	A
Low-side driver pull-up resistance	V_R = 5 V, (V_R - V_{GL}) = 50 mV	–	1.2	2	Ω
Low-side driver pull-down resistance	V_R = 5 V, (V_{GL} - PGND) = 50 mV	–	0.5	2	Ω
Switching timing GH rise and fall time	(V_{BST} - V_{SW}) = 4.5 V, C_{LOAD} = 2.2 nF	–	5	20	ns
GL rise and fall time	V_R = 5 V, C_{LOAD} = 2.2 nF	–	5	20	ns
Tracking					
VTRK input bias current	VTRK = 5.5 V	–	110	200	µA
VTRK tracking ramp accuracy	100% Tracking, V_{OUT} - VTRK	- 100	–	+ 100	mV
VTRK regulation accuracy	100% Tracking, V_{OUT} - VTRK	- 1	–	1	%

Table 3. Electrical Characteristics (continued)

V_{DD} = 12 V, T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Parameter	Conditions	Min (Note 10)	Typ	Max (Note 10)	Unit
Fault Protection Characteristics					
UVLO threshold range	Configurable via I²C/SMBus	2.85	–	16	V
UVLO set-point accuracy		- 150	–	150	mV
UVLO hysteresis	Factory default	–	3	–	%
	Configurable via I²C/SMBus	0	–	100	%
UVLO delay		–	–	2.5	µs
Power good V_{OUT} low threshold	Factory default	–	90	–	% V_{OUT}
Power good V_{OUT} high threshold	Factory default	–	115	–	% V_{OUT}
Power good V_{OUT} hysteresis	Factory default	–	5	–	%
Power good delay	Using pin-strap or resistor [7]	0	–	200	ms
	Configurable via I²C/SMBus	0	–	500	s
VSEN undervoltage threshold	Factory default	–	85	–	% V_{OUT}
	Configurable via I²C/SMBus	0	–	110	% V_{OUT}
VSEN overvoltage threshold	Factory default	–	115	–	% V_{OUT}
	Configurable via I²C/SMBus	0	–	115	% V_{OUT}
VSEN undervoltage hysteresis		–	5	–	% V_{OUT}
VSEN undervoltage/ overvoltage fault response time	Factory default	–	16	–	µs
	Configurable via I²C/SMBus	5	–	60	µs
Current limit set-point accuracy (V_{OUT} referenced)		–	±10	–	% FS[8]
Current limit set-point accuracy (Ground referenced)		–	±10	–	% FS[8]
Current limit protection delay	Factory default	–	5	–	t_{SW}[9]
	Configurable via I²C/SMBus	1	–	32	t_{SW}[9]
Temperature compensation of current limit protection threshold	Factory default		4400		ppm / °C
	Configurable via I²C/SMBus	100		12700	
Thermal protection threshold (junction temperature)	Factory default	–	125	–	°C
	Configurable via I²C/SMBus	- 40	–	125	°C
Thermal protection hysteresis		–	15	–	°C

Notes:

7. Factory default Power Good delay is set to the same value as the soft start ramp time.
8. Percentage of Full Scale (FS) with temperature compensation applied
9. $t_{SW} = 1/f_{SW}$, where f_{SW} is the switching frequency.
10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

2. Pin Descriptions

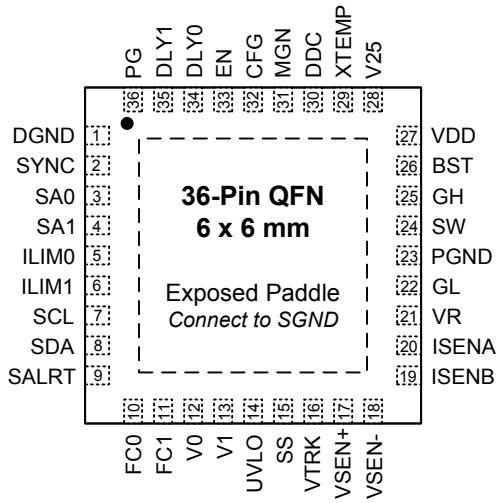


Figure 3. ZL2006 Pin Configurations (top view)

Table 4. Pin Descriptions

Pin	Label	Type[1]	Description
1	DGND	PWR	Digital ground. Common return for digital signals. Connect to low impedance ground plane.
2	SYNC	I/O,M[2]	Clock synchronization input. Used to set switching frequency of internal clock or for synchronization to external frequency reference.
3	SA0	I, M	Serial address select pins. Used to assign unique SMBus address to each IC or to enable certain management features.
4	SA1		
5	ILIM0	I, M	Current limit select. Sets the overcurrent threshold voltage for ISENA, ISENB.
6	ILIM1		
7	SCL	I/O	Serial clock. Connect to external host and/or to other ZL2006s.
8	SDA	I/O	Serial data. Connect to external host and/or to other ZL2006s.
9	SALRT	O	Serial alert. Connect to external host if desired.
10	FC0	I	Loop compensation selection pins.
11	FC1		
12	V0	I	Output voltage selection pins. Used to set V_{OUT} set-point and V_{OUT} max.
13	V1		
14	UVLO	I, M	Undervoltage lockout selection. Sets the minimum value for V_{DD} voltage to enable V_{OUT}.
15	SS	I, M	Soft start pin. Set the output voltage ramp time during turn-on and turnoff.
16	VTRK	I	Tracking sense input. Used to track an external voltage source.
17	VSEN+	I	Output voltage feedback. Connect to output regulation point.

Notes:

1. I = Input, O = Output, PWR = Power or Ground. M = Multi-mode pins.
2. The SYNC pin can be used as a logic pin, a clock input or a clock output.

Table 4. Pin Descriptions (continued)

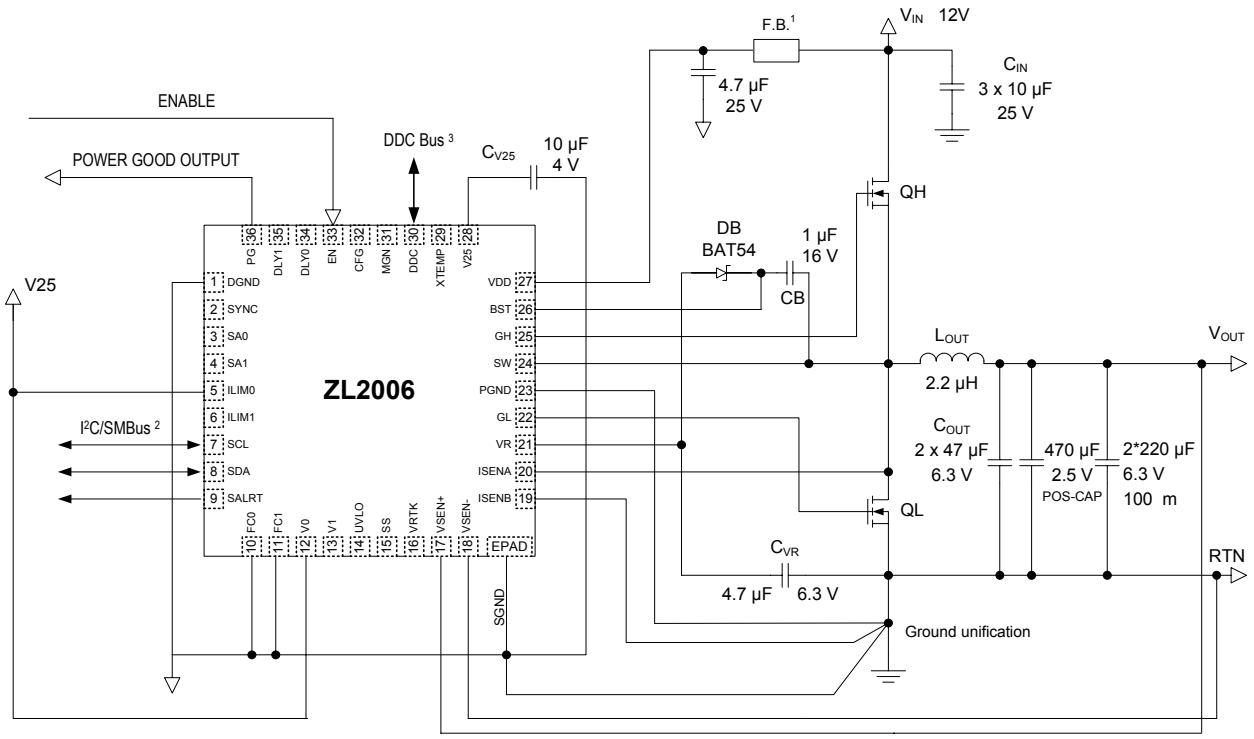
Pin	Label	Type[1]	Description
18	VSEN-	I	Output voltage feedback. Connect to load return or ground regulation point.
19	ISENB	I	Differential voltage input for current limit.
20	ISENA	I	Differential voltage input for current limit. High voltage tolerant.
21	VR	PWR	Internal 5V reference used to power internal drivers.
22	GL	O	Low side FET gate drive.
23	PGND	PWR	Power ground. Connect to low impedance ground plane.
24	SW	PWR	Drive train switch node.
25	GH	O	High-side FET gate drive.
26	BST	PWR	High-side drive boost voltage.
27	VDD[3]	PWR	Supply voltage.
28	V25	PWR	Internal 2.5 V reference used to power internal circuitry.
29	XTEMP	I	External temperature sensor input. Connect to external 2N3904 diode connected transistor.
30	DDC	I/O	Digital-DC Bus. (Open Drain) Communication between Zilker Labs devices.
31	MGN	I	Signal that enables margining of output voltage.
32	CFG	I, M	Configuration pin. Used to control the switching phase offset, sequencing and other management features.
33	EN	I	Enable input. Active high signal enables PWM switching.
34	DLY0	I, M	Softstart delay select. Sets the delay from when EN is asserted until the output voltage starts to ramp.
35	DLY1		
36	PG	O	Power good output.
ePad	SGND	PWR	Exposed thermal pad. Common return for analog signals; internal connection to SGND. Connect to low impedance ground plane.

Notes:

1. I = Input, O = Output, PWR = Power or Ground. M = Multi-mode pins. Please refer to Section 4.4“Multi-mode Pins,” on page 13.
2. The SYNC pin can be used as a logic pin, a clock input or a clock output.
3. V_{DD} is measured internally and the value is used to modify the PWM loop gain.

3. Typical Application Circuit

The following application circuit represents a typical implementation of the ZL2006. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.



Notes:
1. Ferrite bead is optional for input noise suppression
2. The I²C/SMBus requires pull-up resistors. Please refer to the I²C/SMBus specifications for more details.
3. The DDC bus requires a pull-up resistor. The resistance will vary based on the capacitive loading of the bus (and on the number of devices connected). The 10 kΩ default value, assuming a maximum of 100 pF per device, provides the necessary 1 µs pull-up rise time. Please refer to the DDC Bus section for more details.

Figure 4. 12 V to 1.8 V / 20 A Application Circuit (4.5 V UVLO, 10 ms SS delay, 5 ms SS ramp)

4. ZL2006 Overview

4.1 Digital-DC Architecture

The ZL2006 is an innovative mixed-signal power conversion and power management IC based on Zilker Labs patented Digital-DC technology that provides an integrated, high performance step-down converter for a wide variety of power supply applications.

Today's embedded power systems are typically designed for optimal efficiency at maximum load, reducing the peak thermal stress by limiting the total thermal dissipation inside the system. Unfortunately, many of these systems are often operated at load levels far below the peak where the power system has been optimized, resulting in reduced efficiency. While this may not cause thermal stress to occur, it does contribute to higher electricity usage and results in higher overall system operating costs.

Zilker Labs' efficiency-adaptive ZL2006 DC-DC controller helps mitigate this scenario by enabling the power converter to automatically change their operating state to increase efficiency and overall performance with little or no user interaction needed.

Its unique PWM loop utilizes an ideal mix of analog and digital blocks to enable precise control of the entire power conversion process with no software required, resulting in a very flexible device that is also very easy to use. An extensive set of power management functions are fully integrated and can be configured using simple pin connections. The user configuration can be saved in an internal non-volatile memory (NVM). Additionally, all functions can be configured and monitored via the SMBus hardware interface using standard PMBus commands, allowing ultimate flexibility.

Once enabled, the ZL2006 is immediately ready to regulate power and perform power management tasks with no programming required. Advanced configuration options and real-time configuration changes are available via the I^2C/SMBus interface if desired and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated sub-regulation circuitry enables single supply operation from any supply between 3 V and 14 V with no secondary bias supplies needed.

The ZL2006 can be configured by simply connecting its pins according to the tables provided in the following sections. Additionally, a comprehensive set of online tools and application notes are available to help simplify the design process. An evaluation board is also available to help the user become familiar with the device. This board can be evaluated as a standalone platform using pin configuration settings. A Windows™-based GUI is also provided to enable full configuration and monitoring capability via the I^2C/SMBus interface using an available computer and the included USB cable.

Application notes and reference designs are available to assist the user in designing to specific application demands. Please register for My ZL on www.zilkerlabs.com to access the most up-to-date documentation or call your local Zilker Labs sales office to order an evaluation kit.

4.2 Power Conversion Overview

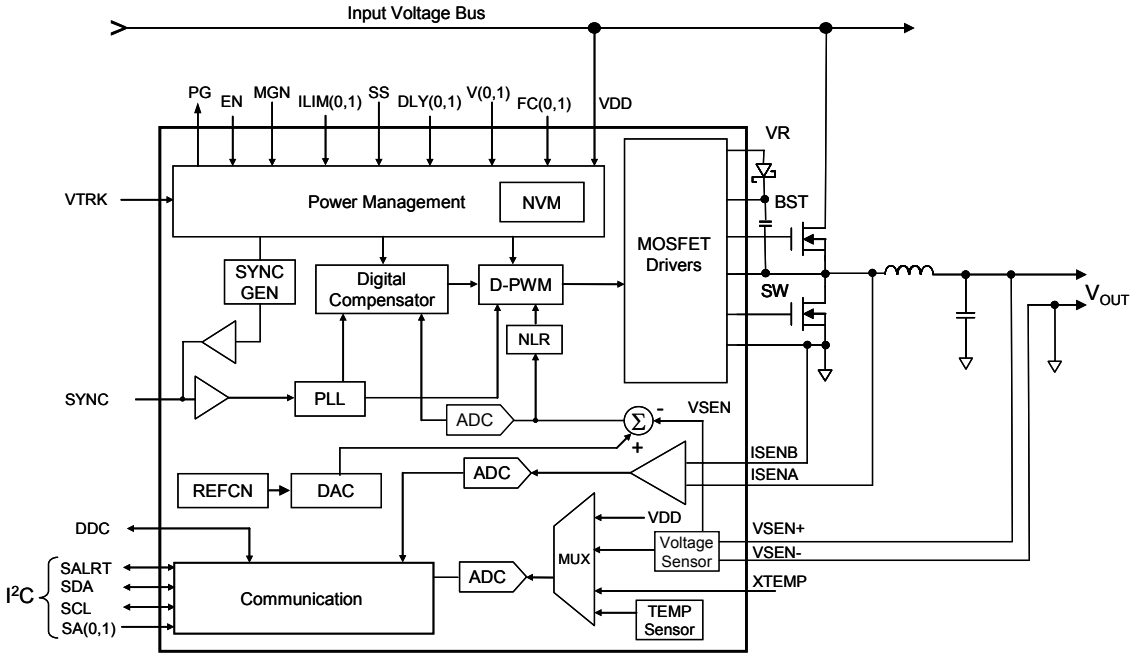


Figure 5. ZL2006 Block Diagram

The ZL2006 operates as a voltage-mode, synchronous buck converter with a selectable constant frequency pulse width modulator (PWM) control scheme that uses external MOSFETs, capacitors, and an inductor to perform power conversion.

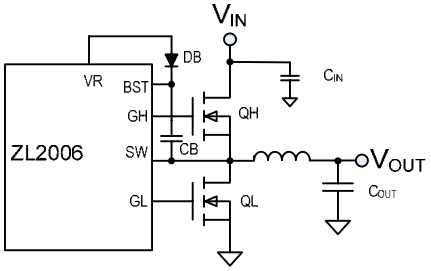


Figure 6. Synchronous Buck Converter

Figure 6 illustrates the basic synchronous buck converter topology showing the primary power train components. This converter is also called a step-down converter, as the output voltage must always be lower than the input voltage. In its most simple configuration, the ZL2006 requires two external N-channel power MOSFETs, one for the top control MOSFET (QH) and one for the bottom synchronous MOSFET (QL). The amount of time that QH is on as a fraction of the total switching period is known as the duty cycle *D*, which is described by the following equation:

$$D \approx \frac{V_{OUT}}{V_{IN}}$$

During time D, QH is on and $V_{IN} - V_{OUT}$ is applied across the inductor. The current ramps up as shown in Figure 7.

When QH turns off (time 1-D), the current flowing in the inductor must continue to flow from the ground up through QL, during which the current ramps down. Since the output capacitor C_{OUT} exhibits a low impedance at the switching frequency, the AC component of the inductor current is filtered from the output voltage so the load sees nearly a DC voltage.

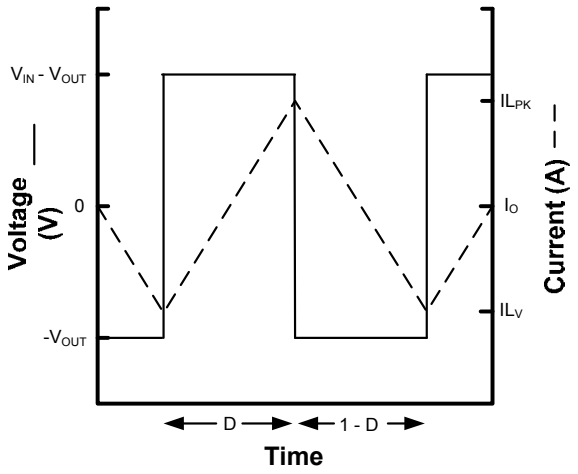


Figure 7. Inductor Waveform

Typically, buck converters specify a maximum duty cycle that effectively limits the maximum output voltage that can be realized for a given input voltage. This duty cycle limit ensures that the lowside MOSFET is allowed to turn on for a minimum amount of time during each switching cycle, which enables the bootstrap capacitor (CB in Figure 6) to be charged up and provide adequate gate drive voltage for the high-side MOSFET. See Section 5.2, "High-side Driver Boost Circuit," for more details.

In general, the size of components L1 and C_{OUT} as well as the overall efficiency of the circuit are inversely proportional to the switching frequency, f_{SW}. Therefore, the highest efficiency circuit may be realized by switching the MOSFETs at the lowest possible frequency; however, this will result in the largest component size. Conversely, the smallest possible footprint may be realized by switching at the fastest possible frequency but this gives a somewhat lower efficiency. Each user should determine the optimal combination of size and efficiency when determining the switching frequency for each application.

The block diagram for the ZL2006 is illustrated in Figure 5. In this circuit, the target output voltage is regulated by connecting the differential VSEN pins directly to the output regulation point. The VSEN signal is then compared to a reference voltage that has been set to the desired output voltage level by the user. The error signal derived from this comparison is converted to a digital value with a low-resolution, analog to digital (A/D) converter. The digital signal is applied to an adjustable digital compensation filter, and the compensated signal is used to derive the appropriate PWM duty cycle for driving the external MOSFETs in a way that produces the desired output.

The ZL2006 has several features to improve the power conversion efficiency. A non-linear response (NLR) loop improves the response time and reduces the output deviation as a result of a load transient. The ZL2006 monitors the power converter's operating conditions and continuously adjusts the turn-on and turn-off timing of the high-side and low-side MOSFETs to optimize the overall efficiency of the power supply. Adaptive performance optimization algorithms such as dead-time control, diode emulation, and frequency control are available to provide greater efficiency improvement.

4.3 Power Management Overview

The ZL2006 incorporates a wide range of configurable power management features that are simple to implement with no external components. Additionally, the ZL2006 includes circuit protection features that continuously safeguard the device and load from damage due to unexpected system faults. The ZL2006 can continuously monitor input voltage, output voltage/current, internal temperature, and the temperature of an external thermal diode. A Power Good output signal is also included to enable power-on reset functionality for an external processor.

All power management functions can be configured using either pin configuration techniques (see Figure 8) or via the I^2C/SMBus interface. Monitoring parameters can also be pre-configured to provide alerts for specific conditions. See Application Note AN33 for more details on SMBus monitoring.

4.4 Multi-mode Pins

In order to simplify circuit design, the ZL2006 incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device with no programming. Most power management features can be configured using these pins. The multi-mode pins can respond to four different connections as shown in Table 5. These pins are sampled when power is applied or by issuing a PMBus Restore command (See Application Note AN33).

Pin-strap Settings: This is the simplest implementation method, as no external components are required. Using this method, each pin can take on one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to the V25 pin for logic HIGH settings as this pin provides a regulated voltage higher than 2 V. Using a single pin, one of three settings can be selected. Using two pins, one of nine settings can be selected.

Table 5. Multi-mode Pin Configuration

Pin Tied To	Value
LOW (Logic LOW)	< 0.8 VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	> 2.0 VDC
Resistor to SGND	Set by resistor value

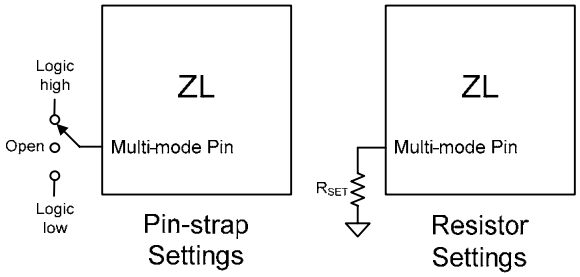


Figure 8. Pin-strap and Resistor Setting Examples

Resistor Settings: This method allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multi-mode pin and SGND. Standard 1% resistor values are used, and only every fourth E96 resistor value is used so the device can reliably recognize the value of resistance connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

I^2C/SMBus Method: Almost any ZL2006 function can be configured via the I^2C/SMBus interface using standard PMBus commands. Additionally, any value that has been configured using the pin-strap or resistor setting methods can also be re-configured and/or verified via the I^2C/SMBus. See Application Note AN33 for more details.

The SMBus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set via the I^2C/SMBus. The device address is set using the SA0 and SA1 pins. VOUT_MAX is determined as 10% greater than the voltage set by the V0 and V1 pins.

5. Power Conversion Functional Description

5.1 Internal Bias Regulators and Input Supply Connections

The ZL2006 employs two internal low dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

VR: The VR LDO provides a regulated 5 V bias supply for the MOSFET driver circuits. It is powered from the VDD pin. A 4.7 µF filter capacitor is required at the VR pin.

V25: The V25 LDO provides a regulated 2.5 V bias supply for the main controller circuitry. It is powered from an internal 5V node. A 10 µF filter capacitor is required at the V25 pin.

When the input supply (VDD) is higher than 5.5 V, the VR pin should not be connected to any other pins. It should only have a filter capacitor attached as shown in Figure 9. Due to the dropout voltage associated with the VR bias regulator, the VDD pin must be connected to the VR pin for designs operating from a supply below 5.5 V. Figure 9 illustrates the required connections for both cases.

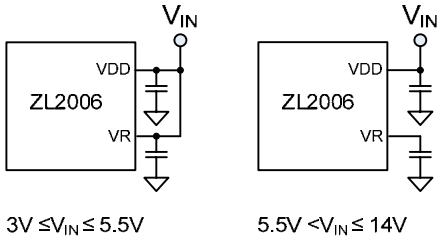


Figure 9. Input Supply Connections

Note: the internal bias regulators are not designed to be outputs for powering other circuitry. Do not attach external loads to any of these pins. The multi-mode pins may be connected to the V25 pin for logic HIGH settings.

5.2 High-side Driver Boost Circuit

The gate drive voltage for the high-side MOSFET driver is generated by a floating bootstrap capacitor, CB (see Figure 6). When the lower MOSFET (QL) is turned on, the SW node is pulled to ground and the capacitor is charged from the internal VR bias regulator through diode DB. When QL turns off and the upper MOSFET (QH) turns on, the SW node is pulled up to V_{DD} and the voltage on the bootstrap capacitor is boosted approximately 5 V above V_{DD} to provide the necessary voltage to power the high-side driver. A Schottky diode should be used for DB to help maximize the high-side drive supply voltage.

5.3 Output Voltage Selection

5.3.1 Standard Mode

The output voltage may be set to any voltage between 0.6 V and 5.0 V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification. Using the pin-strap method, V_{OUT} can be set to any of nine standard voltages as shown in Table 6.

Table 6. Pin-strap Output Voltage Settings

		V0		
		LOW	OPEN	HIGH
V1	LOW	0.6 V	0.8 V	1.0 V
	OPEN	1.2 V	1.5 V	1.8 V
	HIGH	2.5 V	3.3 V	5.0 V

The resistor setting method can be used to set the output voltage to levels not available in Table 6. Resistors R0 and R1 are selected to produce a specific voltage between 0.6 V and 5.0 V in 10 mV steps. Resistor R1 provides a coarse setting and resistor R0 provides a fine adjustment, thus eliminating the additional errors associated with using two 1% resistors (this typically adds approx 1.4% error).

To set V_{OUT} using resistors, follow the steps below to calculate an index value and then use Table 7 to select the resistor that corresponds to the calculated index value as follows:

1. Calculate Index1:
   Index1 = 4 x V_{OUT} (V_{OUT} in 10 mV steps)
2. Round the result down to the nearest whole number.
3. Select the value of R1 from Table 7 using the Index1 rounded value from step 2.
4. Calculate Index0:
   Index0 = 100 x V_{OUT} – (25 x Index1)
5. Select the value of R0 from Table 7 using the Index0 value from step 4.

Table 7. Resistors for Setting Output Voltage

Index	R0 or R1	Index	R0 or R1
0	10 kΩ	13	34.8 kΩ
1	11 kΩ	14	38.3 kΩ
2	12.1 kΩ	15	42.2 kΩ
3	13.3 kΩ	16	46.4 kΩ
4	14.7 kΩ	17	51.1 kΩ
5	16.2 kΩ	18	56.2 kΩ
6	17.8 kΩ	19	61.9 kΩ
7	19.6 kΩ	20	68.1 kΩ
8	21.5 kΩ	21	75 kΩ
9	23.7 kΩ	22	82.5 kΩ
10	26.1 kΩ	23	90.9 kΩ
11	28.7 kΩ	24	100 kΩ
12	31.6 kΩ		

Example from Figure 10: For V_{OUT} = 1.33 V,

Index1 = 4 x 1.33 V = 5.32;
From Table 7, R1 = 16.2 kΩ

Index0 = (100 x 1.33 V) – (25 x 5) = 8;
From Table 7, R0 = 21.5 kΩ

The output voltage can be determined from the R0 (Index0) and R1 (Index1) values using the following equation:

$$V_{OUT} = \frac{Index0 + (25 \times Index1)}{100}$$

5.3.2 SMBus Mode

The output voltage may be set to any value between 0.6 V and 5.0 V using a PMBus command over the I^2C/SMBus interface. See Application Note AN33 for details.

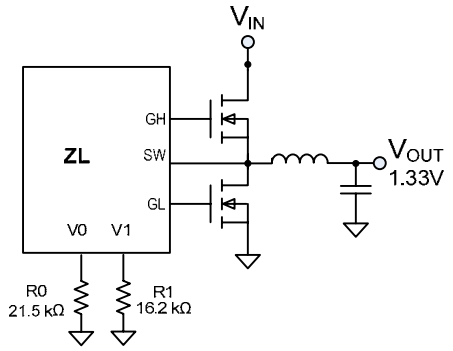


Figure 10. Output Voltage Resistor Setting Example

5.3.3 POLA Voltage Trim Mode

The output voltage mapping can be changed to match the voltage setting equations for POLA and DOSA standard modules.

The standard method for adjusting the output voltage for a POLA module is defined by the following equation:

$$R_{SET} = 10k\Omega \times \frac{0.69V}{V_{OUT} - 0.69V} - 1.43k\Omega$$

The resistor, R_{SET}, is external to the POLA module. See Figure 11.

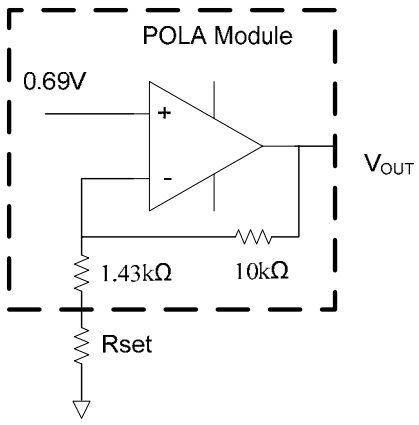


Figure 11. Output Voltage Setting on POLA Module

To stay compatible with this existing method for adjusting the output voltage, the module manufacturer should add a 10kΩ resistor on the module as shown in Figure 12. Now, the same R_{SET} used for an analog POLA module will provide the same output voltage when using a digital POLA module based on the ZL2006.

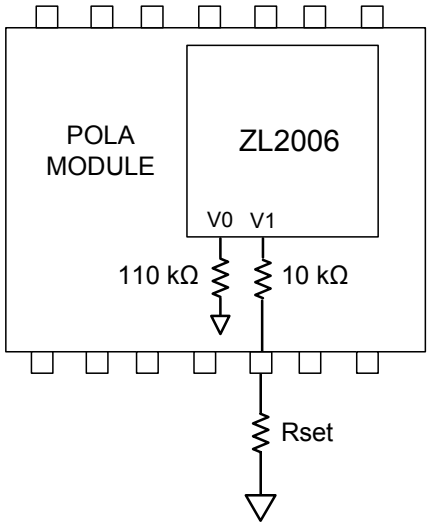


Figure 12. R_{SET} on a POLA Module

The POLA mode is activated through pin-strap by connecting a 110 kΩ resistor on V0 to SGND. The V1 pin is then used to adjust the output voltage as shown in Table 8.

Table 8. POLA Mode V_{OUT} Settings
(R0 = 110 kΩ, R1 = R_{SET} + 10 kΩ)

V_{OUT}	R_{SET} In series with 10kΩ resistor	V_{OUT}	R_{SET} In series with 10kΩ resistor
0.700 V	162 kΩ	0.991 V	21.5 kΩ
0.752 V	110 kΩ	1.000 V	19.6 kΩ
0.758 V	100 kΩ	1.100 V	16.2 kΩ
0.765 V	90.9 kΩ	1.158 V	13.3 kΩ
0.772 V	82.5 kΩ	1.200 V	12.1 kΩ
0.790 V	75.0 kΩ	1.250 V	9.09 kΩ
0.800 V	56.2 kΩ	1.500 V	7.50 kΩ
0.821 V	51.1 kΩ	1.669 V	5.62 kΩ
0.834 V	46.4 kΩ	1.800 V	4.64 kΩ
0.848 V	42.2 kΩ	2.295 V	2.87 kΩ
0.880 V	34.8 kΩ	2.506 V	2.37 kΩ
0.899 V	31.6 kΩ	3.300 V	1.21 kΩ
0.919 V	28.7 kΩ	5.000 V	0.162 kΩ
0.965 V	23.7 kΩ		

5.3.4 DOSA Voltage Trim Mode

On a DOSA module, the V_{OUT} setting follows this equation:

$$R_{SET} = \frac{6900}{V_{OUT} - 0.69V}$$

To maintain DOSA compatibility, the same scheme is used as with a POLA module except the 10 kΩ resistor is replaced with a 8.66 kΩ resistor as shown in Figure 13.

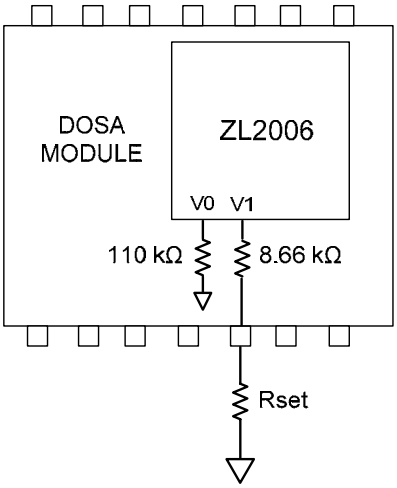


Figure 13. R_{SET} on a DOSA Module

The DOSA mode V_{OUT} settings are listed in Table 9.

Table 9. DOSA Mode V_{OUT} Settings
(R0 = 110 kΩ, R1 = R_{SET} + 8.66 kΩ)

V_{OUT}	R_{SET} In series with 8.66kΩ resistor	V_{OUT}	R_{SET} In series with 8.66kΩ resistor
0.700 V	162 kΩ	0.991 V	22.6 kΩ
0.752 V	113 kΩ	1.000 V	21.0 kΩ
0.758 V	100 kΩ	1.100 V	17.8 kΩ
0.765 V	90.9 kΩ	1.158 V	14.7 kΩ
0.772 V	82.5 kΩ	1.200 V	13.3 kΩ
0.790 V	75.0 kΩ	1.250 V	10.5 kΩ
0.800 V	57.6 kΩ	1.500 V	8.87 kΩ
0.821 V	52.3 kΩ	1.669 V	6.98 kΩ
0.834 V	47.5 kΩ	1.800 V	6.04 kΩ
0.848 V	43.2 kΩ	2.295 V	4.32 kΩ
0.880 V	36.5 kΩ	2.506 V	3.74 kΩ
0.899 V	33.2 kΩ	3.300 V	2.61 kΩ
0.919 V	30.1 kΩ	5.000 V	1.50 kΩ
0.965 V	25.5 kΩ		

5.4 Start-up Procedure

The ZL2006 follows a specific internal start-up procedure after power is applied to the VDD pin. Table 10 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. The device requires approximately 5-10 ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the I^2C/SMBus interface and the device is ready to be enabled. Once enabled, the device requires approximately 2 ms before its output voltage may be allowed to start its ramp-up process. If a soft-start delay period less than 2 ms has been configured (using DLY pins or PMBus commands), the device will default to a 2 ms delay period. If a delay period greater than 2 ms is configured, the device will wait for the configured delay period prior to starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the pre-configured soft-start ramp time that has been set using the SS pin. It should be noted that if the EN pin is tied to VDD, the device will still require approx 5-10 ms before the output can begin its ramp-up as described in Table 10 below.

5.5 Soft Start Delay and Ramp Times

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ZL2006 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires. The soft-start delay period is set using the DLY (0,1) pins. Precise ramp delay timing reduces the delay time variations but is only available when the appropriate bit in the MISC_CONFIG register has been set. Please refer to Application Note AN33 for details.

The soft-start ramp timer enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the delay period has expired. The ramp-up is guaranteed monotonic and its slope may be precisely set using the SS pin.

The soft start delay and ramp times can be set to standard values according to Table 11 and Table 12 respectively.

Table 10. ZL2006 Start-up Sequence

Step #	Step Name	Description	Time Duration
1	Power Applied	Input voltage is applied to the ZL2006's VDD pin	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approx 5-10 ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by the multi-mode pins.	
4	Device Ready	The device is ready to accept an enable signal.	—
5	Pre-ramp Delay	The device requires approximately 2 ms following an enable signal and prior to ramping its output. Additional pre-ramp delay may be configured using the Delay pins.	Approximately 2 ms

Table 11. Soft Start Delay Settings

		DLY0		
		LOW	OPEN	HIGH
DLY1	LOW	0 ms[1]	1 ms[1]	2 ms
	OPEN	5 ms	10 ms	20 ms
	HIGH	50 ms	100 ms	200 ms

Note:
1. When the device is set to 0 ms or 1 ms delay, it will begin its ramp up after the internal circuitry has initialized (approx. 2 ms).

Table 12. Soft Start Ramp Settings

SS	Ramp Time
LOW	0 ms [2]
OPEN	5 ms
HIGH	10 ms

Note:
2. When the device is set to 0 ms ramp, it will attempt to ramp as fast as the external load capacitance and loop settings will allow. It is generally recommended to set the soft-start ramp to a value greater than 500 µs to prevent inadvertent fault conditions due to excessive inrush current.

If the desired soft start delay and ramp times are not one of the values listed in Table 11 and Table 12, the times can be set to a custom value by connecting a resistor from the DLY0 or SS pin to SGND using the appropriate resistor value from Table 13. The value of this resistor is measured upon start-up or Restore and will not change if the resistor is varied after power has been applied to the ZL2006. See Figure 14 for typical connections using resistors.

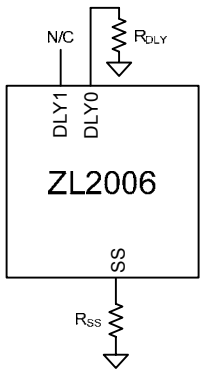


Figure 14. DLY and SS Pin Resistor Connections

Table 13. DLY and SS Resistor Settings

DLY or SS	R_{DLY} or R_{SS}
0 ms [2]	10 kΩ
10 ms	11 kΩ
20 ms	12.1 kΩ
30 ms	13.3 kΩ
40 ms	14.7 kΩ
50 ms	16.2 kΩ
60 ms	17.8 kΩ
70 ms	19.6 kΩ
80 ms	21.5 kΩ
90 ms	23.7 kΩ
100 ms	26.1 kΩ
110 ms	28.7 kΩ
120 ms	31.6 kΩ
130 ms	34.8 kΩ
140 ms	38.3 kΩ
150 ms	42.2 kΩ
160 ms	46.4 kΩ
170 ms	51.1 kΩ
180 ms	56.2 kΩ
190 ms	61.9 kΩ
200 ms	68.1 kΩ

Note: Do not connect a resistor to the DLY1 pin. This pin is not utilized for setting soft-start delay times. Connecting an external resistor to this pin may cause conflicts with other device settings.

The soft start delay and ramp times can also be set to custom values via the I^2C/SMBus interface. When the SS delay time is set to 0 ms, the device will begin its ramp-up after the internal circuitry has initialized (approx. 2 ms). When the soft-start ramp period is set to 0 ms, the output will ramp up as quickly as the output load capacitance and loop settings will allow. It is generally recommended to set the soft-start ramp to a value greater than 500 µs to prevent inadvertent fault conditions due to excessive inrush current.

5.6 Power Good

The ZL2006 provides a Power Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within -10%/+15% of the target voltage. These limits and the polarity of the pin may be changed via the I^2C/SMBus interface. See Application Note AN33 for details.

A PG delay period is defined as the time from when all conditions within the ZL2006 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL2006 PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 10 ms, the PG delay will be set to 10 ms. The PG delay may be set independently of the soft-start ramp using the I^2C/SMBus as described in Application Note AN33.

5.7 Switching Frequency and PLL

The ZL2006 incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Zilker Labs devices.

The SYNC pin is a unique pin that can perform multiple functions depending on how it is configured. The CFG pin is used to select the operating mode of the SYNC pin as shown in Table 14. Figure 15 illustrates the typical connections for each mode.

Table 14. SYNC Pin Function Selection

CFG Pin	SYNC Pin Function
LOW	SYNC is configured as an input
OPEN	Auto Detect mode
HIGH	SYNC is configured as an output f_{SW} = 400 kHz

Configuration A: SYNC OUTPUT

When the SYNC pin is configured as an output (CFG pin is tied HIGH), the device will run from its internal oscillator and will drive the resulting internal oscillator signal (preset to 400 kHz) onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode.

Configuration B: SYNC INPUT

When the SYNC pin is configured as an input (CFG pin is tied LOW), the device will automatically check for a clock signal on the SYNC pin each time EN is asserted. The ZL2006's oscillator will then synchronize with the rising edge of the external clock.

The incoming clock signal must be in the range of 200 kHz to 1.4 MHz and must be stable when the enable pin is asserted. The clock signal must also exhibit the necessary performance requirements (see Table 3). In the event of a loss of the external clock signal, the output voltage may show transient over/undershoot.

If this happens, the ZL2006 will automatically switch to its internal oscillator and switch at a frequency close to the previous incoming frequency.

Configuration C: SYNC AUTO DETECT

When the SYNC pin is configured in auto detect mode (CFG pin is left OPEN), the device will automatically check for a clock signal on the SYNC pin after enable is asserted.

If a clock signal is present, The ZL2006's oscillator will then synchronize the rising edge of the external clock. Refer to SYNC INPUT description.

If no incoming clock signal is present, the ZL2006 will configure the switching frequency according to the state of the SYNC pin as listed in Table 15. In this mode, the ZL2006 will only read the SYNC pin connection during the start-up sequence. Changes to SYNC pin connections will not affect f_{SW} until the power (VDD) is cycled off and on.

Table 15. Switching Frequency Selection

SYNC Pin	Frequency
LOW	200 kHz
OPEN	400 kHz
HIGH	1 MHz
Resistor	See Table 16

If the user wishes to run the ZL2006 at a frequency not listed in Table 15, the switching frequency can be set using an external resistor, R_{SYNC}, connected between SYNC and SGND using Table 16.

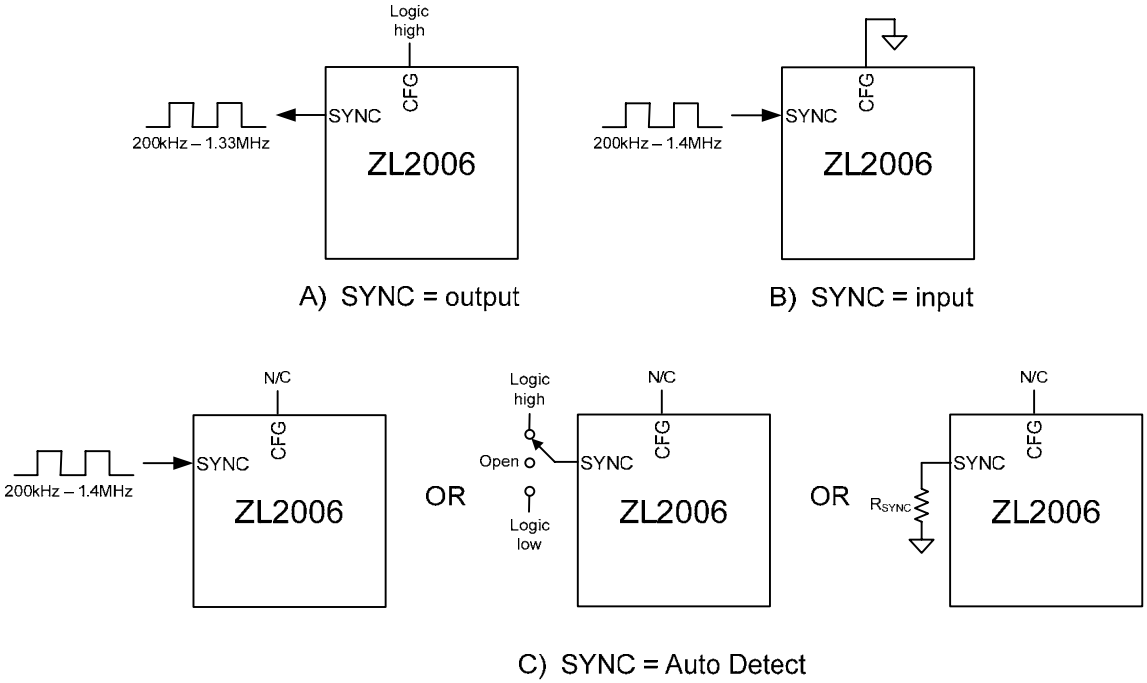


Figure 15. SYNC Pin Configurations

Table 16. R_{SYNC} Resistor Values

R_{SYNC}	f_{SW}	R_{SYNC}	f_{SW}
10 kΩ	200 kHz	26.1 kΩ	533 kHz
11 kΩ	222 kHz	28.7 kΩ	571 kHz
12.1 kΩ	242 kHz	31.6 kΩ	615 kHz
13.3 kΩ	267 kHz	34.8 kΩ	727 kHz
14.7 kΩ	296 kHz	38.3 kΩ	800 kHz
16.2 kΩ	320 kHz	46.4 kΩ	889 kHz
17.8 kΩ	364 kHz	51.1 kΩ	1000 kHz
19.6 kΩ	400 kHz	56.2 kΩ	1143 kHz
21.5 kΩ	421 kHz	68.1 kΩ	1333 kHz
23.7 kΩ	471 kHz		

The switching frequency can also be set to any value between 200 kHz and 1.33 MHz using the I^2C/SMBus interface. The available frequencies below 1.4 MHz are defined by f_{SW} = 8 MHz/N, where the whole number N is $6 \leq N \leq 40$. See Application Note AN33 for details.

If a value other than f_{SW} = 8 MHz/N is entered using a PMBus command, the internal circuitry will select the valid switching frequency value that is closest to the entered value. For example, if 810 kHz is entered, the device will select 800 kHz (N=10).

When multiple Zilker Labs devices are used together, connecting the SYNC pins together will force all devices to synchronize with each other. The CFG pin of one device must set its SYNC pin as an output and the remaining devices must have their SYNC pins set as Auto Detect.

Note: The switching frequency read back using the appropriate PMBus command will differ slightly from the selected values in Table 16. The difference is due to hardware quantization.

5.8 Power Train Component Selection

The ZL2006 is a synchronous buck converter that uses external MOSFETs, inductor and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance.

To select the appropriate external components for the desired performance goals, the power supply requirements listed in Table 17 must be known.

Table 17. Power Supply Requirements

Parameter	Range	Example Value
Input voltage (V_{IN})	3.0 – 14.0 V	12 V
Output voltage (V_{OUT})	0.6 – 5.0 V	1.2 V
Output current (I_{OUT})	0 to ~25 A	20 A
Output voltage ripple (V_{orip})	< 3% of V_{OUT}	1% of V_{OUT}
Output load step (I_{ostep})	< Io	50% of I_o
Output load step rate	—	10 A/µS
Output deviation due to load step	—	± 50 mV
Maximum PCB temp.	120°C	85°C
Desired efficiency	—	85%
Other considerations	Various	Optimize for small size

5.8.1 Design Goal Trade-offs

The design of the buck power stage requires several compromises among size, efficiency, and cost. The inductor core loss increases with frequency, so there is a trade-off between a small output filter made possible by a higher switching frequency and getting better power supply efficiency. Size can be decreased by increasing the switching frequency at the expense of efficiency. Cost can be minimized by using through-hole inductors and capacitors; however these components are physically large.

To start the design, select a switching frequency based on Table 18. This frequency is a starting point and may be adjusted as the design progresses.

Table 18. Circuit Design Considerations

Frequency Range	Efficiency	Circuit Size
200–400 kHz	Highest	Larger
400–800 kHz	Moderate	Smaller
800 kHz – 1.4 MHz	Lower	Smallest

5.8.2 Inductor Selection

The output inductor selection process must include several trade-offs. A high inductance value will result in a low ripple current (I_{opp}), which will reduce output capacitance and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be struck between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple equal to the expected load transient step magnitude (I_{ostep}):

$$I_{opp} = I_{ostep}$$

Now the output inductance can be calculated using the following equation, where V_{INM} is the maximum input voltage:

$$L_{OUT} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INM}}\right)}{fsw \times I_{opp}}$$

The average inductor current is equal to the maximum output current. The peak inductor current (I_{Lpk}) is calculated using the following equation where I_{OUT} is the maximum output current:

$$I_{Lpk} = I_{OUT} + \frac{I_{opp}}{2}$$

Select an inductor rated for the average DC current with a peak current rating above the peak current computed above.

In over-current or short-circuit conditions, the inductor may have currents greater than 2X the normal maximum rated output current. It is desirable to use an inductor that still provides some inductance to protect the load and the MOSFETs from damaging currents in this situation.

Once an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's datasheet.

$$P_{LDCR} = DCR \times I_{Lrms}^{2}$$

I_{Lrms} is given by

$$I_{Lrms} = \sqrt{I_{OUT}^{2} + \frac{(I_{opp})^2}{12}}$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor datasheet. Add the core loss and the ESR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

5.8.3 Output Capacitor Selection

Several trade-offs must also be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output ripple voltage to the capacitor ESR and the other half to capacitance, as shown in the following equations:

$$C_{OUT} = \frac{I_{opp}}{8 \times f_{sw} \times \frac{V_{orip}}{2}}$$

$$ESR = \frac{V_{orip}}{2 \times I_{opp}}$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using the following equation:

$$V_{orip} = I_{opp} \times ESR + \frac{I_{opp}}{8 \times f_{sw} \times C_{OUT}}$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

5.8.4 Input Capacitor

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5 or 12 V “bulk” supply from an off-line power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple (I_{CINrms}) can be determined from the following equation:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2X the ripple current calculated above to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage are recommended.

5.8.5 Bootstrap Capacitor Selection

The high-side driver boost circuit utilizes an external Schottky diode (D_B) and an external bootstrap capacitor (C_B) to supply sufficient gate drive for the high-side MOSFET driver. D_B should be a 20 mA, 30 V Schottky diode or equivalent device and C_B should be a 1 µF ceramic type rated for at least 6.3V.

5.8.6 QL Selection

The bottom MOSFET should be selected primarily based on the device's $R_{DS(ON)}$ and secondarily based on its gate charge. To choose QL, use the following equation and allow 2–5% of the output power to be dissipated in the $R_{DS(ON)}$ of QL (lower output voltages and higher step-down ratios will be closer to 5%):

$$P_{QL} = 0.05 \times V_{OUT} \times I_{OUT}$$

Calculate the RMS current in QL as follows:

$$I_{botrms} = I_{Lrms} \times \sqrt{1-D}$$

Calculate the desired maximum $R_{DS(ON)}$ as follows:

$$R_{DS(ON)} = \frac{P_{QL}}{(I_{botrms})^2}$$

Note that the $R_{DS(ON)}$ given in the manufacturer's datasheet is measured at 25°C. The actual $R_{DS(ON)}$ in the end-use application will be much higher. For example, a Vishay Si7114 MOSFET with a junction temperature of 125°C has an $R_{DS(ON)}$ that is 1.4 times higher than the value at 25°C. Select a candidate MOSFET, and calculate the required gate drive current as follows:

$$I_g = f_{SW} \times Q_g$$

Keep in mind that the total allowed gate drive current for both QH and QL is 80 mA.

MOSFETs with lower $R_{DS(ON)}$ tend to have higher gate charge requirements, which increases the current and resulting power required to turn them on and off. Since the MOSFET gate drive circuits are integrated in the ZL2006, this power is dissipated in the ZL2006 according to the following equation:

$$P_{QL} = f_{sw} \times Q_g \times V_{INM}$$

5.8.7 QH Selection

In addition to the $R_{DS(ON)}$ loss and gate charge loss, QH also has switching loss. The procedure to select QH is similar to the procedure for QL. First, assign 2–5% of the output power to be dissipated in the $R_{DS(ON)}$ of QH using the equation for QL above. As was done with QL, calculate the RMS current as follows:

$$I_{toprms} = I_{Lrms} \times \sqrt{D}$$

Calculate a starting $R_{DS(ON)}$ as follows, in this example using 5%:

$$P_{QH} = 0.05 \times V_{OUT} \times I_{OUT}$$

$$R_{DS(ON)} = \frac{P_{QH}}{(I_{toprms})^2}$$

Select a MOSFET and calculate the resulting gate drive current. Verify that the combined gate drive current from QL and QH does not exceed 80 mA.

Next, calculate the switching time using:

$$t_{SW} = \frac{Q_g}{I_{gdr}}$$

where Q_g is the gate charge of the selected QH and I_{gdr} is the peak gate drive current available from the ZL2006.

Although the ZL2006 has a typical gate drive current of 3 A, use the minimum guaranteed current of 2 A for a conservative design. Using the calculated switching time, calculate the switching power loss in QH using:

$$P_{swtop} = V_{INM} \times t_{sw} \times I_{OUT} \times f_{sw}$$

The total power dissipated by QH is given by the following equation:

$$P_{QHtot} = P_{QH} + P_{swtop}$$

5.8.8 MOSFET Thermal Check

Once the power dissipations for QH and QL have been calculated, the MOSFETs junction temperature can be estimated. Using the junction-to-case thermal resistance (R_{th}) given in the MOSFET manufacturer's datasheet and the expected maximum printed circuit board temperature, calculate the junction temperature as follows:

$$T_{j\max} = T_{pcb} + (P_Q \times R_{th})$$

5.8.9 Current Sensing Components

Once the current sense method has been selected (Refer to Section 5.9, "Current Limit Threshold Selection,"), the components are selected as follows.

When using the inductor DCR sensing method, the user must also select an R/C network comprised of R1 and CL (see Figure 16).

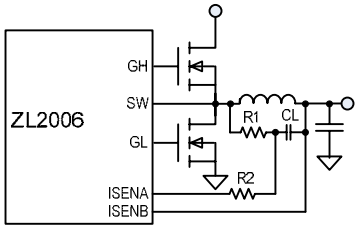


Figure 16. DCR Current Sensing

For the voltage across C_L to reflect the voltage across the DCR of the inductor, the time constant of the inductor must match the time constant of the RC network. That is:

$$\tau_{RC} = \tau_{L/DCR}$$

$$R_1 \cdot C_L = \frac{L}{DCR}$$

For L, use the average of the nominal value and the minimum value. Include the effects of tolerance, DC Bias and switching frequency on the inductance when determining the minimum value of L. Use the typical value for DCR.

The value of R_1 should be as small as feasible and no greater than 5 kΩ for best signal-to-noise ratio. The designer should make sure the resistor package size is appropriate for the power dissipated and include this loss in efficiency calculations. In calculating the minimum value of R_1, the average voltage across C_L (which is the average $I_{OUT} \cdot DCR$ product) is small and can be neglected. Therefore, the minimum value of R_1 may be approximated by the following equation:

$$R_{1-\min} = \frac{D\left(V_{IN-\max} - V_{OUT}\right)^2 + \left(1-D\right)\cdot {V_{OUT}}^2}{P_{R1\,pkg-\max} \cdot \delta_P},$$

where $P_{R1pkg\text{-max}}$ is the maximum power dissipation specification for the resistor package and δ_P is the derating factor for the same parameter (eg.: $P_{R1pkg\text{-max}}$ = 0.0625W for 0603 package, δ_P = 50% @ 85°C). Once $R_{1\text{-min}}$ has been calculated, solve for the maximum value of C_L from

$$C_{L-\max} = \frac{L}{R_{1-\min} \cdot DCR}$$

and choose the next-lowest readily available value (eg.: For $C_{L\text{-max}}$ = 1.86uF, C_L = 1.5uF is a good choice). Then substitute the chosen value into the same equation and re-calculate the value of R_1. Choose the 1% resistor standard value closest to this re-calculated value of R_1. The error due to the mismatch of the two time constants is

$$\varepsilon_\tau = \left(1 - \frac{R_1 \cdot C_L \cdot DCR}{L_{avg}}\right) \cdot 100\%$$

The value of R_2 should be simply five times that of R_1:

$$R_2 = 5 \cdot R_1$$

For the $R_{DS(ON)}$ current sensing method, the external low side MOSFET will act as the sensing element as indicated in Figure 17.

5.9 Current Limit Threshold Selection

It is recommended that the user include a current limiting mechanism in their design to protect the power supply from damage and prevent excessive current from being drawn from the input supply in the event that the output is shorted to ground or an overload condition is imposed on the output. Current limiting is accomplished by sensing the current through the circuit during a portion of the duty cycle.

Output current sensing can be accomplished by measuring the voltage across a series resistive sensing element according to the following equation:

$$V_{LIM} = I_{LIM} \times R_{SENSE}$$

Where:

I_{LIM} is the desired maximum current that should flow in the circuit

R_{SENSE} is the resistance of the sensing element

V_{LIM} is the voltage across the sensing element at the point the circuit should start limiting the output current.

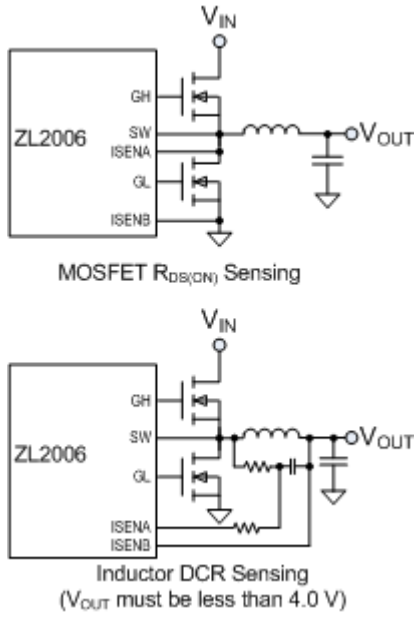


Figure 17. Current Sensing Methods

The ZL2006 supports "lossless" current sensing by measuring the voltage across a resistive element that is already present in the circuit. This eliminates additional efficiency losses incurred by devices that must use an additional series resistance in the circuit.

To set the current limit threshold, the user must first select a current sensing method. The ZL2006 incorporates two methods for current sensing, synchronous MOSFET $R_{DS(ON)}$ sensing and inductor DC resistance (DCR) sensing; Figure 17 shows a simplified schematic for each method.

The current sensing method can be selected using the ILIM1 pin using Table 19. The ILIM0 pin must have a finite resistor connected to ground in order for Table 19 to be valid. If no resistor is connected between ILIM0 and ground, the default method is MOSFET $R_{DS(ON)}$ sensing. The current sensing method can be modified via the I^2C/SMBus interface. Please refer to Application Note AN33 for details.

In addition to selecting the current sensing method, the ZL2006 gives the power supply designer several choices for the fault response during over or under current condition. The user can select the number of violations allowed before declaring fault, a blanking time and the action taken when a fault is detected.

Table 19. Resistor Settings for Current Sensing

ILIM0 Pin[1]	ILIM1 Pin	Current Limiting Configuration	Number of Violations Allowed[2]	Comments
R_{ILIM0}	LOW	Ground-referenced, $R_{DS(ON)}$, sensing Blanking time: 672 ns	5	Best for low duty cycle and low f_{SW}
R_{ILIM0}	OPEN	Output-referenced, down-slope sensing (Inductor DCR sensing) Blanking time: 352 ns	5	Best for low duty cycle and high f_{SW}
R_{ILIM0}	HIGH	Output-referenced, up-slope sensing (Inductor DCR sensing) Blanking time: 352 ns	5	Best for high duty cycle
	Resistor	Depends on resistor value used; see Table 20		

Notes:
1. 10 kΩ < R_{ILIM0} < 100 kΩ
2. The number of violations allowed prior to issuing a fault response.