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RECOMMENDED REPLACEMENT PART
ZL6105

Digital DC/DC Controller with Drivers and Pin-Strap Current Sharing

ZL2008

The ZL2008 is a digital power controller with integrated MOSFET drivers. Current sharing allows multiple devices to be connected in parallel to source loads with very high current demands. Adaptive performance optimization algorithms improve power conversion efficiency. Zilker Labs Digital-DC™ technology enables a blend of power conversion performance and power management features.

The ZL2008 is designed to be a flexible building block for DC power and can be easily adapted to designs ranging from a single-phase power supply operating from a 3.3V input to a multi-phase supply operating from a 12V input. The ZL2008 eliminates the need for complicated power supply managers as well as numerous external discrete components.

Key operating features can be configured by pin-straps, including compensation, current sharing and output voltage. The ZL2008 uses the I^2C/SMBus™ with PMBus™ protocol for communication with a host controller and the Digital-DC bus for communication between Zilker Labs devices.

Applications

- Servers/storage equipment
- Telecom/datacom equipment
- Power supply modules

Features

Power Conversion

- Efficient synchronous buck controller
- Adaptive light load efficiency optimization
- 3V to 14V input range
- 0.54V to 5.5V output range (with margin)
- POLA and DOSA voltage trim modes
- ±1% output voltage accuracy
- Internal 3A MOSFET drivers
- Fast load transient response
- Current sharing and phase interleaving
- *Snapshot™* parameter capture
- RoHS compliant (6mmx6mm) QFN package

Power Management

- Digital soft-start/stop
- Precision delay and ramp-up
- Power good/enable
- Voltage tracking, sequencing and margining
- Voltage, current and temperature monitoring
- I^2C/SMBus interface, PMBus compatible
- Output voltage and current protection
- Internal non-volatile memory (NVM)

Block Diagram

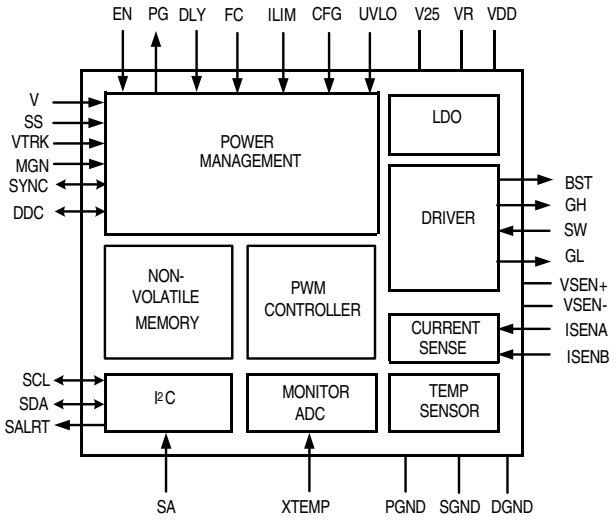


FIGURE 1. BLOCK DIAGRAM

Efficiency vs Load Current

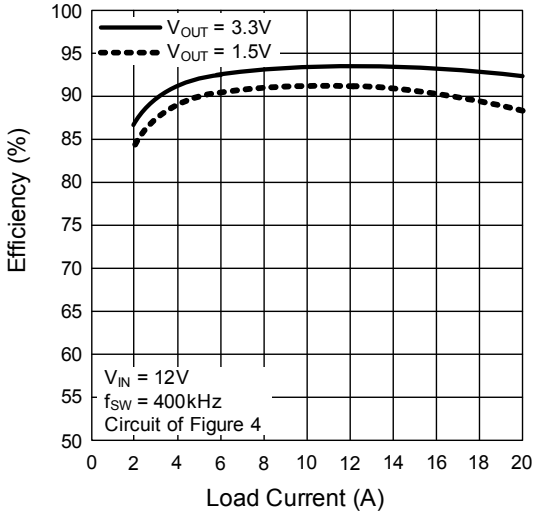


FIGURE 2. EFFICIENCY vs LOAD CURRENT

Table of Contents

Absolute Maximum Ratings

DC Supply Voltage for VDD Pin . . . . . -0.3V to 17V
MOSFET Drive Reference for VR Pin. . . . . -0.3V to 6.5V
2.5V Logic Reference for V25 Pin . . . . . -0.3V to 3V
Logic I/O Voltage for CFG(0, 1 ,2), DDC, EN, FC(0,1), ILIM, MGN, PG, PH_EN, SA(0, 1), SALRT, SCL, SDA, SS, SYNC, UVLO, V(0, 1) Pins . . . . . -0.3V to 6V
Analog Input Voltages for ISENB, VSEN, VTRK, XTEMP Pins . . . . . -0.3V to 6.5V
Analog Input Voltages for ISENA PIn . . . . . -1.5V to 6.5V
High Side Supply Voltage for BST Pin . . . . . -0.3V to 30V
Boost to Switch Voltage for BST -SW Pins . . . . . -0.3V to 8V
High Side Drive Voltage for GH Pin. . . . . (V_{SW}-0.3V) to (V_{BST}+0.3V)
Low Side Drive Voltage for GL Pin . . . . . (PGND-0.3V) to (VR+0.3V)
Switch Node Continuous for SW Pin . . . . . (PGND-0.3V) to 30V
Switch Node Transient (<100ns) for SW Pin. . . . . (PGND-5V) to 30V
Ground Differential for DGND – SGND, PGND - SGND Pins . . . . . -0.3V to 0.3V
ESD Rating
Human Body Model (Note 1, Tested per JESD22-A114E). 2kV
Machine Model (Tested per JESD22-A115-A). 500V
Latch Up (Tested per JESD78). 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
36 Ld QFN (Notes 2, 3)	35	5

Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Input Supply Voltage Range, V_{DD} (See Figure 9)
VDD tied to VR. . . . . 3.0V to 5.5V
VR floating. . . . . 4.5V to 14V
Output Voltage Range, V_{OUT} (Note 4) . . . . . 0.54V to 5.5V
Operating Junction Temperature Range, T_J. . . . . -40°C to +125°C
Input Voltage
V_{IN}, Rise Time . . . . . 5ms minimum
V_{IN} Ramp . . . . . Monotonic

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. BST, SW pins rated at 1.5kV.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
4. Includes margin limits.

Electrical Specifications

V_{DD} = 12V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
Input and Supply Characteristics					
I_{DD} Supply Current at f_{SW} = 200kHz	GH, GL no load	–	16	30	mA
I_{DD} Supply Current at f_{SW} = 1.4MHz	MISC_CONFIG[7] = 1	–	25	50	mA
I_{DDS} Shutdown Current	EN = 0V No I^2C/SMBus activity	–	6.5	9	mA
Vr Reference Output Voltage	V_{DD} > 6V, I_{VR} < 20mA	4.5	5.2	5.5	V
V25 Reference Output Voltage	V_R > 3V, I_{V25} < 20mA	2.25	2.5	2.75	V
Output Characteristics					
Output Voltage Adjustment Range (Note 5)	V_{IN} > V_{OUT}	0.6	–	5.0	V
Output Voltage Set-point Resolution	Set using resistors	–	10	–	mV
	Set using I^2C/SMBus	–	±0.025	–	% FS (Note 6)
Output Voltage Accuracy (Note 7)	Includes line, load, temp	-1	–	1	%
Vsen Input Bias Current	VSEN = 5.5V	–	110	200	µA
Current Sense Differential Input Voltage (Ground Referenced)	V_{ISENA} -V_{ISENB}	-100	–	100	mV
Current Sense Differential Input Voltage (V_{out} Referenced, V_{out} < 4.0V)	V_{ISENA} -V_{ISENB}	-50	–	50	mV
Current Sense Input Bias Current	Ground referenced	-100	–	100	µA

Electrical Specifications

V_{DD} = 12V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
Current Sense Input Bias Current (V_{out} Referenced, V_{out} < 4.0V)	ISENA	**-1**	–	**1**	µA
	ISENB	**-100**	–	**100**	µA
Soft-start Delay Duration Range (Note 8)	Set using SS pin or resistor	**2**	–	**30**	ms
	Set using I²C/SMBus	**0.002**	–	**500**	s
Soft-start Delay Duration Accuracy	Turn-on delay (precise mode) (Notes 8, 9, 10)	**-**	±0.25	**-**	ms
	Turn-on delay (normal mode) (Note 10)	**-**	-0.25/+4	**-**	ms
	Turn-off delay (Note 10)	**-**	-0.25/+4	**-**	ms
Soft-start Ramp Duration Range	Set using SS pin or resistor	**2**	–	**20**	ms
	Set using I²C	**0**	–	**200**	ms
Soft-start Ramp Duration Accuracy		**–**	100	**–**	µs
Logic Input/Output Characteristics					
Logic Input Leakage Current	EN, PG, SCL, SDA, SALRT pins	**-250**	–	**250**	nA
Logic Input Low, V_{IL}		**–**	–	**0.8**	V
Logic Input OPEN (N/C)	Multi-mode logic pins	**–**	1.4	**–**	V
Logic Input High, V_{IH}		**2.0**	–	**–**	V
Logic Output Low, V_{OL}	$I_{OL} \leq$ 4mA	**–**	–	**0.4**	V
Logic Output High, V_{OH}	$I_{OH} \geq$ -2mA	**2.25**	–	**–**	V
Oscillator and Switching Characteristics					
Switching Frequency Range		**200**	–	**1400**	kHz
Switching Frequency Set-point Accuracy	Predefined settings (See Table 11)	**-5**	–	**5**	%
Maximum Pwm Duty Cycle	Factory default	**95**	–	**–**	%
Minimum Sync Pulse Width		**150**	–	**–**	ns
Input Clock Frequency Drift Tolerance	External clock source	**-13**	–	**13**	%
Gate Drivers					
High-side driver voltage (V_{BST} -V_{SW})		**–**	4.5	**–**	V
High-side Driver Peak Gate Drive Current (Pull-down)	(V_{BST} -V_{SW}) = 4.5V	**2**	3	**–**	A
High-side Driver Pull-up Resistance	(V_{BST} -V_{SW}) = 4.5V, (V_{BST} -V_{GH}) = 50mV	**–**	0.8	**2**	Ω
High-side Driver Pull-down Resistance	(V_{BST} -V_{SW}) = 4.5V, (V_{GH} -V_{SW}) = 50mV	**–**	0.5	**2**	Ω
Low-side Driver Peak Gate Drive Current (Pull-up)	V_R = 5V	**–**	2.5	**–**	A
Low-side Driver Peak Gate Drive Current (Pull-down)	V_R = 5V	**–**	1.8	**–**	A
Low-side Driver Pull-up Resistance	V_R = 5V, (V_R -V_{GL}) = 50mV	**–**	1.2	**2**	Ω
Low-side Driver Pull-down Resistance	V_R = 5V, (V_{GL} -PGND) = 50mV	**–**	0.5	**2**	Ω
Switching Timing					
Gh Rise and Fall Time	(V_{BST} -V_{SW}) = 4.5V, C_{LOAD} = 2.2nF	**–**	5	**20**	ns
Gl Rise and Fall Time	V_R = 5V, C_{LOAD} = 2.2nF	**–**	5	**20**	ns
Tracking					
VTRK Input Bias Current	VTRK = 5.5V	**–**	110	**200**	µA
VTRK Tracking Ramp Accuracy	100% Tracking, V_{OUT} -VTRK	**-100**	–	**+ 100**	mV
VTRK Regulation Accuracy	100% Tracking, V_{OUT} -VTRK	**-1**	–	**1**	%

Electrical Specifications

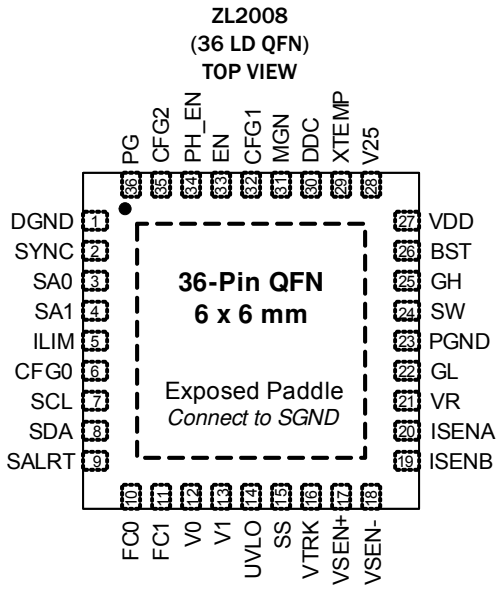
V_{DD} = 12V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
Fault Protection Characteristics					
UVLO Threshold Range	Configurable via I²C/SMBus	**2.85**	–	**16**	V
UVLO Set-point Accuracy		**-150**	–	**150**	mV
UVLO Hysteresis	Factory default	**–**	3	**–**	%
	Configurable via I²C/SMBus	**0**	–	**100**	%
UVLO Delay		**–**	–	**2.5**	µs
Power Good V_{OUT} Threshold	Factory default	**–**	90	**–**	% V_{OUT}
Power Good V_{OUT} Hysteresis	Factory default	**–**	5	**–**	%
Power Good Delay	Using pin-strap or resistor (Note 11)	**0**	–	**200**	ms
	Configurable via I²C/SMBus	**0**	–	**500**	s
VSEN Undervoltage Threshold	Factory default	**–**	85	**–**	% V_{OUT}
	Configurable via I²C/SMBus	**0**	–	**110**	% V_{OUT}
VSEN Overvoltage Threshold	Factory default	**–**	115	**–**	% V_{OUT}
	Configurable via I²C/SMBus	**0**	–	**115**	% V_{OUT}
VSEN Undervoltage Hysteresis		**–**	5	**–**	% V_{OUT}
VSEN Undervoltage/Overvoltage Fault Response Time	Factory default	**–**	16	**–**	µs
	Configurable via I²C/SMBus	**5**	–	**60**	µs
Current Limit Set-point Accuracy (V_{OUT} Referenced)		**–**	±10	**–**	% FS (Note 12)
Current Limit Set-point Accuracy (Ground Referenced)		**–**	±10	**–**	% FS (Note 12)
Current Limit Protection Delay	Factory default	**–**	5	**–**	t_{SW} (Note 13)
	Configurable via I²C/SMBus	**1**	–	**32**	t_{SW} (Note 13)
Temperature Compensation of Current Limit Protection Threshold	Factory default		4400		ppm/°C
	Configurable via I²C/SMBus	**100**		**12700**	
Thermal Protection Threshold (Junction Temperature)	Factory default	**–**	125	**–**	°C
	Configurable via I²C/SMBus	**-40**	–	**125**	°C
Thermal Protection Hysteresis		**–**	15	**–**	°C

NOTES:

5. Does not include margin limits.
6. Percentage of Full Scale (FS) with temperature compensation applied.
7. V_{OUT} measured at the termination of the VSEN+ and VSEN-sense points.
8. The device requires a delay period following an enable signal and prior to ramping its output. Precise timing mode limits this delay period to approx 2ms, where in normal mode it may vary up to 4ms. Current Share member minimum delay is 5ms. Current share reference must be 10ms greater than member delay.
9. Precise ramp timing mode is only valid when using EN pin to enable the device rather than PMBus enable.
10. The devices may require up to a 4ms delay following the assertion of the enable signal (normal mode) or following the de-assertion of the enable signal.
11. Factory default Power Good delay is set to the same value as the soft-start ramp time.
12. Percentage of Full Scale (FS) with temperature compensation applied
13. $t_{SW} = 1/f_{SW}$, where f_{SW} is the switching frequency.
14. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
15. Nominal capacitance of logic pins is 5pF.

Pin Configuration



Pin Descriptions

Pin	Label	Type (Note 16)	Description
1	DGND	PWR	Digital ground. Common return for digital signals. Connect to low impedance ground plane.
2	SYNC	I/O, M (Note 17)	Clock synchronization input. Used to set switching frequency of internal clock or for synchronization to external frequency reference.
3	SA0	I, M	Serial address select pins. Used to assign unique SMBus address to each IC or to enable certain management features.
4	SA1		
5	ILIM	I, M	Current limit select. Sets the overcurrent threshold voltage for ISENA and ISENB.
6	CFG0	I, M	Configuration pin. Used to setup current sharing and non-linear response.
7	SCL	I/O	Serial clock. Connect to external host and/or to other ZL devices.
8	SDA	I/O	Serial data. Connect to external host and/or to other ZL devices.
9	SALRT	O	Serial alert. Connect to external host if desired.
10	FC0	I	Loop compensation configuration pins.
11	FC1		
12	V0	I	Output voltage selection pins. Used to set V_{OUT} set-point and V_{OUT} max.
13	V1		
14	UVLO	I, M	Undervoltage lockout selection. Sets the minimum value for V_{DD} voltage to enable V_{OUT}.
15	SS	I, M	Soft-start pin. Sets the output voltage ramp time during turn-on and turn-off. Sets the delay from when EN is asserted until the output voltage starts to ramp.
16	VTRK	I	Tracking sense input. Used to track an external voltage source.
17	VSEN+	I	Output voltage feedback. Connect to output regulation point.
18	VSEN-	I	Output voltage feedback. Connect to load return or ground regulation point.
19	ISENB	I	Differential voltage input for current limit.
20	ISENA	I	Differential voltage input for current limit. High voltage tolerant.

Pin Descriptions (Continued)

Pin	Label	Type (Note 16)	Description
21	VR	PWR	Internal 5V reference used to power internal drivers.
22	GL	O	Low side FET gate drive.
23	PGND	PWR	Power ground. Connect to low impedance ground plane.
24	SW	PWR	Drive train switch node.
25	GH	O	High-side FET gate drive.
26	BST	PWR	High-side drive boost voltage.
27	VDD (Note 18)	PWR	Supply voltage.
28	V25	PWR	Internal 2.5V reference used to power internal circuitry.
29	XTEMP	I	External temperature sensor input. Connect to external 2N3904 diode connected transistor.
30	DDC	I/O	Digital-DC Bus. (Open Drain) Interoperability between Zilker Labs devices.
31	MGN	I	Signal that enables margining of output voltage.
32	CFG1	I, M	Configuration pin. Used to setup clock synchronization and sequencing.
33	EN	I	Enable input (active high). Pull-up to enable PWM switching and pull-down to disable PWM switching.
34	PH_EN	I	Phase enable input (active high). Pull-up to enable phase and pull-down to disable phase for current sharing.
35	CFG2	I, M	Configuration pin. Sets the phase offset (single-phase) or current sharing group position (multi-phase).
36	PG	O	Power good output.
ePad	SGND	PWR	Exposed thermal pad. Common return for analog signals; internal connection to SGND. Connect to low impedance ground plane.

NOTES:

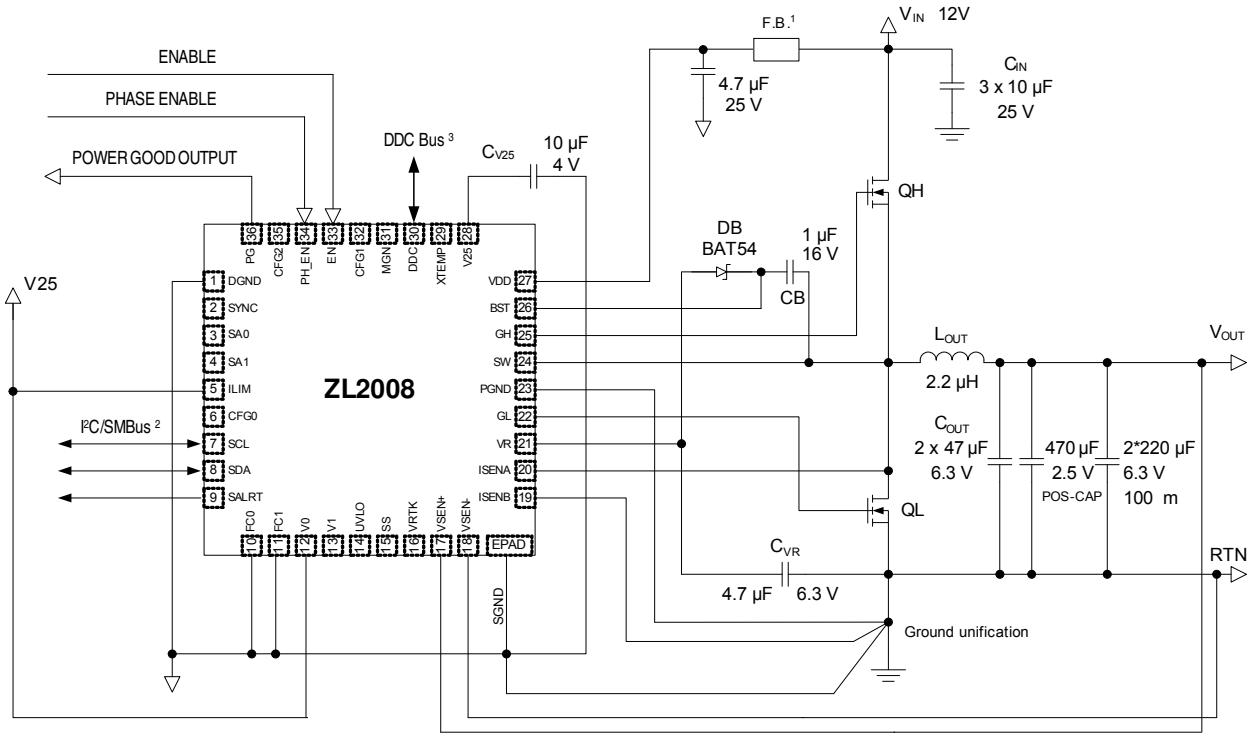
16. I = Input, O = Output, PWR = Power or Ground. M = Multi-mode pins. Please refer to “Multi-mode Pins” on page 12.

17. The SYNC pin can be used as a logic pin, a clock input or a clock output.

18. V_{DD} is measured internally and the value is used to modify the PWM loop gain.

Typical Application Circuit

The following application circuit represents a typical implementation of the ZL2008. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.



Notes:
1. Ferrite bead is optional for input noise suppression
2. The I²C/SMBus requires pull-up resistors. Please refer to the I²C/SMBus specifications for more details.
3. The DDC bus requires a pull-up resistor. The resistance will vary based on the capacitive loading of the bus(and on the number of devices connected). The 10 kΩ default value, assuming a maximum of 100 pF per device, provides the necessary 1 µs pull-up rise time. Please refer to the DDC Bus section for more details

FIGURE 3. 12V to 1.8V/16A Application Circuit

ZL2008 Overview

Digital-DC Architecture

The ZL2008 is an innovative mixed-signal power conversion and power management IC based on Zilker Labs patented Digital-DC technology that provides an integrated, high performance step-down converter for a wide variety of power supply applications.

Today's embedded power systems are typically designed for optimal efficiency at maximum load, reducing the peak thermal stress by limiting the total thermal dissipation inside the system. Unfortunately, many of these systems are often operated at load levels far below the peak where the power system has been optimized, resulting in reduced efficiency. While this may not cause thermal stress to occur, it does contribute to higher electricity usage and results in higher overall system operating costs.

Zilker Labs' efficiency-adaptive ZL2008 DC/DC controller helps mitigate this scenario by enabling the power converter to automatically change their operating state to increase efficiency and overall performance with little or no user interaction needed. Its unique PWM loop utilizes an ideal mix of analog and digital blocks to enable precise control of the entire power conversion process with no software required, resulting in a very flexible device that is also very easy to use. An extensive set of power management functions are fully integrated and can be configured using simple pin connections. The user configuration can be saved in an internal non-volatile memory (NVM). Additionally, all functions can be configured and monitored via the SMBus hardware interface using standard PMBus commands, allowing ultimate flexibility.

Once enabled, the ZL2008 is immediately ready to regulate power and perform power management tasks with no programming required. Advanced configuration options and real-time configuration changes are available via the I^2C/SMBus interface if desired and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated sub-regulation circuitry enables single supply operation from any supply between 3V and 14V with no secondary bias supplies needed.

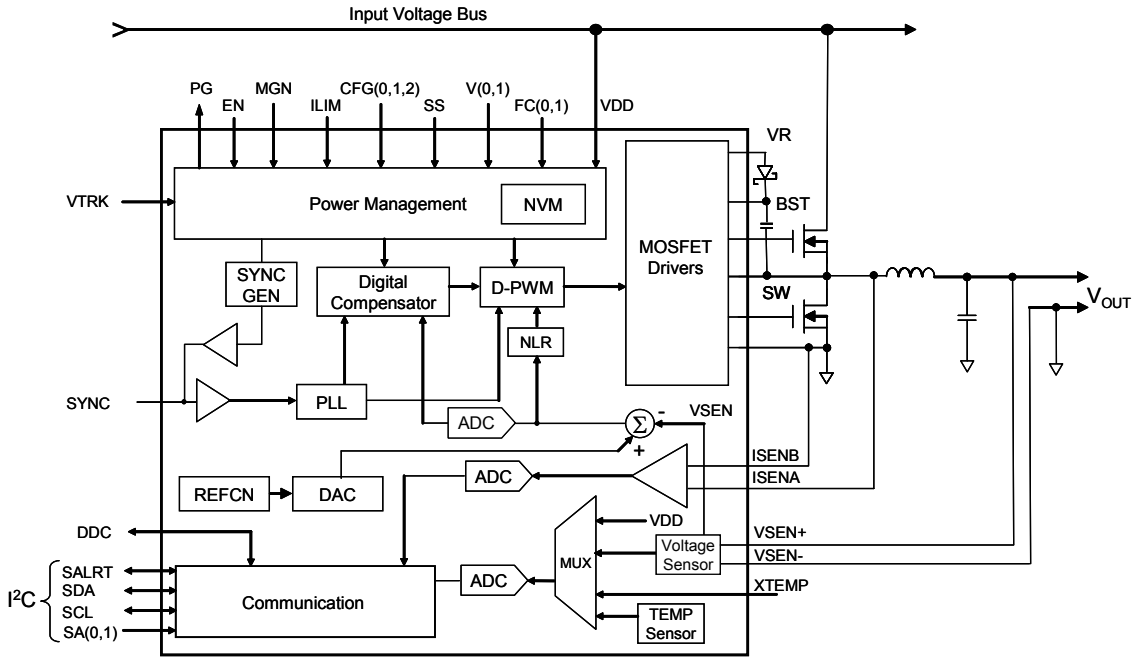


FIGURE 4. ZL2008 Block Diagram

Power Conversion Overview

The ZL2008 operates as a voltage-mode, synchronous buck converter with a selectable constant frequency pulse width modulator (PWM) control scheme that uses external MOSFETs, capacitors, and an inductor to perform power conversion.

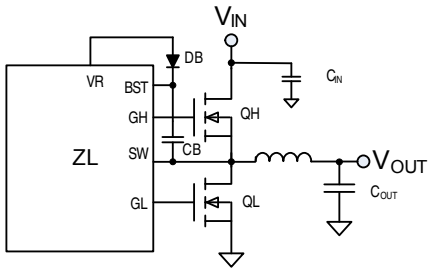


FIGURE 5. Synchronous Buck Converter

Figure 5 illustrates the basic synchronous buck converter topology showing the primary power train components. This converter is also called a step-down converter, as the output voltage must always be lower than the input voltage. In its most simple configuration, the ZL2008 requires two external N-channel power MOSFETs, one for the top control MOSFET (QH) and one for the bottom synchronous MOSFET (QL). The amount of time that QH is on as a fraction of the total switching period is known as the duty cycle *D*, which is described by Equation 1:

$$D \approx \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 1)}$$

During time D, QH is on and $V_{IN} - V_{OUT}$ is applied across the inductor. The current ramps up as shown in Figure 6.

When QH turns off (time 1-D), the current flowing in the inductor must continue to flow from the ground up through QL, during which the current ramps down. Since the output capacitor C_{OUT} exhibits a low impedance at the switching frequency, the AC component of the inductor current is filtered from the output voltage so the load sees nearly a DC voltage.

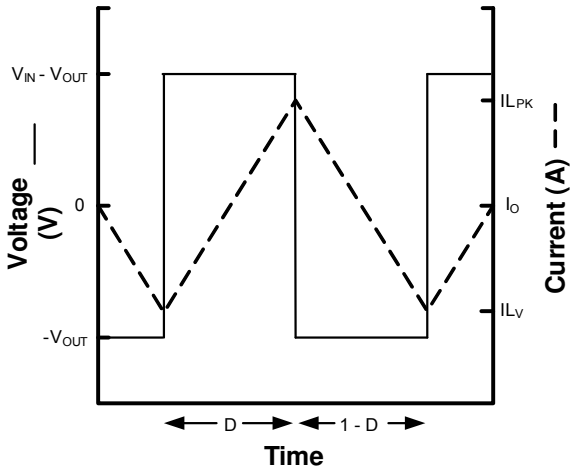


FIGURE 6. Inductor Waveform

Typically, buck converters specify a maximum duty cycle that effectively limits the maximum output voltage that can be realized for a given input voltage. This duty cycle limit ensures that the lowside MOSFET is allowed to turn on for a minimum amount of time during each switching cycle, which enables the bootstrap capacitor (CB in Figure 5) to be charged up and provide adequate gate drive voltage for the high-side MOSFET. See section“High-side Driver Boost Circuit” on page 12 for more details.

In general, the size of components L1 and C_{OUT} as well as the overall efficiency of the circuit are inversely proportional to the switching frequency, f_{SW}. Therefore, the highest efficiency circuit may be realized by switching the MOSFETs at the lowest possible frequency; however, this will result in the largest component size. Conversely, the smallest possible footprint may be realized by switching at the fastest possible frequency but this gives a somewhat lower efficiency. Each user should determine the optimal combination of size and efficiency when determining the switching frequency for each application.

The block diagram for the ZL2008 is illustrated in Figure 4. In this circuit, the target output voltage is regulated by connecting the differential VSEN pins directly to the output regulation point. The VSEN signal is then compared to a reference voltage that has been set to the desired output voltage level by the user. The error signal derived from this comparison is converted to a digital value with a low-resolution, analog to digital (A/D) converter. The digital signal is applied to an adjustable digital compensation filter, and the compensated signal is used to derive the appropriate PWM duty cycle for driving the external MOSFETs in a way that produces the desired output.

The ZL2008 has several features to improve the power conversion efficiency. A non-linear response (NLR) loop improves the response time and reduces the output deviation as a result of a load transient. The ZL2008 monitors the power converter’s operating conditions and continuously adjusts the turn-on and turn-off timing of the high-side and low-side MOSFETs to optimize the overall efficiency of the power supply. Adaptive performance optimization algorithms such as dead-time control, diode emulation, and frequency control are available to provide greater efficiency improvement.

Power Management Overview

The ZL2008 incorporates a wide range of configurable power management features that are simple to implement with no external components. Additionally, the ZL2008 includes circuit protection features that continuously safeguard the device and load from damage due to unexpected system faults. The ZL2008 can continuously monitor input voltage, output voltage/current, internal temperature, and the temperature of an external thermal diode. A Power Good output signal is also included to enable power-on reset functionality for an external processor.

All power management functions can be configured using either pin configuration techniques (see Figure 7) or via the I^2C/SMBus interface. Monitoring parameters can also be pre-configured to provide alerts for specific conditions. See Application Note AN2033 for more details on SMBus monitoring.

Multi-mode Pins

In order to simplify circuit design, the ZL2008 incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device with no programming. Most power management features can be configured using these pins. The multi-mode pins can respond to four different connections as shown in Table 1. These pins are sampled when power is applied or by issuing a PMBus Restore command (See Application Note AN2033).

Pin-strap Settings: This is the simplest implementation method, as no external components are required. Using this method, each pin can take on one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to the V25 pin for logic HIGH settings as this pin provides a regulated voltage higher than 2V. Using a single pin, one of three settings can be selected. Using two pins, one of nine settings can be selected.

TABLE 1. Multi-mode Pin Configuration

Pin Tied To	Value
LOW (Logic LOW)	< 0.8VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	> 2.0VDC
Resistor to SGND	Set by resistor value

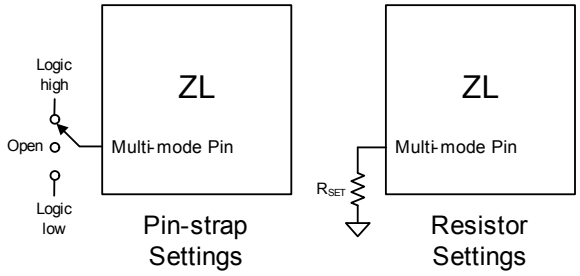


FIGURE 7. Pin-strap and Resistor Setting Examples

Resistor Settings: This method allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multi-mode pin and SGND. Standard 1% resistor values are used, and only every fourth E96 resistor value is used so the device can reliably recognize the value of resistance connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

I²C/SMBus Method: Almost any ZL2008 function can be configured via the I²C/SMBus interface using standard PMBus commands. Additionally, any value that has been configured using the pin-strap or resistor setting methods can also be re-configured and/or verified via the I²C/SMBus. See Application Note AN2033 for more details.

The SMBus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set via the I²C/SMBus. The device address is set using the SA0 and SA1 pins. VOUT_MAX is determined as 10% greater than the voltage set by the V0 and V1 pins.

Power Conversion Functional Description

Internal Bias Regulators and Input Supply Connections

The ZL2008 employs two internal low dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

VR: The VR LDO provides a regulated 5V bias supply for the MOSFET driver circuits. It is powered from the VDD pin. A 4.7µF filter capacitor is required at the VR pin.

V25: The V25 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from an internal 5V node. A 10µF filter capacitor is required at the V25 pin.

When the input supply (VDD) is higher than 5.5V, the VR pin should not be connected to any other pins. It should only have a filter capacitor attached as shown in Figure 8. Due to the dropout voltage associated with the VR bias regulator, the VDD pin must be connected to the VR pin for designs operating from a supply below 5.5V. Figure 8 illustrates the required connections for both cases.

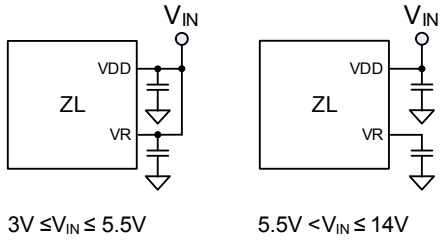


FIGURE 8. Input Supply Connections

Note: the internal bias regulators are not designed to be outputs for powering other circuitry. Do not attach external loads to any of these pins. The multi-mode pins may be connected to the V25 pin for logic HIGH settings.

High-side Driver Boost Circuit

The gate drive voltage for the high-side MOSFET driver is generated by a floating bootstrap capacitor, CB (see Figure 5). When the lower MOSFET (QL) is turned on, the SW node is pulled to ground and the capacitor is charged from the internal VR bias regulator through diode DB. When QL turns off and the upper MOSFET (QH) turns on, the SW node is pulled up to V_{DD} and the voltage on the bootstrap capacitor is boosted approximately 5V above V_{DD} to provide the necessary voltage to power the high-side driver. A Schottky diode should be used for DB to help maximize the high-side drive supply voltage.

Output Voltage Selection

STANDARD MODE

The output voltage may be set to any voltage between 0.6V and 5.0V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification. Using the pin-strap method, V_{OUT} can be set to any of nine standard voltages as shown in Table 2.

TABLE 2. Output Voltage Pin-strap Settings

		V0		
		LOW (V)	OPEN (V)	HIGH (V)
V1	LOW	0.6	0.8	1.0
	OPEN	1.2	1.5	1.8
	HIGH	2.5	3.3	5.0

The resistor setting method can be used to set the output voltage to levels not available in Table 2. Resistors R0 and R1 are selected to produce a specific voltage between 0.6V and 5.0V in 10mV steps. Resistor R1 provides a coarse setting and resistor R0 provides a fine adjustment, thus eliminating the additional errors associated with using two 1% resistors (this typically adds approx 1.4% error).

To set V_{OUT} using resistors, follow the steps below to calculate an index value and then use Table 3 to select the resistor that corresponds to the calculated index value as follows:

1. Calculate Index1:
   Index1 = 4 x V_{OUT} (V_{OUT} in 10mV steps)
2. Round the result down to the nearest whole number.
3. Select the value of R1 from Table 3 using the Index1 rounded value from step 2.
4. Calculate Index0:
5. Index0 = 100 x V_{OUT} – (25 x Index1)
6. Select the value of R0 from Table 3 using the Index0 value from Step 4.

TABLE 3. Output Voltage Resistors Settings

Index	R0 or R1 (kΩ)
0	10
1	11
2	12.1
3	13.3
4	14.7
5	16.2
6	17.8
7	19.6
8	21.5
9	23.7
10	26.1
11	28.7
12	31.6
13	34.8
14	38.3
15	42.2
16	46.4
17	51.1
18	56.2
19	61.9
20	68.1
21	75
22	82.5
23	90.9
24	100

Example from Figure 9: For V_{OUT} = 1.33V,

Index1 = 4 x 1.33V = 5.32;

From Table 3, R1 = 16.2kΩ

Index0 = (100 x 1.33V) – (25 x 5) = 8;

From Table 3, R0 = 21.5kΩ

SMBUS MODE

The output voltage may be set to any value between 0.6V and 5.0V using a PMBus command over the I^2C/SMBus interface. See Application Note AN2033 for details.

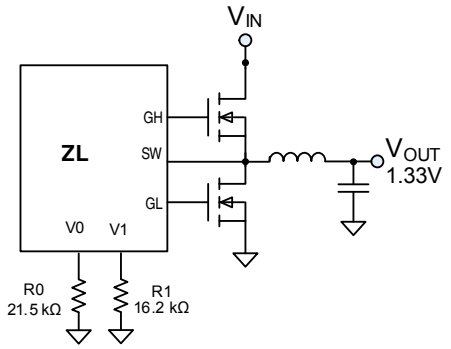


FIGURE 9. Output Voltage Resistor Setting Example

POLA VOLTAGE TRIM MODE

The output voltage mapping can be changed to match the voltage setting equations for POLA and DOSA standard modules.

The standard method for adjusting the output voltage for a POLA module is defined by Equation 2:

$$R_{SET} = 10k\Omega \times \frac{0.69V}{V_{OUT} - 0.69V} - 1.43k\Omega \quad \text{(EQ. 2)}$$

The resistor, R_{SET}, is external to the POLA module. See Figure 10.

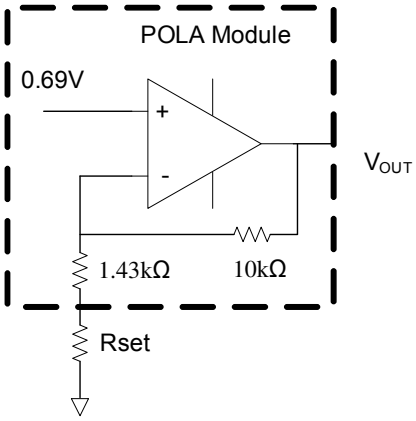


FIGURE 10. Output Voltage Setting on POLA Module

To stay compatible with this existing method for adjusting the output voltage and to keep the same external R_{SET} resistor when using the ZL2008, the module manufacturer should add a 10kΩ resistor on the module as shown in Figure 11. Now, the same R_{SET} used for an analog POLA module will provide the same output voltage when using a digital POLA module based on the ZL2008.

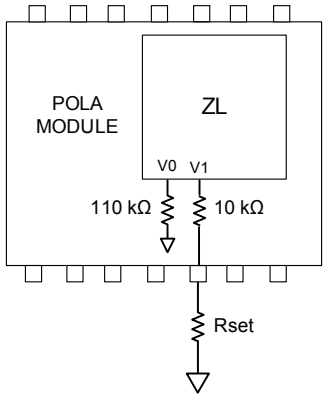


FIGURE 11. R_{SET} on a POLA Module

The POLA mode is activated through pin-strap by connecting a 110kΩ resistor on V0 to SGND. The V1 pin is then used to adjust the output voltage as shown in Table 4.

The POLA mode can also be activated through PMBus commands. See Application Note AN2033 for more details.

TABLE 4. POLA Mode V_{OUT} Settings

V_{OUT} (V)	R_{SET} (kΩ) In series with 10kΩ resistor
0.700	162
0.752	110
0.758	100
0.765	90.9
0.772	82.5
0.790	75.0
0.800	56.2
0.821	51.1
0.834	46.4
0.848	42.2
0.880	34.8
0.899	31.6
0.919	28.7
0.965	23.7
0.991	21.5
1.000	19.6
1.100	16.2
1.158	13.3
1.200	12.1
1.250	9.09
1.500	7.50
1.669	5.62
1.800	4.64
2.295	2.87
2.506	2.37
3.300	1.21
5.000	0.162

NOTE: (R0 = 110kΩ, R1 = R_{SET} + 10kΩ)

DOSA VOLTAGE TRIM MODE

On a DOSA module, the V_{OUT} setting follows Equation 3:

$$R_{SET} = \frac{6900}{V_{OUT} - 0.69V} \quad \text{(EQ. 3)}$$

To maintain DOSA compatibility, the same scheme is used as with a POLA module except the 10kΩ resistor is replaced with a 8.66kΩ resistor as shown in Figure 12.

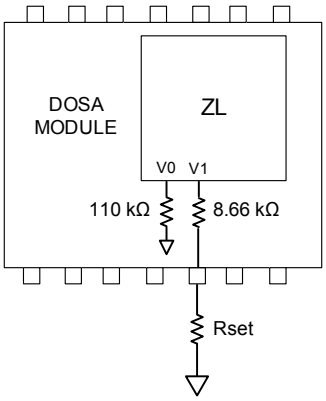


FIGURE 12. R_{SET} on a DOSA Module

The DOSA mode V_{OUT} settings are listed in Table 5.

TABLE 5. DOSA Mode V_{OUT} Settings

V_{OUT} (V)	R_{SET} (kΩ) In series with 8.660kΩ resistor
0.700	162
0.752	113
0.758	100
0.765	90.9
0.772	82.5
0.790	75.0
0.800	57.6
0.821	52.3
0.834	47.5
0.848	43.2
0.880	36.5
0.899	33.2
0.919	30.1
0.965	25.5
0.991	22.6
1.000	21.0
1.100	17.8
1.158	14.7
1.200	13.3
1.250	10.5
1.500	8.87
1.669	6.98
1.800	6.04
2.295	4.32
2.506	3.74
3.300	2.61
5.000	1.50

NOTE: (R0 = 110kΩ, R1 = R_{SET} + 8.66kΩ)

Start-up Procedure

The ZL2008 follows a specific internal start-up procedure after power is applied to the VDD pin. Table 6 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. The device requires approximately 5ms to 10ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the I^2C/SMBus interface and the device is ready to be enabled. Once enabled, the device requires approximately 2ms before its output voltage may be allowed to start its ramp-up process. If a soft-start delay period less than 2ms has been configured (using PMBus commands), the device will default to a 2ms delay period. If a delay period greater than 2ms is configured, the device will wait for the configured delay period prior to starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the pre-configured soft-start ramp time that has been set using the SS pin. It should be noted that if the EN pin is tied to VDD, the device will still require approx 5ms to 10ms before the output can begin its ramp-up as described in Table 6.

Soft-start Delay and Ramp Times

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ZL2008 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires. The soft-start delay period is set using the SS pin. Precise ramp delay timing reduces the delay time variations but is only available when the appropriate bit in the MISC_CONFIG register has been set. Please refer to Application Note AN2033 for details.

The soft-start ramp timer enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the delay period has expired. The ramp-up is guaranteed monotonic and its slope may be precisely set using the SS pin.

The soft-start delay and ramp times can be set to standard values according to Table 7.

TABLE 6. ZL2106 START-UP SEQUENCE

STEP #	STEP NAME	DESCRIPTION	TIME DURATION
1	Power Applied	Input voltage is applied to the ZL2008's VDD pin	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approx 5ms to 10ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by the multi-mode pins.	
4	Device Ready	The device is ready to accept an enable signal.	-
5	Pre-ramp Delay	The device requires approximately 2ms following an enable signal and prior to ramping its output. Additional pre-ramp delay may be configured using the SS pin.	Approximately 2ms

TABLE 7. Soft-start Pin-strap Settings

SS Pin	Delay Time (ms)	Ramp Time (ms)
LOW	2	2
OPEN	5	5
HIGH	10	10

If the desired soft-start delay and ramp times are not one of the values listed in Table 7, the times can be set to a custom value by connecting a resistor from the SS pin to SGND using the appropriate resistor value from Table 8. The value of this resistor is measured upon start-up or Restore and will not change if the resistor is varied after power has been applied to the ZL2008. See Figure 13 for typical connections using resistors.

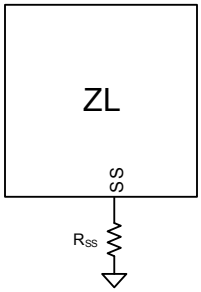


FIGURE 13. SS Pin Resistor Connections

The soft-start delay and ramp times can also be set to custom values via the I²C/SMBus interface. When the SS delay time is set to 0ms, the device will begin its ramp-up after the internal circuitry has initialized (approx. 2ms). When the soft-start ramp period is set to 0ms, the output will ramp up as quickly as the output load capacitance and loop settings will allow. It is generally recommended to set the soft-start ramp to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current.

Power Good

The ZL2008 provides a Power Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within
-10% of the target voltage. These limits and the polarity of the pin may be changed via the I²C/SMBus interface. See Application Note AN2033 for details.

A PG delay period is defined as the time from when all conditions within the ZL2008 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL2008 PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 10ms, the PG delay will be set to 10ms. The PG delay may be set independently of the soft-start ramp using the I²C/SMBus as described in Application Note AN2033.

TABLE 8. SS Resistor Settings

R_{SS} (kΩ)	Delay Time (ms)	Ramp Time (ms)
10	2	5
11		10
12.1		20
13.3	5	2
14.7		5
16.2		10
17.8		20
19.6	10	2
21.5		5
23.7		10
26.1		20
28.7	15	2
31.6		5
34.8		10
38.3		20
42.2	20	2
46.4		5
51.1		10
56.2		20
61.9	30	2
68.1		5
75		10
82.5		20

Switching Frequency and PLL

The ZL2008 incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Zilker Labs devices.

The SYNC pin is a unique pin that can perform multiple functions depending on how it is configured. The CFG1 pin is used to select the operating mode of the SYNC pin as shown in Table 9. Figure 14 illustrates the typical connections for each mode.

TABLE 9. SYNC Pin Function Selection

CFG1 Pin	SYNC Pin Function
LOW	SYNC is configured as an input
OPEN	Auto Detect mode
HIGH	SYNC is configured as an output f_{SW} = 400kHz

Configuration A: SYNC OUTPUT

When the SYNC pin is configured as an output (CFG1 pin is tied HIGH), the device will run from its internal oscillator and will drive the resulting internal oscillator signal (preset to 400kHz) onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode.

Configuration B: SYNC INPUT

When the SYNC pin is configured as an input (CFG1 pin is tied LOW), the device will automatically check for a clock signal on the SYNC pin each time EN is asserted. The ZL2008's oscillator will then synchronize with the rising edge of the external clock.

The incoming clock signal must be in the range of 200kHz to 1.4MHz and must be stable when the enable pin is asserted. The clock signal must also exhibit the necessary performance requirements (see "Electrical Specifications" on page 4). In the event of a loss of the external clock signal, the output voltage may show transient over/undershoot.

If this happens, the ZL2008 will automatically switch to its internal oscillator and switch at a frequency close to the previous incoming frequency.

Configuration C: SYNC AUTO DETECT

When the SYNC pin is configured in auto detect mode (CFG1 pin is left OPEN), the device will automatically check for a clock signal on the SYNC pin after enable is asserted.

If a clock signal is present, The ZL2008's oscillator will then synchronize the rising edge of the external clock. Refer to SYNC INPUT description.

If no incoming clock signal is present, the ZL2008 will configure the switching frequency according to the state of the SYNC pin as listed in Table 10. In this mode, the ZL2008 will only read the SYNC pin connection during the start-up sequence. Changes to SYNC pin connections will not affect f_{SW} until the power (VDD) is cycled off and on.

TABLE 10. Switching Frequency Pin-strap Setting

SYNC Pin	Frequency
LOW	200kHz
OPEN	400kHz
HIGH	1MHz
Resistor	See Table 11

If the user wishes to run the ZL2008 at a frequency not listed in Table 10, the switching frequency can be set using an external resistor, R_{SYNC}, connected between SYNC and SGND using Table 11.

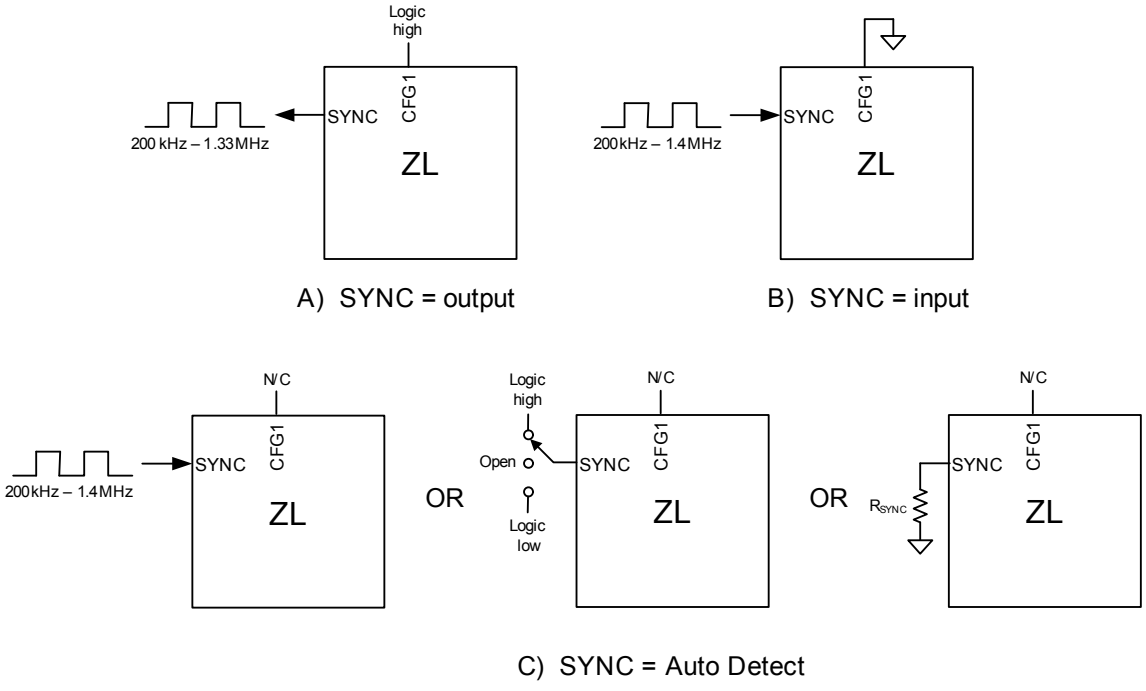


FIGURE 14. Sync Pin Configurations

TABLE 11. Switching Frequency Resistor Settings

R_{SYNC} (kΩ)	f_{SW} (kHz)
10	200
11	222
12.1	242
13.3	267
14.7	296
16.2	320
17.8	364
19.6	400
21.5	421
23.7	471
26.1	533
28.7	571
31.6	615
34.8	727
38.3	800
46.4	889
51.1	1000
56.2	1143
68.1	1333

The switching frequency can also be set to any value between 200kHz and 1.33MHz using the I^2C/SMBus interface. The available frequencies below 1.4MHz are defined by f_{SW} = 8MHz/N, where the whole number N is $6 \leq N \leq 40$. See Application Note AN2033 for details.

If a value other than f_{SW} = 8MHz/N is entered using a PMBus command, the internal circuitry will select the valid switching frequency value that is closest to the entered value. For example, if 810kHz is entered, the device will select 800kHz (N=10).

When multiple Zilker Labs devices are used together, connecting the SYNC pins together will force all devices to synchronize with each other. The CFG1 pin of one device must set its SYNC pin as an output and the remaining devices must have their SYNC pins set as Auto Detect.

Note: The switching frequency read back using the appropriate PMBus command will differ slightly from the selected values in Table 11. The difference is due to hardware quantization.

Power Train Component Selection

The ZL2008 is a synchronous buck converter that uses external MOSFETs, inductor and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance.

To select the appropriate external components for the desired performance goals, the power supply requirements listed in Table 12 must be known.

TABLE 12. Power Supply Requirements

Parameter	Range	Example Value
Input voltage (V_{IN})	3.0V to 14.0V	12V
Output voltage (V_{OUT})	0.6V to 5.0V	1.2V
Output current (I_{OUT})	0A to ~25A	20A
Output voltage ripple (V_{orip})	< 3% of V_{OUT}	1% of V_{OUT}
Output load step (I_{ostep})	< Io	50% of I_o
Output load step rate	—	10A/µs
Output deviation due to load step	—	± 50mV
Maximum PCB temp.	+120°C	+85°C
Desired efficiency	—	85%
Other considerations	Various	Optimize for small size

DESIGN GOAL TRADE-OFFS

The design of the buck power stage requires several compromises among size, efficiency, and cost. The inductor core loss increases with frequency, so there is a trade-off between a small output filter made possible by a higher switching frequency and getting better power supply efficiency. Size can be decreased by increasing the switching frequency at the expense of efficiency. Cost can be minimized by using through-hole inductors and capacitors; however these components are physically large.

To start the design, select a switching frequency based on Table 13. This frequency is a starting point and may be adjusted as the design progresses.

TABLE 13. Circuit Design Consideration

Frequency Range	Efficiency	Circuit Size
200kHz to 400kHz	Highest	Larger
400kHz to 800kHz	Moderate	Smaller
800kHz to 1.4MHz	Lower	Smallest

INDUCTOR SELECTION

The output inductor selection process must include several trade-offs. A high inductance value will result in a low ripple current (I_{opp}), which will reduce output capacitance and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be struck between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple equal to the expected load transient step magnitude (I_{ostep}):

$$I_{opp} = I_{ostep} \quad \text{(EQ. 4)}$$

Now the output inductance can be calculated using Equation 5, where V_{INM} is the maximum input voltage:

$$L_{OUT} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INM}}\right)}{fsw \times I_{opp}} \quad \text{(EQ. 5)}$$

The average inductor current is equal to the maximum output current. The peak inductor current (I_{Lpk}) is calculated using Equation 6 where I_{OUT} is the maximum output current:

$$I_{Lpk} = I_{OUT} + \frac{I_{opp}}{2} \quad \text{(EQ. 6)}$$

Select an inductor rated for the average DC current with a peak current rating above the peak current computed above.

In overcurrent or short-circuit conditions, the inductor may have currents greater than 2X the normal maximum rated output current. It is desirable to use an inductor that still provides some inductance to protect the load and the MOSFETs from damaging currents in this situation.

Once an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's datasheet.

$$P_{LDCR} = DCR \times I_{Lrms}^{\ 2} \quad \text{(EQ. 7)}$$

I_{Lrms} is given by Equation 8:

$$I_{Lrms} = \sqrt{I_{OUT}^{\ 2} + \frac{(I_{opp})^2}{12}} \quad \text{(EQ. 8)}$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor datasheet. Add the core loss and the ESR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

OUTPUT CAPACITOR SELECTION

Several trade-offs must also be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output ripple voltage to the capacitor ESR and the other half to capacitance, as shown in Equations 9 and 10:

$$C_{OUT} = \frac{I_{opp}}{8 \times f_{sw} \times \frac{V_{orip}}{2}} \quad \text{(EQ. 9)}$$

$$ESR = \frac{V_{orip}}{2 \times I_{opp}} \quad \text{(EQ. 10)}$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using Equation 11:

$$V_{orip} = I_{opp} \times ESR + \frac{I_{opp}}{8 \times f_{sw} \times C_{OUT}} \quad \text{(EQ. 11)}$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

INPUT CAPACITOR

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5V or 12V "bulk" supply from an off-line power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple (I_{CINrms}) can be determined from Equation 12:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad \text{(EQ. 12)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2X the ripple current calculated above to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage are recommended.

BOOTSTRAP CAPACITOR SELECTION

The high-side driver boost circuit utilizes an external Schottky diode (D_B) and an external bootstrap capacitor (C_B) to supply sufficient gate drive for the high-side MOSFET driver. D_B should be a 20mA, 30V Schottky diode or equivalent device and C_B should be a 1µF ceramic type rated for at least 6.3V.

QL SELECTION

The bottom MOSFET should be selected primarily based on the device's $R_{DS(ON)}$ and secondarily based on its gate charge. To choose QL, use the following equation and allow 2% to 5% of the output power to be dissipated in the $R_{DS(ON)}$ of QL (lower output voltages and higher step-down ratios will be closer to 5%):

Calculate the RMS current in QL as follows:

$$P_{QL} = 0.05 \times V_{OUT} \times I_{OUT} \quad \text{(EQ. 13)}$$

$$I_{botrms} = I_{Lrms} \times \sqrt{1-D} \quad \text{(EQ. 14)}$$

Calculate the desired maximum $R_{DS(ON)}$ as follows:

$$R_{DS(ON)} = \frac{P_{QL}}{\left(I_{botrms}\right)^2} \quad \text{(EQ. 15)}$$

Note that the $R_{DS(ON)}$ given in the manufacturer's datasheet is measured at +25°C. The actual $R_{DS(ON)}$ in the end-use application will be much higher. For example, a Vishay Si7114 MOSFET with a junction temperature of +125°C has an $R_{DS(ON)}$ that is 1.4 times higher than the value at +25°C. Select a candidate MOSFET, and calculate the required gate drive current as follows:

$$I_g = f_{SW} \times Q_g \quad \text{(EQ. 16)}$$

Keep in mind that the total allowed gate drive current for both QH and QL is 80mA.

MOSFETs with lower $R_{DS(ON)}$ tend to have higher gate charge requirements, which increases the current and resulting power required to turn them on and off. Since the MOSFET gate drive circuits are integrated in the ZL2008, this power is dissipated in the ZL2008 according to Equation 17:

$$P_{QL} = f_{sw} \times Q_g \times V_{INM} \quad \text{(EQ. 17)}$$

QH SELECTION

In addition to the $R_{DS(ON)}$ loss and gate charge loss, QH also has switching loss. The procedure to select QH is similar to the procedure for QL. First, assign 2% to 5% of the output power to be dissipated in the $R_{DS(ON)}$ of QH using the equation for QL above. As was done with QL, calculate the RMS current as follows:

$$I_{toprms} = I_{Lrms} \times \sqrt{D} \quad \text{(EQ. 18)}$$

Calculate a starting $R_{DS(ON)}$ as follows, in this example using 5%:

$$P_{QH} = 0.05 \times V_{OUT} \times I_{OUT} \quad \text{(EQ. 19)}$$

$$R_{DS(ON)} = \frac{P_{QH}}{\left(I_{toprms}\right)^2} \quad \text{(EQ. 20)}$$

Select a MOSFET and calculate the resulting gate drive current. Verify that the combined gate drive current from QL and QH does not exceed 80mA.

Next, calculate the switching time using:

$$t_{SW} = \frac{Q_g}{I_{gdr}} \quad \text{(EQ. 21)}$$

where Q_g is the gate charge of the selected QH and I_{gdr} is the peak gate drive current available from the ZL2008.

Although the ZL2008 has a typical gate drive current of 3A, use the minimum guaranteed current of 2A for a conservative design. Using the calculated switching time, calculate the switching power loss in QH using:

$$P_{swtop} = V_{INM} \times t_{sw} \times I_{OUT} \times f_{sw} \quad \text{(EQ. 22)}$$

The total power dissipated by QH is given by Equation 23:

$$P_{QHtot} = P_{QH} + P_{swtop} \quad \text{(EQ. 23)}$$

MOSFET THERMAL CHECK

Once the power dissipations for QH and QL have been calculated, the MOSFETs junction temperature can be estimated. Using the junction-to-case thermal resistance (R_{th}) given in the MOSFET manufacturer's datasheet and the expected maximum printed circuit board temperature, calculate the junction temperature as follows:

$$T_{j\max} = T_{pcb} + \left(P_Q \times R_{th}\right) \quad \text{(EQ. 24)}$$

CURRENT SENSING COMPONENTS

Once the current sense method has been selected (refer to section "Current Limit Threshold Selection" on page 21), the components are selected as follows.

When using the inductor DCR sensing method, the user must also select an R/C network comprised of R1 and CL (see Figure 15).

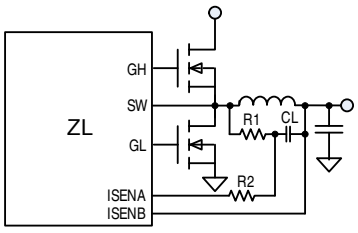


FIGURE 15. DCR Current Sensing

For the voltage across C_L to reflect the voltage across the DCR of the inductor, the time constant of the inductor must match the time constant of the RC network. That is:

$$\tau_{RC} = \tau_{L/DCR}$$
$$R_1 \cdot C_L = \frac{L}{DCR} \quad \text{(EQ. 25)}$$

For *L*, use the average of the nominal value and the minimum value. Include the effects of tolerance, DC Bias and switching frequency on the inductance when determining the minimum value of *L*. Use the typical value for *DCR*.

The value of R_1 should be as small as feasible and no greater than 5kΩ for best signal-to-noise ratio. The designer should make sure the resistor package size is appropriate for the power dissipated and include this loss in efficiency calculations. In calculating the minimum value of R_1, the average voltage across

C_L (which is the average $I_{OUT}DCR$ product) is small and can be neglected. Therefore, the minimum value of R_1 may be approximated Equation 26:,

$$R_{1-\min} = \frac{D\left(V_{IN-\max} - V_{OUT}\right)^2 + \left(1-D\right)\cdot V_{OUT}{}^2}{P_{R1\,pkg-\max}\cdot \delta_P} \quad \text{(EQ. 26)}$$

where P_{R1pkg}-max is the maximum power dissipation specification for the resistor package and $_P$ is the derating factor for the same parameter (eg.: P_{R1pkg}-max = 0.0625W for 0603 package, $_P$ = 50% @ 85°C). Once R_1-min has been calculated, solve for the maximum value of C_L from Equation 27:

$$C_{L-\max} = \frac{L}{R_{1-\min}\cdot DCR} \quad \text{(EQ. 27)}$$

and choose the next-lowest readily available value (e.g.: For C_{L}-max = 1.86µF, C_L = 1.5µF is a good choice). Then substitute the chosen value into the same equation and re-calculate the value of R_1. Choose the 1% resistor standard value closest to this re-calculated value of R_1. The error due to the mismatch of the two time constants is expressed in Equation 28:

$$\varepsilon_\tau = \left(1 - \frac{R_1\cdot C_L\cdot DCR}{L_{avg}}\right)\cdot 100\% \quad \text{(EQ. 28)}$$

The value of R_2 should be simply five times that of R_1:

$$R_2 = 5\cdot R_1 \quad \text{(EQ. 29)}$$

For the $R_{DS(ON)}$ current sensing method, the external low side MOSFET will act as the sensing element as indicated in Figure 16.

Current Limit Threshold Selection

It is recommended that the user include a current limiting mechanism in their design to protect the power supply from damage and prevent excessive current from being drawn from the input supply in the event that the output is shorted to ground or an overload condition is imposed on the output. Current limiting is accomplished by sensing the current through the circuit during a portion of the duty cycle.

Output current sensing can be accomplished by measuring the voltage across a series resistive sensing element according to Equation 30:

$$V_{LIM} = I_{LIM}\times R_{SENSE} \quad \text{(EQ. 30)}$$

Where:

I_{LIM} is the desired maximum current that should flow in the circuit.

R_{SENSE} is the resistance of the sensing element.

V_{LIM} is the voltage across the sensing element at the point the circuit should start limiting the output current.

The ZL2008 supports “lossless” current sensing by measuring the voltage across a resistive element that is already present in the circuit. This eliminates additional efficiency losses incurred by devices that must use an additional series resistance in the circuit.

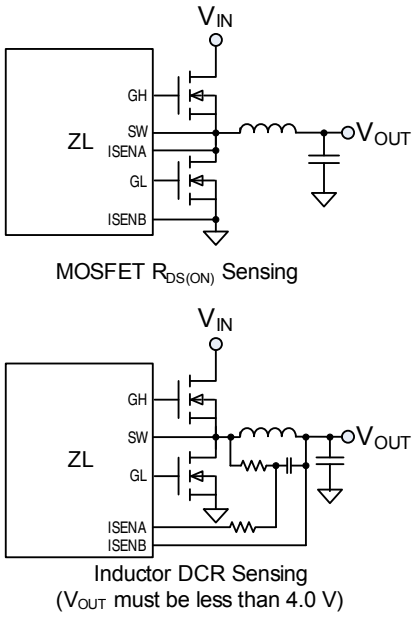


FIGURE 16. Current Sensing Methods

To set the current limit threshold, the user must first select a current sensing method. The ZL2008 incorporates two methods for current sensing, synchronous MOSFET $R_{DS(ON)}$ sensing and inductor DC resistance (DCR) sensing; Figure 16 shows a simplified schematic for each method. The current sensing method can be selected using the CFG2 pin, as shown in Tables 26 and 28, or via the I^2C/SMBus interface. Please refer to Application Note AN2033 for details.

In addition to selecting the current sensing method, the ZL2008 gives the power supply designer several choices for the fault response during over or under current condition. The user can select the number of violations allowed before declaring fault, a blanking time and the action taken when a fault is detected.

The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after a switching transition (less accurate due to potential ringing). It is a configurable parameter.

Once the sensing method has been selected, the user must select the voltage threshold (VLIM), the desired current limit threshold, and the resistance of the sensing element.

The current limit threshold voltage can be selected by simply connecting the ILIM pin as shown in Table 14. The ground-referenced sensing method is being used in this mode. By default, the IOUT_CAL_GAIN is set to 1mΩ for DCR mode and 2mΩ for RDS mode.

TABLE 14. Current Limit Threshold Voltage Pin-strap Settings

ILIM Pin	R_{DS} V_{LIM} (mV)	DCR V_{LIM} (mV)
LOW	50	25
OPEN	60	30
HIGH	70	35

TABLE 15. Current Limit Threshold Voltage Resistor Settings

R_{LIM} (kΩ)	R_{DS} V_{LIM} (mV)	DCR V_{LIM} (mV)
10	0	0
11	5	2.5
12.1	10	5
13.3	15	7.5
14.7	20	10
16.2	25	12.5
17.8	30	15
19.6	35	17.5
21.5	40	20
23.7	45	22.5
26.1	50	25
28.7	55	27.5
31.6	60	30
34.8	65	32.5
38.3	70	35
42.2	75	37.5
46.4	80	40
51.1	85	42.5
56.2	90	45
61.9	95	47.5
68.1	100	50
75	105	52.5
82.5	110	55
90.9	115	57.5
100	120	60

The threshold voltage can also be selected in 5mV increments by connecting a resistor, R_{LIM}, between the ILIM pin and ground according to Table 15. This method is preferred if the user does not desire to use or does not have access to the I²C/SMBus interface and the desired threshold value is contained in Table 15.

The current limit threshold can also be set to a custom value via the I²C/SMBus interface. Please refer to Application Note AN2033 for further details.

Loop Compensation

The ZL2008 operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. Although the ZL2008 uses a digital control loop, it operates much like a traditional analog PWM controller. Figure 17 is a simplified block diagram of the ZL2008 control loop, which differs from an analog control loop only by the constants in the PWM and compensation blocks. As in the analog controller case, the compensation block compares the output voltage to the desired voltage reference and compensation zeroes are added to keep the loop stable. The resulting integrated error signal is used to drive the PWM logic, converting the error signal to a duty cycle to drive the external MOSFETs.

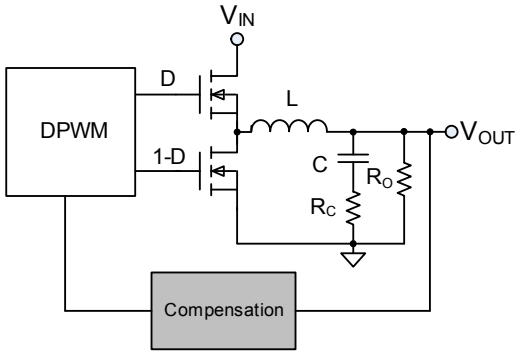


FIGURE 17. Control Loop Block Diagram

In the ZL2008, the compensation zeros and gain are set by configuring the FC0 and FC1 pins or via the I²C/SMBus interface once the user has calculated the required settings. This method eliminates the inaccuracies due to the component tolerances associated with using external resistors and capacitors required with traditional analog controllers.

The compensation is configured using a baseline set of PID taps which are scaled on the factors of Gain, Q and Fn as shown in Tables 16, 17 and 18. The parameters Gain, Q and Fn are defined in AN2035 and are parameters of the compensator (not the power stage being compensated).

The selection of these scaling factors is based on compensation required for additional output capacitance used in an application.

TABLE 16. FC0 Pin-strap Settings

FC0 Pin	Gain Scale (dB)	Q-new/Q-base
LOW	-12	1
OPEN	0	
HIGH	6	

TABLE 17. FC1 Pin-strap Settings

FC1 Pin	Fn-new/Fn-base
LOW	1
OPEN	
HIGH	

The scaling factors are applied to the baseline set of taps to achieve the desired compensation results. These baseline taps correspond to zeroes of the form:

$$G_{base}\left[1+\frac{s}{(Q_{base}*2\pi f_{nbase})}+\left(\frac{s}{(Q_{base}*2\pi f_{nbase})}\right)^2\right] \quad \text{(EQ. 31)}$$

Where G_{base} = 20dB

Q_{base} = 2

$f_{nbase} = f_{SW}/10$

Both the baseline taps and the calculated taps determined by the FC0 and FC1 resistors can be read via the I²C/SMBus interface. Please refer to Application Note AN2033 for further details.

TABLE 18. Loop Compensation Resistor Settings

R_{FC0} (kΩ)	Gain Scale (dB)	Q-new/Q-base	R_{FC1} (kΩ)	Fn-new/Fn-base
10	12	0.6813	10	1.0000
11		0.4642	11	0.9050
12.1		0.3162	12.1	0.8190
13.3		0.2154	13.3	0.7411
14.7		0.1468	14.7	0.6707
16.2		0.1000	16.2	0.6070
17.8	6	0.6813	17.8	0.5493
19.6		0.4642	19.6	0.4971
21.5		0.3162	21.5	0.4498
23.7		0.2154	23.7	0.4071
26.1		0.1468	26.1	0.3684
28.7		0.1000	28.7	0.3334
31.6	0	0.6813	31.6	0.3017
34.8		0.4642	34.8	0.2730
38.3		0.3162	38.3	0.2471
42.2		0.2154	42.2	0.2236
46.4		0.1468	46.4	0.2024
51.1		0.1000	51.1	0.1831
56.2	-6	1.0000	56.2	0.1657
61.9		0.6813	61.9	0.1500
68.1		0.4642	68.1	0.1357
75		0.3162	75	0.1228
82.5		0.2154	82.5	0.1112
90.9		0.1468	90.9	0.1006
100		0.1000	100	0.0910
110	-12	0.6813	110	0.0824
121		0.4642	121	0.0745
133		0.3162	133	0.0675
147		0.2154	147	0.0611
162		0.1468	162	0.0553
178		0.1000	178	0.0500

Non-linear Response (NLR) Settings

The ZL2008 incorporates a non-linear response (NLR) loop that decreases the response time and the output voltage deviation in the event of a sudden output load current step. The NLR loop incorporates a secondary error signal processing path that bypasses the primary error loop when the output begins to transition outside of the standard regulation limits. This scheme results in a higher equivalent loop bandwidth than what is possible using a traditional linear loop.

When a load current step function imposed on the output causes the output voltage to drop below the lower regulation limit, the NLR circuitry will force a positive correction signal that will turn on the upper MOSFET and quickly force the output to increase. Conversely, a negative load step (i.e. removing a large load current) will cause the NLR circuitry to force a negative correction signal that will turn on the lower MOSFET and quickly force the output to decrease.

NLR can be configured using resistor pin-straps as follows:

CFG0 disables NLR or enables NLR inner thresholds to 1.5%, 2% or 3% (see Table 30).

CFG1 sets NLR inner thresholds timeout and blanking to 1 and 4 or 2 and 8 (see Table 27).

Please refer to Application Note AN2032 for more details regarding NLR settings.

Efficiency Optimized Driver Dead-time Control

The ZL2008 utilizes a closed loop algorithm to optimize the dead-time applied between the gate drive signals for the top and bottom FETs. In a synchronous buck converter, the MOSFET drive circuitry must be designed such that the top and bottom MOSFETs are never in the conducting state at the same time. Potentially damaging currents flow in the circuit if both top and bottom MOSFETs are simultaneously on for periods of time exceeding a few nanoseconds. Conversely, long periods of time in which both MOSFETs are off reduce overall circuit efficiency by allowing current to flow in their parasitic body diodes.

It is therefore advantageous to minimize this dead-time to provide optimum circuit efficiency. In the first order model of a buck converter, the duty cycle is determined by Equation 32:

$$D \approx \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 32)}$$

However, non-idealities exist that cause the real duty cycle to extend beyond the ideal. Dead-time is one of those non-idealities that can be manipulated to improve efficiency. The ZL2008 has an internal algorithm that constantly adjusts dead-time non-overlap to minimize duty cycle, thus maximizing efficiency. This circuit will null out dead-time differences due to component variation, temperature, and loading effects.

This algorithm is independent of application circuit parameters such as MOSFET type, gate driver delays, rise and fall times and circuit layout. In addition, it does not require drive or MOSFET voltage or current waveform measurements.

Adaptive Diode Emulation

Most power converters use synchronous rectification to optimize efficiency over a wide range of input and output conditions. However, at light loads the synchronous MOSFET will typically sink current and introduce additional energy losses associated with higher peak inductor currents, resulting in reduced efficiency. Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is available to single-phase devices only.

Note: the overall bandwidth of the device may be reduced when in diode emulation mode. It is recommended that diode emulation is disabled prior to applying significant load steps.

Adaptive Frequency Control

Since switching losses contribute to the efficiency of the power converter, reducing the switching frequency will reduce the switching losses and increase efficiency. The ZL2008 includes Adaptive Frequency Control mode, which effectively reduces the observed switching frequency as the load decreases.

Adaptive frequency mode is enabled by setting bit 0 of MISC_CONFIG to 1 and is only available while the device is operating within Adaptive Diode Emulation Mode. As the load current is decreased, diode emulation mode decreases the GL on-time to prevent negative inductor current from flowing. As the load is decreased further, the GH pulse width will begin to decrease while maintaining the programmed frequency, f_{PROG} (set by the FREQ_SWITCH command).

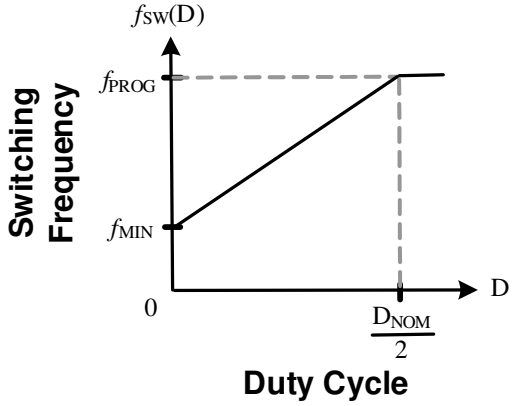


FIGURE 18. Adaptive Frequency

Once the GH pulse width (D) reaches 50% of the nominal duty cycle, D_{NOM} (determined by Vin and Vout), the switching frequency will start to decrease according to Equation 33:

If

$$\frac{D_{NOM}}{2}$$

then,

$$\left(\frac{2(f_{SW} - f_{MIN})}{D_{NOM}}\right)D + f_{MIN} \quad \text{(EQ. 33)}$$

Otherwise $f_{SW}(D) = f_{PROG}$

This is illustrated in Figure 18. Due to quantizing effects inside the IC, the ZL2008 will decrease its frequency in steps between f_{SW} and f_{MIN}. The quantity and magnitude of the steps will depend on the difference between f_{SW} and f_{MIN} as well as the frequency range.

Adaptive frequency mode is not available for current sharing groups when using an external clock, or if the device is outputting a clock signal on its SYNC pin.

Power Management Functional Description

Input Undervoltage Lockout

The input undervoltage lockout (UVLO) prevents the ZL2008 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 2.85V and 16V using the UVLO pin. The simplest implementation is to connect the UVLO pin as shown in Table 19. If the UVLO pin is left unconnected, the UVLO threshold will default to 4.5V.

TABLE 19. UVLO Threshold Pin-strap Settings

UVLO Pin	UVLO Threshold (V)
LOW	3
OPEN	4.5
HIGH	10.8

If the desired UVLO threshold is not one of the listed choices, the user can configure a threshold between 2.85V and 16V by connecting a resistor between the UVLO pin and SGND by selecting the appropriate resistor from Table 20.

TABLE 20. UVLO Threshold Resistor Settings

R_{UVLO} (kΩ)	UVLO (V)
17.8	2.85
19.6	3.14
21.5	3.44
23.7	3.79
26.1	4.18
28.7	4.59
31.6	5.06
34.8	5.57
38.3	6.13
42.2	6.75
46.4	7.42
51.1	8.18
56.2	8.99
61.9	9.9
68.1	10.9
75	12
82.5	13.2
90.9	14.54
100	16

The UVLO voltage can also be set to any value between 2.85V and 16V via the I^2C/SMBus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the ZL2008 will be re-enabled.