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**Features**

April 2010

- Synchronizes to clock-and-sync-pair to maintain minimal phase skew between an H.110 primary master clock and a secondary master clock
- Supports Telcordia GR-1244-CORE Stratum 4 and 4E
- Supports ITU-T G.823 and G.824 for 2048 kbit/s and 1544 kbit/s interfaces
- Supports ANSI T1.403 and ETSI ETS 300 011 for ISDN primary rate interfaces
- Simple hardware control interface
- Manual and Automatic hitless reference switching between any combination of valid input reference frequencies
- Accepts three input references and synchronizes to any combination of 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz or 16.384 MHz inputs
- Provides a range of clock outputs: 1.544 MHz, 2.048 MHz, 3.088 MHz, 6.312 MHz, 16.384 MHz and either 4.096 MHz and 8.192 MHz or 32.768 MHz and 65.536 MHz
- Provides 5 styles of 8 kHz framing pulses
- Holdover frequency accuracy of  $1 \times 10^{-7}$

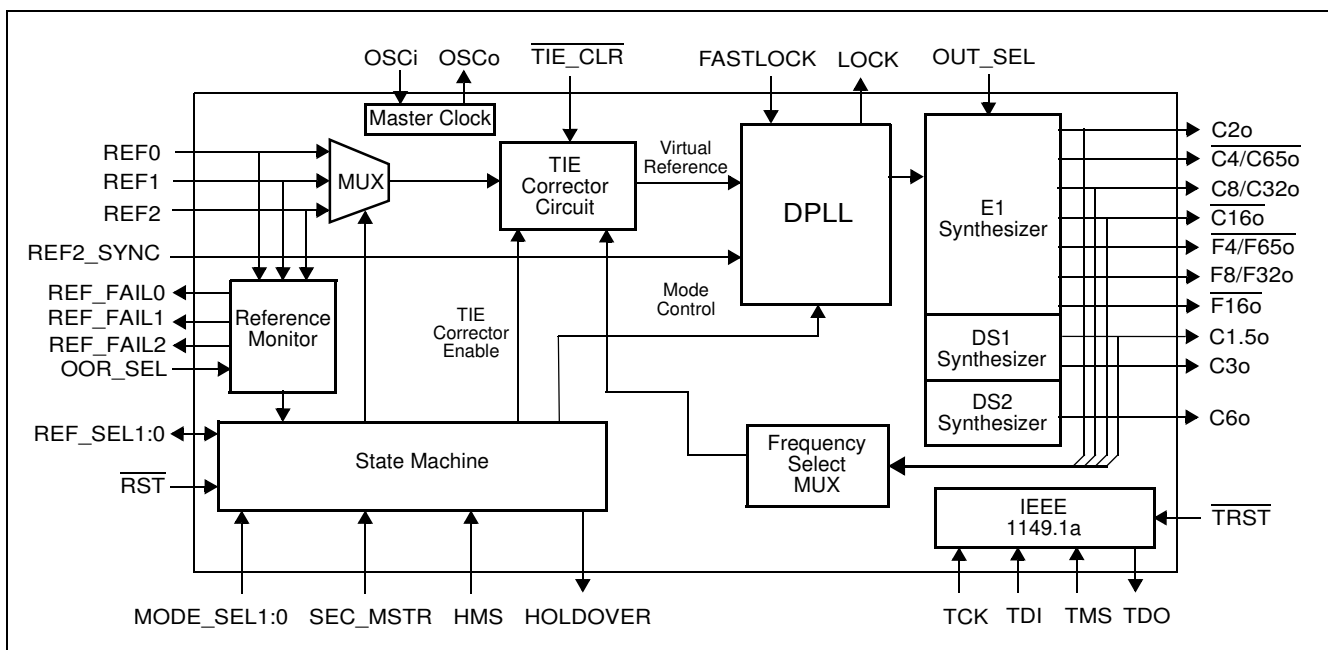
**Ordering Information**

ZL30102QDG1 64 pin TQFP\* Trays, Bake & Drypack  
 \*Pb Free Matte Tin  
**-40°C to +85°C**

- Provides Lock, Holdover and selectable Out of Range indication
- Attenuates wander from 1.8 Hz
- Less than 0.6 ns<sub>pp</sub> intrinsic jitter on all output clocks
- External master clock source: Clock Oscillator or Crystal

**Applications**

- Synchronization and timing control for multi-trunk DS1/ E1 terminal systems such as DSLAMs, Gateways and PBXs
- Clock and frame pulse source for H.110 CT Bus, ST-BUS, GCI and other time division multiplex (TDM) buses


**Figure 1 - Functional Block Diagram**

**Description**

The ZL30102 DS1/E1 Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization for DS1/E1 transmission equipment deploying redundant network clocks.

The ZL30102 generates ST-BUS and other TDM clock and framing signals that are phase locked to one of three network references or to another system master-clock reference. It helps ensure system reliability by monitoring its references for frequency accuracy and stability and by maintaining a tight phase alignment between the primary master-clock and secondary master clock outputs even in the presence of high network jitter.

The ZL30102 is intended to be the central timing and synchronization resource for network equipment that complies with Telcordia, ETSI, ITU-T and ANSI network specifications.

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## 1.0 Change Summary

Changes from November 2005 Issue to April 2010 Issue. Page, section, figure and table numbers refer to this current issue.

| Page | Item                     | Change  |
|------|--------------------------|---|
| 1    | Ordering Information Box | Leaded part number ZL30102QDG has been obsoleted and replaced by ZL30102QDG1. |

Changes from July 2005 Issue to November 2005 Issue. Page, section, figure and table numbers refer to this current issue.

| Page | Item        | Change   |
|------|-------------|--|
| 1    | Features    | Changed description for hitless reference switching.   |
| 32   | Section 6.1 | Removed power supply decoupling circuit and included reference to synchronizer power supply decoupling application note. |

Changes from October 2004 Issue to July 2005 Issue. Page, section, figure and table numbers refer to this current issue.

| Page | Item  | Change   |
|------|---|--|
| 9    | $\overline{\text{RST}}$ pin                       | Specified clock and frame pulse outputs forced to high impedance |
| 36   | Table "DC Electrical Characteristics**"           | Corrected Schmitt trigger levels                                 |
| 44   | Table "Performance Characteristics* - Functional" | Gave more detail on fast-lock Lock Time conditions               |

Changes from July 2004 Issue to October 2004 Issue. Page, section, figure and table numbers refer to this current issue.

| Page | Item   | Change  |
|------|--|---|
| 7    | Figure 2   | Added note specifying not e-Pad   |
| 17   | Section 3.3  | Changed 20 ns to 200 ns in "HMS=0" section                                    |
| 36   | Table "DC Electrical Characteristics**"  | Corrected current consumption<br>Corrected $V_t$ input voltage characteristic |
| 39   | Table "AC Electrical Characteristics* - Input to output timing for REF0, REF1 and REF2 references when TIE_CLR = 0 (see Figure 24)." | Corrected Min. Max. values  |
| 40   | Section 7.1  | Corrected pulse widths  |
| 45   | Section 7.2  | Corrected jitter numbers  |

2.0 Physical Description

2.1 Pin Connections

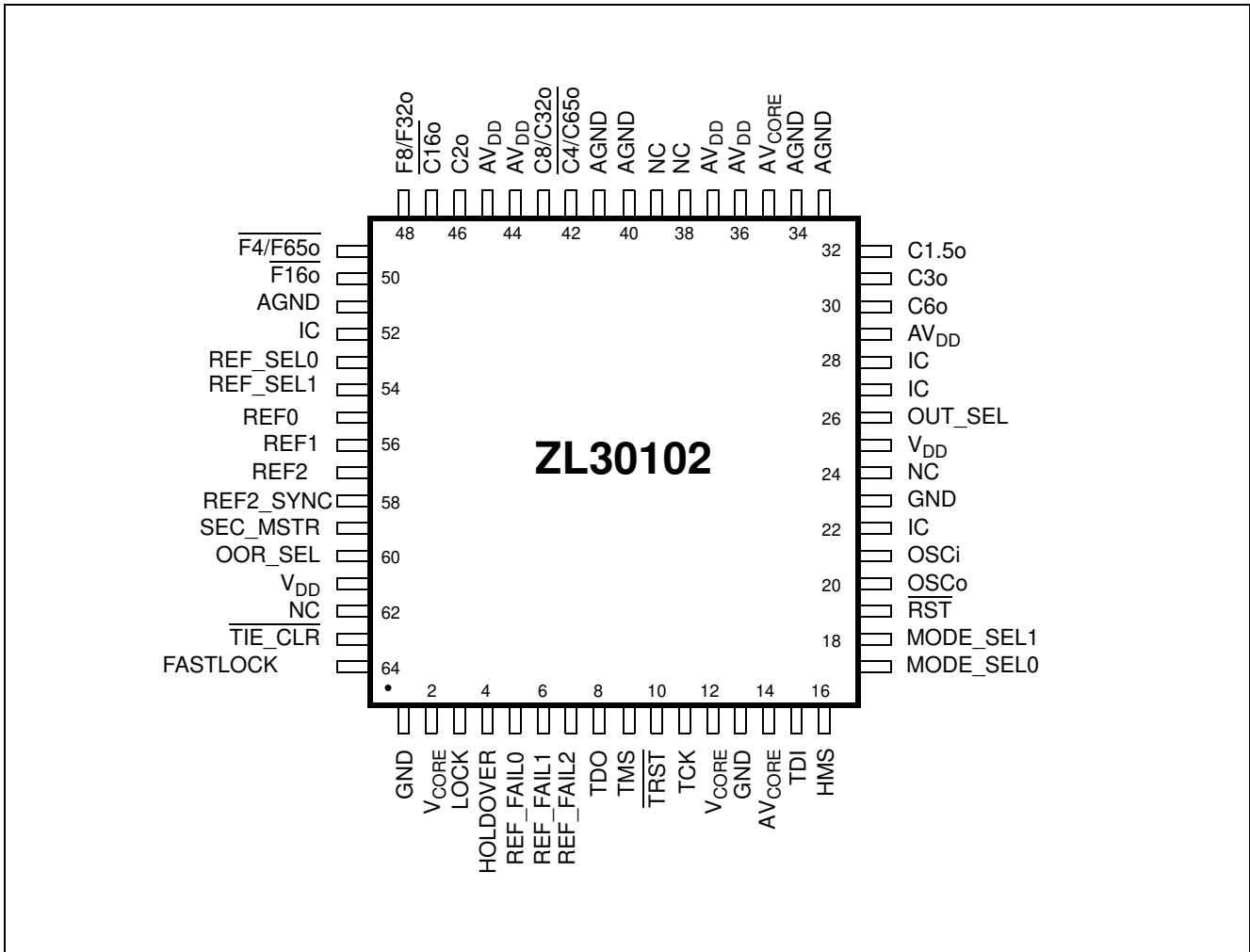


Figure 2 - Pin Connections (64 pin TQFP, please see Note 1)

Note 1: The ZL30102 uses the TQFP shown in the package outline designated with the suffix QD, the ZL30102 does not use the e-Pad TQFP.



## 2.2 Pin Description

| Pin # | Name                     | Description   |
|-------|--------------------------|---|
| 1     | GND                      | <b>Ground.</b> 0 V  |
| 2     | V <sub>CORE</sub>        | <b>Positive Supply Voltage.</b> +1.8 V <sub>DC</sub> nominal  |
| 3     | LOCK                     | <b>Lock Indicator (Output).</b> This output goes to a logic high when the PLL is frequency locked to the selected input reference.  |
| 4     | HOLDOVER                 | <b>Holdover (Output).</b> This output goes to a logic high whenever the PLL goes into holdover mode.  |
| 5     | REF_FAIL0                | <b>Reference 0 Failure Indicator (Output).</b> A logic high at this pin indicates that the REF0 reference frequency has exceeded the out-of-range limit set by the OOR_SEL pin or that it is exhibiting abrupt phase or frequency changes.  |
| 6     | REF_FAIL1                | <b>Reference 1 Failure Indicator (Output).</b> A logic high at this pin indicates that the REF1 reference frequency has exceeded the out-of-range limit set by the OOR_SEL pin or that it is exhibiting abrupt phase or frequency changes.  |
| 7     | REF_FAIL2                | <b>Reference 2 Failure Indicator (Output).</b> A logic high at this pin indicates that the REF2 reference frequency has exceeded the out-of-range limit set by the OOR_SEL pin or that it is exhibiting abrupt phase or frequency changes.  |
| 8     | TDO                      | <b>Test Serial Data Out (Output).</b> JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.  |
| 9     | TMS                      | <b>Test Mode Select (Input).</b> JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V <sub>DD</sub> . If this pin is not used then it should be left unconnected.   |
| 10    | $\overline{\text{TRST}}$ | <b>Test Reset (Input).</b> Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to V <sub>DD</sub> . If this pin is not used then it should be connected to GND.   |
| 11    | TCK                      | <b>Test Clock (Input):</b> Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.   |
| 12    | V <sub>CORE</sub>        | <b>Positive Supply Voltage.</b> +1.8 V <sub>DC</sub> nominal  |
| 13    | GND                      | <b>Ground.</b> 0 V  |
| 14    | AV <sub>CORE</sub>       | <b>Positive Analog Supply Voltage.</b> +1.8 V <sub>DC</sub> nominal   |
| 15    | TDI                      | <b>Test Serial Data In (Input).</b> JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V <sub>DD</sub> . If this pin is not used then it should be left unconnected.  |
| 16    | HMS                      | <b>Hitless Mode Switching (Input).</b> The HMS input controls phase accumulation during the transition from Holdover or Freerun mode to Normal mode on the same reference. A logic low at this pin will cause the ZL30102 to maintain the delay stored in the TIE corrector circuit when it transitions from Holdover or Freerun mode to Normal mode. A logic high on this pin will cause the ZL30102 to measure a new delay for its TIE corrector circuit thereby minimizing the output phase movement when it transitions from Holdover or Freerun mode to Normal mode. |
| 17    | MODE_SEL0                | <b>Mode Select 0 (Input).</b> This input combined with MODE_SEL1 determines the mode of operation, see Table 4 on page 20.  |
| 18    | MODE_SEL1                | <b>Mode Select 1 (Input).</b> See MODE_SEL0 pin description.  |

| Pin # | Name                        | Description  |
|-------|-----------------------------|--|
| 19    | $\overline{\text{RST}}$     | <b>Reset (Input).</b> A logic low at this input resets the device. On power up, the $\overline{\text{RST}}$ pin must be held low for a minimum of 300 ns after the power supply pins have reached the minimum supply voltage. When the RST pin goes high, the device will transition into a Reset state for 3 ms. In the Reset state all clock and frame pulse outputs will be forced into high impedance. |
| 20    | OSCo                        | <b>Oscillator Master Clock (Output).</b> For crystal operation, a 20 MHz crystal is connected from this pin to OSCi. This output is not suitable for driving other devices. For clock oscillator operation, this pin must be left unconnected.   |
| 21    | OSCi                        | <b>Oscillator Master Clock (Input).</b> For crystal operation, a 20 MHz crystal is connected from this pin to OSCo. For clock oscillator operation, this pin must be connected to a clock source.  |
| 22    | IC                          | <b>Internal Connection.</b> Leave unconnected.   |
| 23    | GND                         | <b>Ground.</b> 0 V   |
| 24    | NC                          | <b>No internal bonding Connection.</b> Leave unconnected.  |
| 25    | V <sub>DD</sub>             | <b>Positive Supply Voltage.</b> +3.3 V <sub>DC</sub> nominal   |
| 26    | OUT_SEL                     | <b>Output Selection (Input).</b> This input selects the signals on the combined output clock and frame pulse pins, see Table 3 on page 19.   |
| 27    | IC                          | <b>Internal Connection.</b> Connect this pin to ground.  |
| 28    | IC                          | <b>Internal Connection.</b> Connect this pin to ground.  |
| 29    | AV <sub>DD</sub>            | <b>Positive Analog Supply Voltage.</b> +3.3 V <sub>DC</sub> nominal  |
| 30    | C6o                         | <b>Clock 6.312 MHz (Output).</b> This output is used in DS2 applications.  |
| 31    | C3o                         | <b>Clock 3.088 MHz (Output).</b> This output is used in DS1 applications.  |
| 32    | C1.5o                       | <b>Clock 1.544 MHz (Output).</b> This output is used in DS1 applications.<br>This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.  |
| 33    | AGND                        | <b>Analog Ground.</b> 0 V  |
| 34    | AGND                        | <b>Analog Ground.</b> 0 V  |
| 35    | AV <sub>CORE</sub>          | <b>Positive Analog Supply Voltage.</b> +1.8 V <sub>DC</sub> nominal  |
| 36    | AV <sub>DD</sub>            | <b>Positive Analog Supply Voltage.</b> +3.3 V <sub>DC</sub> nominal  |
| 37    | AV <sub>DD</sub>            | <b>Positive Analog Supply Voltage.</b> +3.3 V <sub>DC</sub> nominal  |
| 38    | NC                          | <b>No internal bonding Connection.</b> Leave unconnected.  |
| 39    | NC                          | <b>No internal bonding Connection.</b> Leave unconnected.  |
| 40    | AGND                        | <b>Analog Ground.</b> 0 V  |
| 41    | AGND                        | <b>Analog Ground.</b> 0 V  |
| 42    | $\overline{\text{C4/C65o}}$ | <b>Clock 4.096 MHz or 65.536 MHz (Output).</b> This output is used for ST-BUS operation at 2.048 Mbit/s, 4.096 Mbit/s or 65.536 MHz (ST-BUS 65.536 Mbit/s). The output frequency is selected via the OUT_SEL pin, see Table 3 on page 19.  |

| Pin # | Name                        | Description   |
|-------|-----------------------------|---|
| 43    | C8/C32o                     | <b>Clock 8.192 MHz or 32.768 MHz (Output).</b> This output is used for ST-BUS and GCI operation at 8.192 Mb/s or for operation with a 32.768 MHz clock. The output frequency is selected via the OUT_SEL pin, see Table 3 on page 19.<br><br>In C8 mode, this clock output pad uses an included Schmitt input as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.                          |
| 44    | AV <sub>DD</sub>            | <b>Positive Analog Supply Voltage.</b> +3.3 V <sub>DC</sub> nominal   |
| 45    | AV <sub>DD</sub>            | <b>Positive Analog Supply Voltage.</b> +3.3 V <sub>DC</sub> nominal   |
| 46    | C2o                         | <b>Clock 2.048 MHz (Output).</b> This output is used for standard E1 interface timing and for ST-BUS operation at 2.048 Mbit/s.<br><br>This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.   |
| 47    | $\overline{\text{C16o}}$    | <b>Clock 16.384 MHz (Output).</b> This output is used for ST-BUS operation with a 16.384 MHz clock.<br><br>This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.   |
| 48    | F8/F32o                     | <b>Frame Pulse (Output).</b> This is an 8 kHz 122 ns active high framing pulse or it is an 8 kHz 31 ns active high framing pulse, which marks the beginning of a frame. The pulse width is selected via the OUT_SEL pin, see Table 3 on page 19.  |
| 49    | $\overline{\text{F4/F65o}}$ | <b>Frame Pulse ST-BUS 2.048 Mbit/s or ST-BUS at 65.536 MHz clock (Output).</b> This output is an 8 kHz 244 ns active low framing pulse which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mbit/s and 4.096 Mbit/s. Or this output is an 8 kHz 15 ns active low framing pulse, typically used for ST-BUS operation with a clock rate of 65.536 MHz. The pulse width is selected via the OUT_SEL pin, see Table 3 on page 19. |
| 50    | $\overline{\text{F16o}}$    | <b>Frame Pulse ST-BUS 8.192 Mbit/s (Output).</b> This is an 8 kHz 61 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mbit/s.  |
| 51    | AGND                        | <b>Analog Ground.</b> 0 V   |
| 52    | IC                          | <b>Internal Connection.</b> Connect this pin to ground.   |
| 53    | REF_SEL0                    | <b>Reference Select 0 (Input/Output).</b> In the manual mode of operation, REF_SEL0 is an input. As an input REF_SEL0 combined with REF_SEL1 selects the reference input that is used for synchronization, see Table 6 on page 23.<br><br>In the Automatic mode of operation, REFSEL0 is an output indicating which of the input references is the being selected. This pin is internally pulled down to GND.   |
| 54    | REF_SEL1                    | <b>Reference Select 1 (Input/Output).</b> See REF_SEL0 pin description.   |
| 55    | REF0                        | <b>Reference (Input).</b> This is one of three (REF0, REF1 and REF2) input reference sources used for synchronization. One of five possible frequencies may be used: 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz or 16.384 MHz. This pin is internally pulled down to GND.   |
| 56    | REF1                        | <b>Reference (Input).</b> See REF0 pin description.   |
| 57    | REF2                        | <b>Reference (Input).</b> See REF0 pin description.   |

| Pin # | Name                         | Description   |
|-------|------------------------------|---|
| 58    | REF2_SYNC                    | <b>REF2 Synchronization Frame Pulse (Input).</b> This is the 8 kHz frame pulse synchronization input associated with the REF2 reference. While the PLL is locked to the REF2 input reference the output (multi) frame pulses are synchronized to this input. This pin is internally pulled down to GND.   |
| 59    | SEC_MSTR                     | <b>Secondary Master Mode Selection (Input).</b> A logic low at this pin selects the Primary Master mode of operation with 1.8 Hz DPLL loop filter bandwidth. A logic high selects Secondary Master mode which forces the PLL to clear its TIE corrector circuit and lock to the selected reference using a high bandwidth loop filter and a phase slope limiting of 9.5 ms/s. |
| 60    | OOR_SEL                      | <b>Out Of Range Selection (Input).</b> This input selects the frequency out of range limits of the reference inputs, see Table 1 on page 19.  |
| 61    | V <sub>DD</sub>              | <b>Positive Supply Voltage.</b> +3.3 V <sub>DC</sub> nominal  |
| 62    | NC                           | <b>No internal bonding Connection.</b> Leave unconnected.   |
| 63    | $\overline{\text{TIE\_CLR}}$ | <b>TIE Circuit Reset (Input).</b> A logic low at this input resets the Time Interval Error (TIE) correction circuit resulting in a realignment of input phase with output phase.  |
| 64    | FASTLOCK                     | <b>Fast Lock (Input).</b> Set temporarily high to allow the ZL30102 to quickly lock to the input reference (one second locking time).   |

### 3.0 Functional Description

The ZL30102 is an SDH/PDH Synchronizer for Redundant System Clocks, providing timing and synchronization signals to interface circuits for the following types of primary rate digital transmission links, see Table 1:

- DS1 compliant with ANSI T1.403 and Telcordia GR-1244-CORE Stratum 4/4E
- E1 compliant with ITU-T G.703 and ETSI ETS 300 011

Figure 1 is a functional block diagram of the ZL30102 which is described in the following sections.

#### 3.1 Reference Select Multiplexer (MUX)

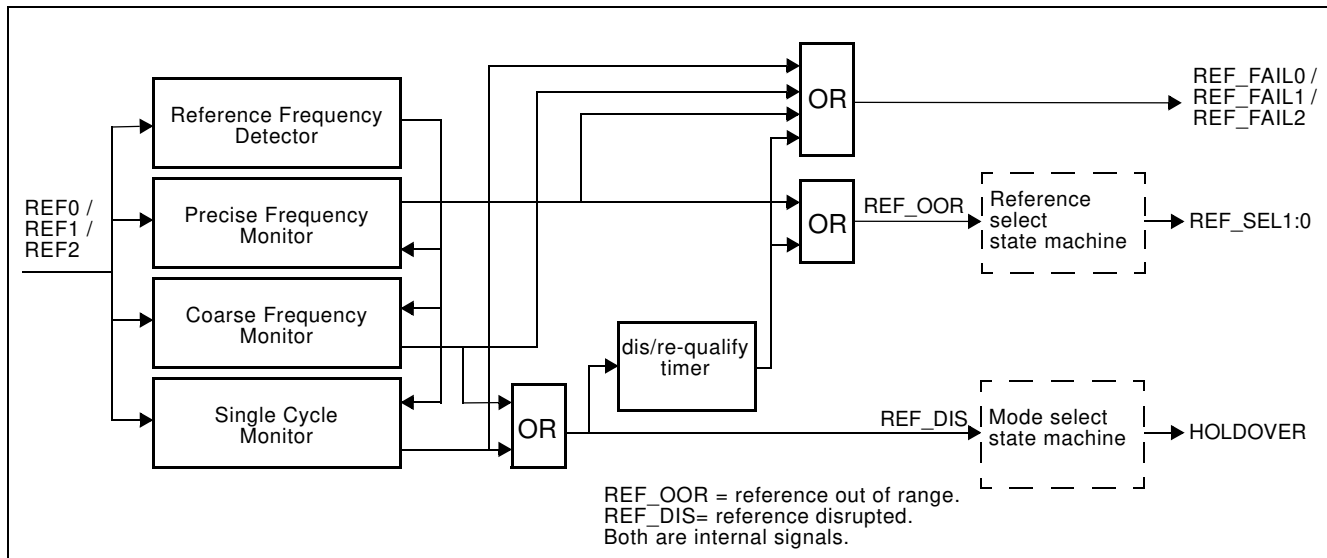
The ZL30102 accepts three simultaneous reference input signals and operates on their rising edges. One of them, the primary reference (REF0), the secondary reference (REF1) or the tertiary reference (REF2) signal is selected as input to the TIE Corrector Circuit based on the Reference Selection (REF\_SEL1:0) inputs.

The use of the combined REF2 and REF2\_SYNC inputs allows for a very accurate phase alignment of the output frame pulses to the 8 kHz frame pulse supplied to the REF2\_SYNC input. This feature supports the implementation of Primary and Secondary Master system clocks in H.110 systems.

#### 3.2 Reference Monitor

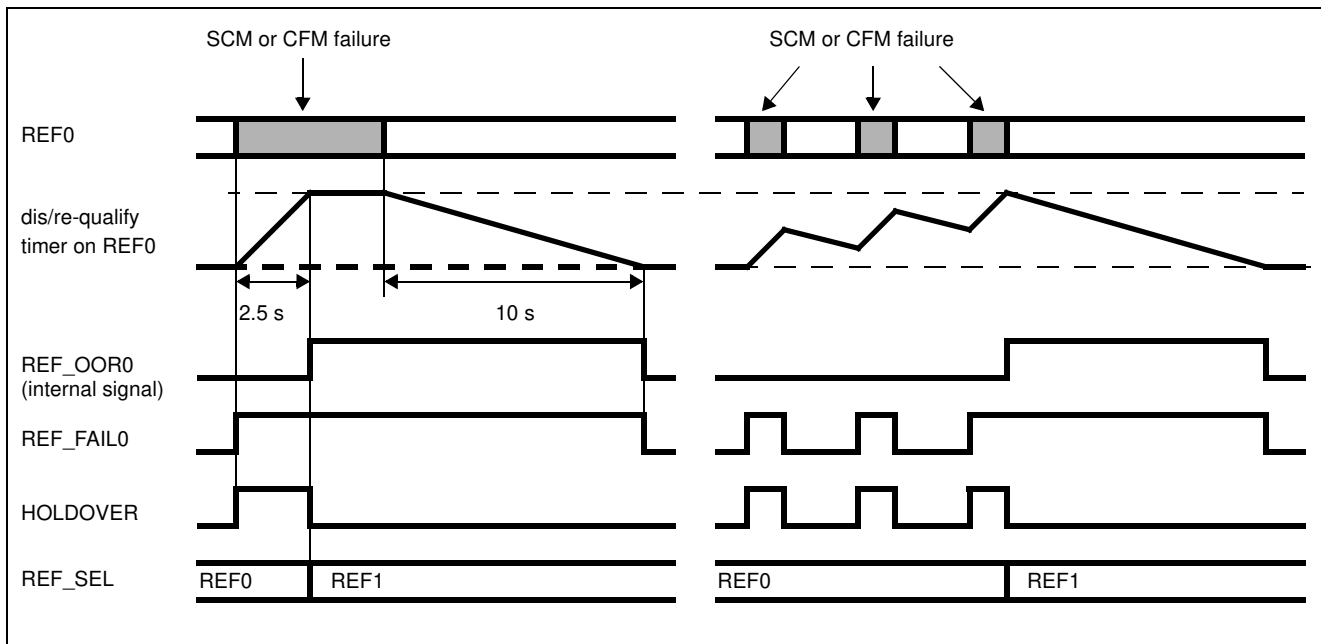
The input references are monitored by three independent reference monitor blocks, one for each reference. The block diagram of a single reference monitor is shown in Figure 3. For each reference clock, the frequency is detected and the clock is continuously monitored for three independent criteria that indicate abnormal behavior of the reference signal, for example; long term drift from its nominal frequency or excessive jitter. To ensure proper operation of the reference monitor circuit, the minimum input pulse width restriction of 15 nsec must be observed.

- **Reference Frequency Detector (RFD):** This detector determines whether the frequency of the reference clock is 8 kHz, 1.544 MHz, 2.048 MHz 8.192 MHz or 16.384 MHz and provides this information to the various monitor circuits and the phase detector circuit of the DPLL.
- **Precise Frequency Monitor (PFM):** This circuit determines whether the frequency of the reference clock is within the selected accuracy range, see Table 1.
- **Coarse Frequency Monitor (CFM):** This circuit monitors the reference frequency over intervals of approximately 30  $\mu$ s to quickly detect large frequency changes.
- **Single Cycle Monitor (SCM):** This detector checks the period of a single clock cycle to detect large phase hits or the complete loss of the clock.



**Figure 3 - Reference Monitor Circuit**

Exceeding the thresholds of any of the monitors forces the corresponding REF\_FAIL pin to go high. The single cycle and coarse frequency failure flags force the DPLL into Holdover mode and feed a timer that disqualifies the reference input signal when the failures are present for more than 2.5 s. The single cycle and coarse frequency failures must be absent for 10 s to let the timer re-qualify the input reference signal as valid. Multiple failures of less than 2.5 s each have an accumulative effect and will disqualify the reference eventually. This is illustrated in Figure 4 where REF0 experiences disruptions while REF1 is stable.

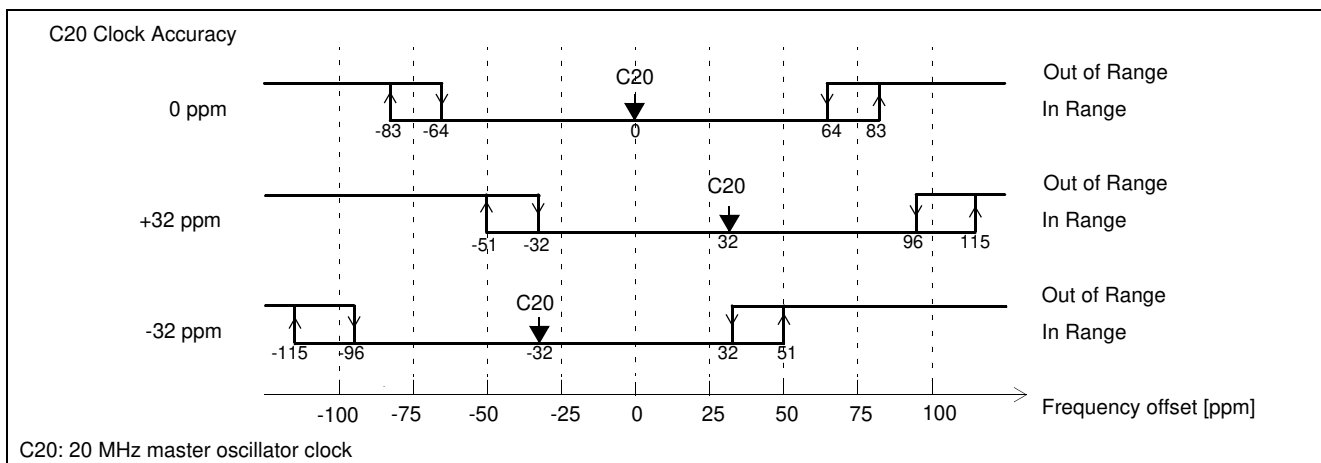


**Figure 4 - Behaviour of the Dis/Re-qualify Timer**

When the incoming signal returns to normal (REF\_FAIL=0), the DPLL returns to Normal mode with the output signal locked to the input signal. Each of the monitors has a built-in hysteresis to prevent flickering of the REF\_FAIL status pin at the threshold boundaries. The precise frequency monitor and the timer do not affect the mode (Holdover/Normal) of the DPLL.

If the device is set to Automatic mode (MODE\_SEL1:0=11), then the state machine does not immediately switch to another reference. If the single cycle and/or coarse frequency failures persist for more than 2.5 s or the precise frequency monitor detects a failure, then the state machine will switch to another valid reference if that is available. If there no other reference available, it stays in Holdover mode.

The precise frequency monitor's failure thresholds are selected with the OOR\_SEL input based on the ZL30102 applications, Table 1. Figure 5 and Figure 6 show the out of range limits for various master clock accuracies. It will take the precise frequency monitor up to 10 s to qualify or disqualify the input reference.



**Figure 5 - DS1 Out-of-Range Thresholds for OOR\_SEL=0**

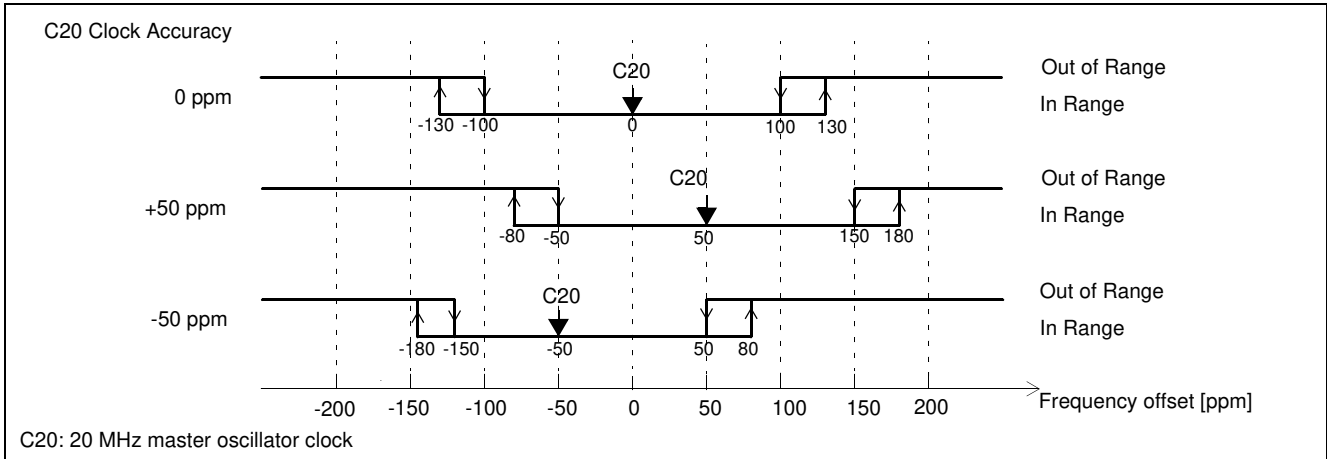


Figure 6 - E1 Out-of-Range Thresholds for OOR\_SEL=1

In addition to the monitoring of the REF2 reference signal the companion REF2\_SYNC input signal is also monitored for failure (see Figure 7).

**Sync Ratio Monitor (SRM):** This monitor detects if the REF2\_SYNC signal is an 8 kHz signal. It also checks the number of REF2 reference clock cycles in a single REF2\_SYNC frame pulse period to determine the integrity of the REF2\_SYNC signal, for example there must be exactly 256 clock cycles of a 2.048 MHz REF2 reference clock in a single REF2\_SYNC 8 kHz frame pulse period to validate the REF2\_SYNC signal. If the REF2 and REF2\_SYNC inputs are selected for synchronization and the Sync Ratio Monitor detects a failure, the DPLL will abandon the mechanism of aligning the output frame pulse to the REF2\_SYNC pulse. Instead only the REF2 reference will be used for synchronization.

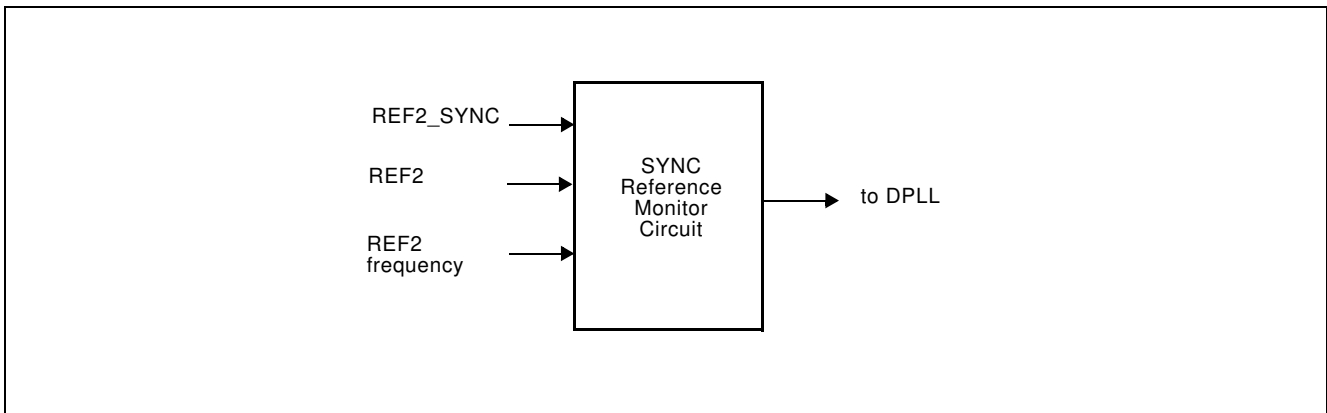


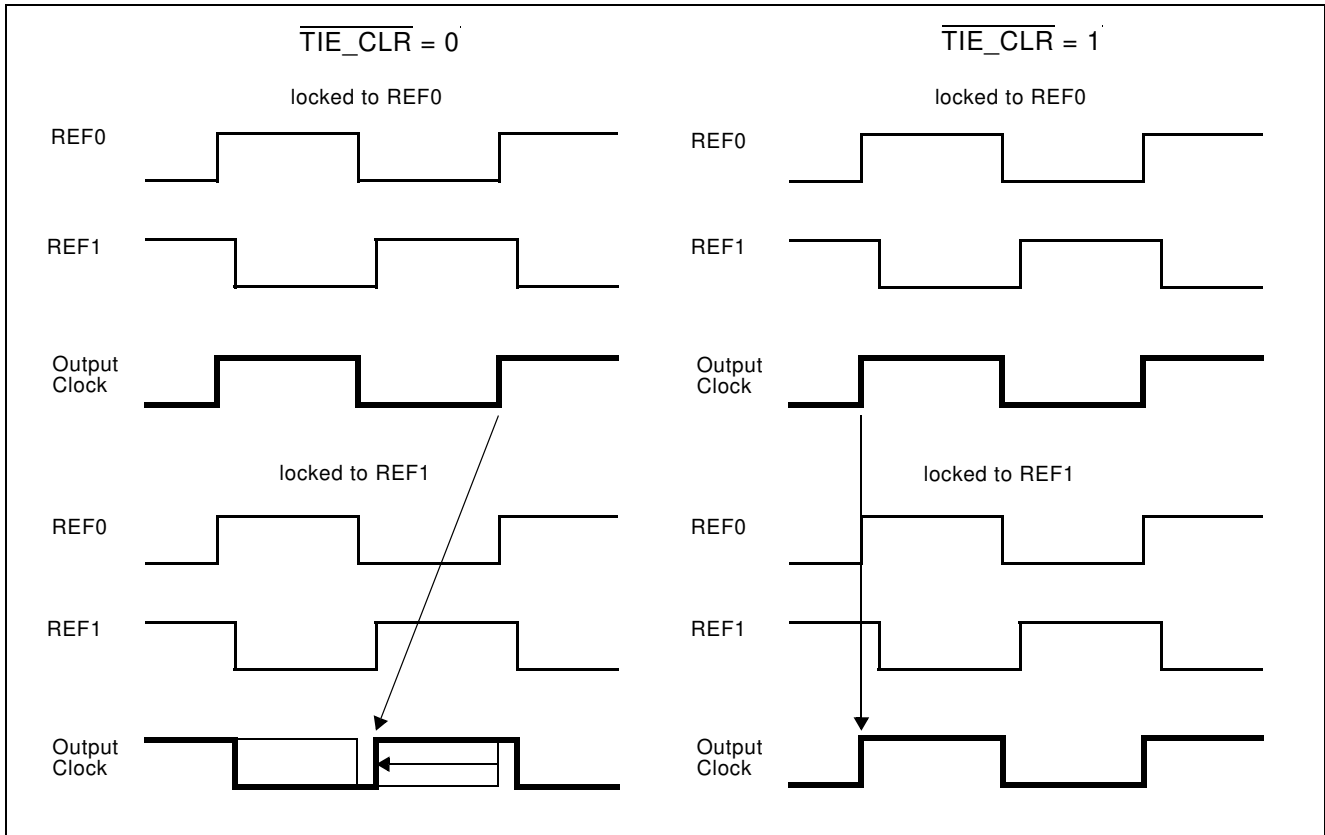
Figure 7 - REF2\_SYNC Reference Monitor

### 3.3 Time Interval Error (TIE) Corrector Circuit

The TIE Circuit eliminates phase transients on the output clock that may occur during reference switching or the recovery from Holdover mode to Normal mode.

On recovery from Holdover mode (dependent on the HMS pin) or when switching to another reference input, the TIE corrector circuit measures the phase delay between the current phase (feedback signal) and the phase of the selected reference signal. This delay value is stored in the TIE corrector circuit. This circuit creates a new virtual reference signal that is at the same phase position as the feedback signal. By using the virtual reference, the PLL minimizes the phase transient it experiences when it recovers from Holdover mode.

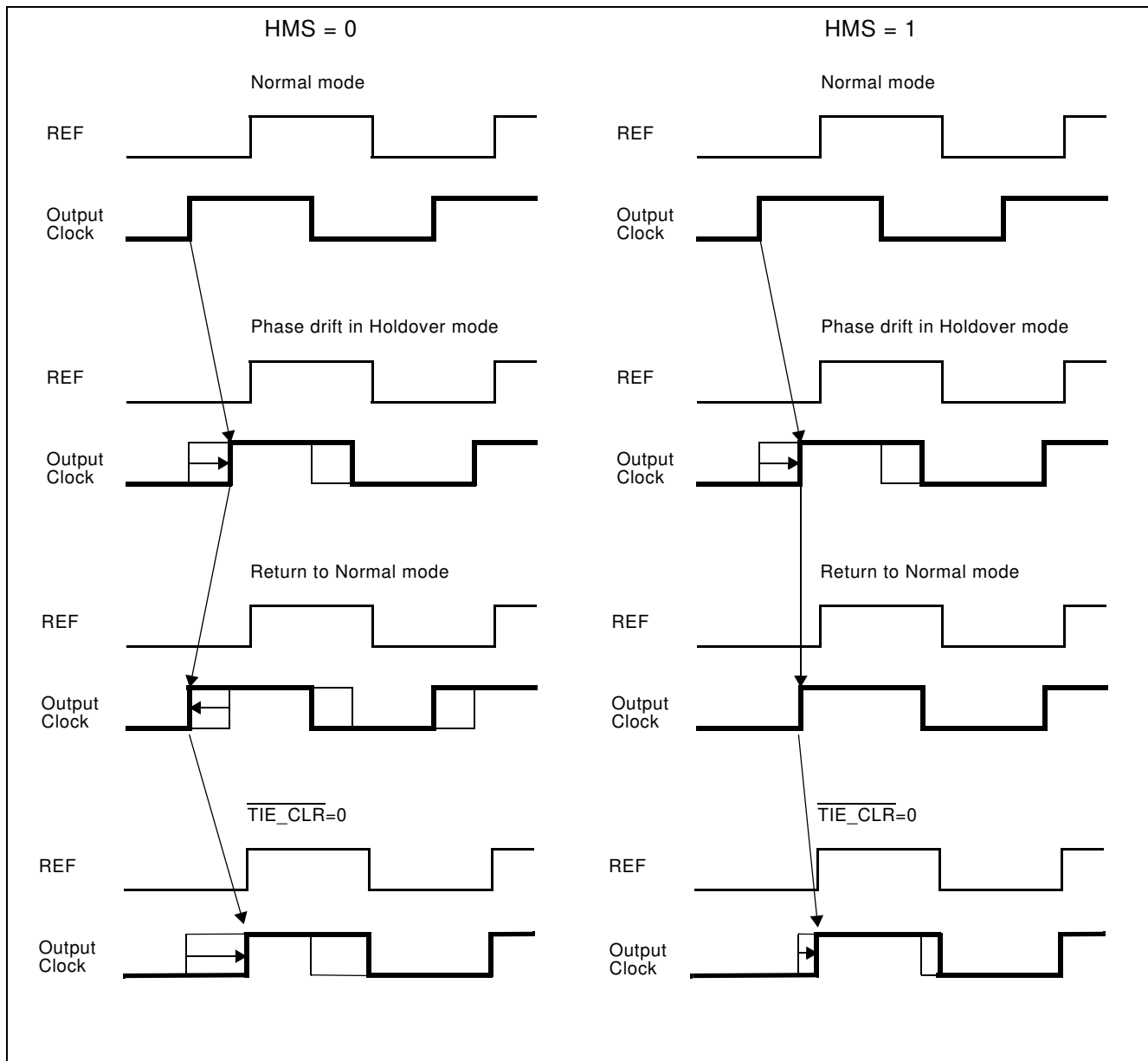
The delay value can be reset by setting the TIE Corrector Circuit Clear pin ( $\overline{\text{TIE\_CLR}}$ ) low for at least 15 ns. This results in a phase alignment between the input reference signal and the output clocks and frame pulses as shown in Figure 24. The speed of the phase alignment correction is limited by the selected loop filter bandwidth and the phase slope limit (see Table 2). Convergence is always in the direction of least phase travel.  $\overline{\text{TIE\_CLR}}$  can be kept low continuously; in that case the output clocks will always align with the selected input reference. This is illustrated in Figure 8.



**Figure 8 - Timing Diagram of Hitless Reference Switching**

The Hitless Mode Switching (HMS) pin enables phase hitless returns from Freerun and Holdover modes to Normal mode in a single reference operation. A logic low at the HMS input disables the TIE circuit updating the delay value thereby forcing the output of the PLL to gradually move back to the original point before it went into Holdover mode. (see Figure 9). This prevents accumulation of phase in network elements. A logic high ( $\text{HMS}=1$ ) enables the TIE circuit to update its delay value thereby preventing a large output phase movement after return to Normal mode. This causes accumulation of phase in network elements. In both cases the PLL's output can be aligned with the input reference by setting  $\overline{\text{TIE\_CLR}}$  low. Regardless of the HMS pin state, reference switching in the ZL30102 is always hitless unless  $\overline{\text{TIE\_CLR}}$  is kept low continuously.





**Figure 9 - Timing Diagram of Hitless Mode Switching**

Examples:

**HMS=1:** When ten Normal to Holdover to Normal mode transitions occur and in each case the Holdover mode was entered for 2 seconds then the accumulated phase change (MTIE) could be as large as 2.13  $\mu$ s.

- $\text{Phase}_{\text{holdover\_drift}} = 0.1 \text{ ppm} \times 2 \text{ s} = 200 \text{ ns}$
- $\text{Phase}_{\text{mode\_change}} = 0 \text{ ns} + 13 \text{ ns} = 13 \text{ ns}$
- $\text{Phase}_{10 \text{ changes}} = 10 \times (200 \text{ ns} + 13 \text{ ns}) = 2.13 \mu\text{s}$

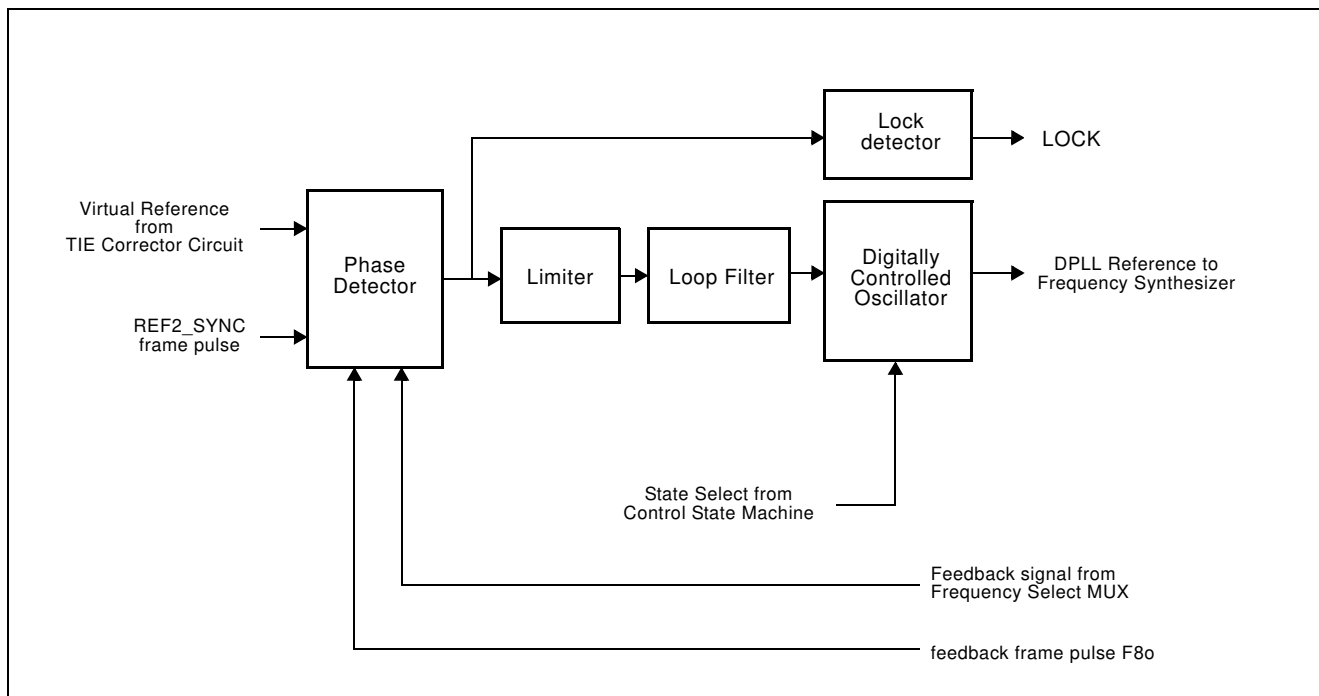
where:

- 0.1 ppm is the accuracy of the Holdover mode
- 0 ns is the maximum phase discontinuity in the transition from the Normal mode to the Holdover mode
- 13 ns is the maximum phase discontinuity in the transition from the Holdover mode to the Normal mode when a new TIE corrector value is calculated

**HMS=0:** When the same ten Normal to Holdover to Normal mode changes occur and in each case Holdover mode was entered for 2 seconds, then the overall MTIE would be 200 ns. As the delay value for the TIE corrector circuit is not updated, there is no 13 ns measurement error at this point. The phase can still drift for 200 ns when the PLL is in Holdover mode but when the PLL enters Normal mode again, the phase moves back to the original point so the phase is not accumulated.

### 3.4 Digital Phase Lock Loop (DPLL)

The DPLL of the ZL30102 consists of a phase detector, a limiter, a loop filter and a digitally controlled oscillator as shown in Figure 10. The data path from the phase detector to the limiter is tapped and routed to the lock detector that provides a lock indication which is output at the LOCK pin.



**Figure 10 - DPLL Block Diagram**

**Phase Detector** - the phase detector compares the virtual reference signal from the TIE corrector circuit with the feedback signal and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the limiter circuit.

**Limiter** - the limiter receives the error signal from the phase detector and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope compliant with the applicable standards. The phase slope limit is dependent on the SEC\_MSTR pin and is listed in Table 2.

**Loop Filter** - the loop filter is similar to a first order low pass filter with a bandwidth of 1.8 Hz suitable to provide Primary Master timing. When Secondary Master mode is selected (SEC\_MSTR=1), the filter bandwidth is set to 922 Hz. For stability reasons, the loop filter bandwidth for 8 kHz reference inputs is limited to a maximum of 58 Hz.

**Digitally Controlled Oscillator (DCO)** - the DCO receives the limited and filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the ZL30102.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Holdover Mode, the DCO is free running at a frequency equal to the frequency that the DCO was generating in Normal Mode. The frequency in Holdover mode is calculated from frequency samples stored 26 ms to 52 ms before the ZL30102 entered Holdover mode. This ensures that the coarse frequency monitor and the single cycle monitor have time to disqualify a bad reference before it corrupts the holdover frequency.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 20 MHz source.

**Lock Indicator** - the lock detector monitors if the output value of the phase detector is within the phase-lock-window for a certain time. The selected phase-lock-window guarantees the stable operation of the LOCK pin with maximum network jitter and wander on the reference input. If the DPLL goes into Holdover mode (auto or manual), the LOCK pin will initially stay high for 1 s in Primary Master mode. In Secondary Master mode, LOCK remains high for 0.1 s. If at that point the DPLL is still in holdover mode, the LOCK pin will go low; subsequently the LOCK pin will not return high for at least the full lock-time duration. In Freerun mode the LOCK pin will go low immediately.

### 3.5 Frequency Synthesizers

The output of the DCO is used by the frequency synthesizers to generate the output clocks and frame pulses which are synchronized to one of three reference inputs (REF0, REF1 or REF2). The frequency synthesizer uses digital techniques to generate output clocks and advanced noise shaping techniques to minimize the output jitter. The clock and frame pulse outputs have limited driving capability and should be buffered when driving high capacitance loads.

### 3.6 State Machine

As shown in Figure 1, the state machine controls the TIE Corrector Circuit and the DPLL. The control of the ZL30102 is based on the inputs MODE\_SEL1:0, REF\_SEL1:0 and HMS.

### 3.7 Master Clock

The ZL30102 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

## 4.0 Control and Modes of Operation

### 4.1 Out of Range Selection

The out of range limits for the Precise Frequency Monitor in the 3 reference monitor blocks are selected through the OOR\_SEL pin, see Table 1.

| OOO_SEL | Application | Applicable Standard                                | Out Of Range Limits |
|---------|-------------|--|---------------------|
| 0       | DS1         | ANSI T1.403<br>Telcordia GR-1244-CORE Stratum 4/4E | 64 - 83 ppm         |
| 1       | E1          | ITU-T G.703<br>ETSI ETS 300 011                    | 100 - 130 ppm       |

**Table 1 - Out of Range Limits Selection**

### 4.2 Loop Filter and Limiter Selection

The loop filter and limiter settings are selected through the SEC\_MSTR pin, see Table 2. The maximum loop filter bandwidth is also dependent on the frequency of the currently selected reference (REF0/1/2).

| SEC_MSTR | Detected REF Frequency                         | Loop Filter Bandwidth | Phase Slope Limiting |
|----------|--|-----------------------|----------------------|
| 0        | any  | 1.8 Hz                | 61 $\mu$ /s          |
| 1        | 8 kHz  | 58 Hz                 | 9.5 ms /s            |
|          | 1.544 MHz, 2.048 MHz,<br>8.192 MHz, 16.384 MHz | 922 Hz                | 9.5 ms /s            |

**Table 2 - Loop Filter and Limiter Settings**

### 4.3 Output Clock and Frame Pulse Selection

The output of the DCO is used by the frequency synthesizers to generate the output clocks and frame pulses which are synchronized to one of three reference inputs (REF0, REF1 or REF2). These signals are available in two groups controlled by the OUT\_SEL pin, see Table 3.

| OUT_SEL | Generated Clocks     | Generated Frame Pulses |
|---------|----------------------|------------------------|
| 0       | C2o, C4o, C8o, C16o  | F4o, F8o, F16o         |
| 1       | C2o, C16o, C32, C65o | F16o, F32o, F65o       |

**Table 3 - Clock and Frame Pulse Selection with OUT\_SEL Pin**

## 4.4 Modes of Operation

The ZL30102 has three possible manual modes of operation; Normal, Holdover and Freerun. These modes are selected with mode select pins MODE\_SEL1 and MODE\_SEL0 as is shown in Table 4. Transitioning from one mode to the other is controlled by an external controller. The ZL30102 can be configured to automatically select a valid input reference under control of its internal state machine by setting MODE\_SEL1:0 = 11. In this mode of operation, a state machine controls selection of references (REF0 or REF1) used for synchronization.

| MODE_SEL1 | MODE_SEL0 | Mode   |
|-----------|-----------|--|
| 0         | 0         | Normal (with automatic Holdover)   |
| 0         | 1         | Holdover   |
| 1         | 0         | Freerun  |
| 1         | 1         | Automatic<br>(Normal with automatic Holdover and<br>automatic reference switching) |

**Table 4 - Operating Modes**

### 4.4.1 Freerun Mode

Freerun mode is typically used when an independent clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun mode, the ZL30102 provides timing and synchronization signals which are based on the master clock frequency (supplied to OSCi pin) only, and are not synchronized to the reference input signals.

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a  $\pm 32$  ppm output clock is required, the master clock must also be  $\pm 32$  ppm. See Applications - Section 6.2, "Master Clock".

### 4.4.2 Holdover Mode

Holdover Mode is typically used for short durations while network synchronization is temporarily disrupted.

In Holdover Mode, the ZL30102 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal.

When in Normal Mode, and locked to the input reference signal, a numerical value corresponding to the ZL30102 output reference frequency is stored alternately in two memory locations every 26 ms. When the device is switched into Holdover Mode, the value in memory from between 26 ms and 52 ms is used to set the output frequency of the device. The frequency accuracy of Holdover Mode is 0.1 ppm.

Two factors affect the accuracy of Holdover mode. One is drift on the master clock while in Holdover mode, drift on the master clock directly affects the Holdover mode accuracy. Note that the absolute master clock (OSCi) accuracy does not affect Holdover accuracy, only the *change* in OSCi accuracy while in Holdover. For example, a  $\pm 32$  ppm master clock may have a temperature coefficient of  $\pm 0.1$  ppm per °C. So a  $\pm 10$  °C change in temperature, while the ZL30102 is in Holdover mode may result in an additional offset (over the 0.1 ppm) in frequency accuracy of  $\pm 1$  ppm. Which is much greater than the 0.1 ppm of the ZL30102. The other factor affecting the accuracy is large jitter on the reference input prior to the mode switch.

### 4.4.3 Normal Mode

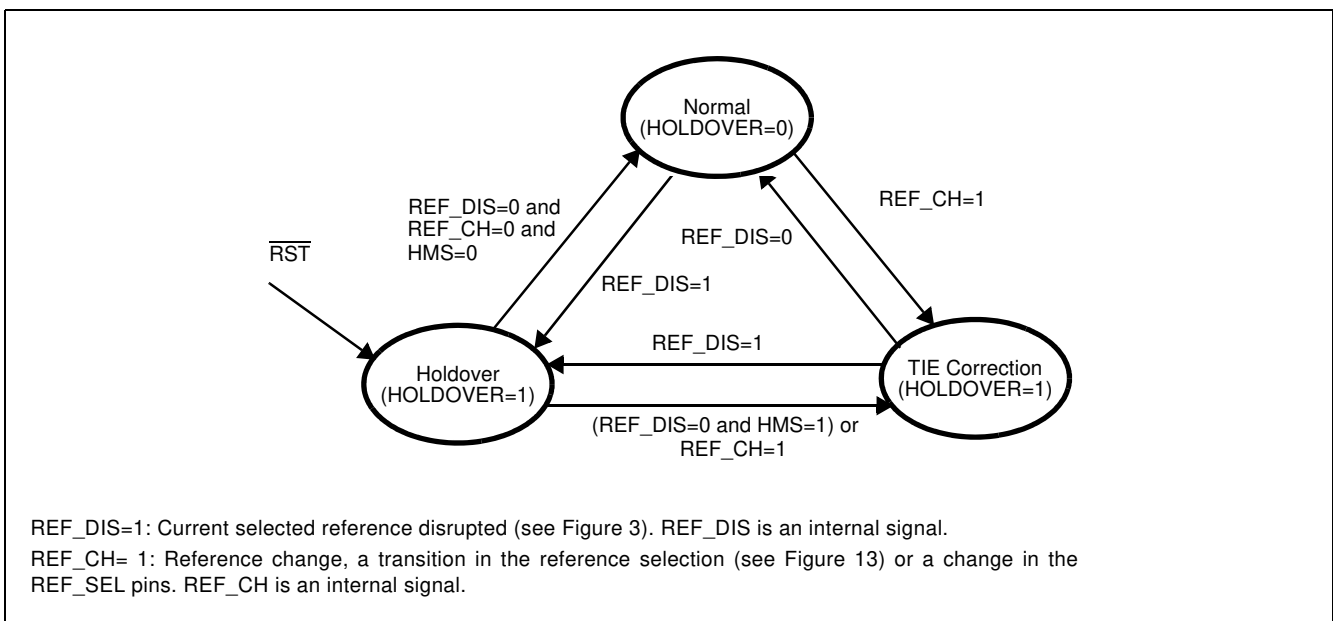
Normal mode is typically used when a system clock source, synchronized to the network is required. In Normal mode, the ZL30102 provides timing and frame synchronization signals, which are synchronized to one of three reference inputs (REF0, REF1 or REF2). The input reference signal may have a nominal frequency of 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz or 16.384 MHz. The frequency of the reference inputs are automatically detected by the reference monitors.

When the ZL30102 comes out of RESET while Normal mode is selected by its MODE\_SEL pins then it will initially go into Holdover mode and generate clocks with the accuracy of its freerunning local oscillator (see Figure 11). If the ZL30102 determines that its selected reference is disrupted (see Figure 3), it will remain in Holdover until the selected reference is no longer disrupted or the external controller selects another reference that is not disrupted. If the ZL30102 determines that its selected reference is not disrupted (see Figure 3) then the state machine will cause the DPLL to recover from Holdover via one of two paths depending on the logic level at the HMS pin. If HMS=0 then the ZL30102 will transition directly to Normal mode and it will align its output signals with its selected input reference (see Figure 9). If HMS=1 then the ZL30102 will transition to Normal mode via the TIE correction state and the phase difference between the output signals and the selected input reference will be maintained.

When the ZL30102 is operating in Normal mode, if it determines that its selected reference is disrupted (Figure 3) then its state machine will cause it to automatically go to Holdover mode. When the ZL30102 determines that its selected reference is not disrupted then the state machine will cause the DPLL to recover from Holdover via one of two paths depending on the logic level at the HMS pin (see Figure 11). If HMS=0 then the ZL30102 will transition directly to Normal mode and it will align its output signals with its input reference (see Figure 9). If HMS=1 then the ZL30102 will transition to Normal mode via the TIE correction state and the phase difference between the output signals and the input reference will be maintained.

If the reference selection changes because the value of the REF\_SEL1:0 pins changes or because the reference selection state machine selected a different reference input, the ZL30102 goes into Holdover mode and returns to Normal mode through the TIE correction state regardless of the logic value on HMS pin.

ZL30102 provides a fast lock pin (FASTLOCK), which, when set high enables the PLL to lock to an incoming reference within approximately 1 s.



**Figure 11 - Mode Switching in Normal Mode**

#### 4.4.4 Automatic Mode

The Automatic mode combines the functionality of the Normal mode (automatic Holdover) with automatic reference switching. The automatic reference switching is described in more detail in section 4.5.2, “Automatic Reference Switching”.

### 4.5 Reference Switching

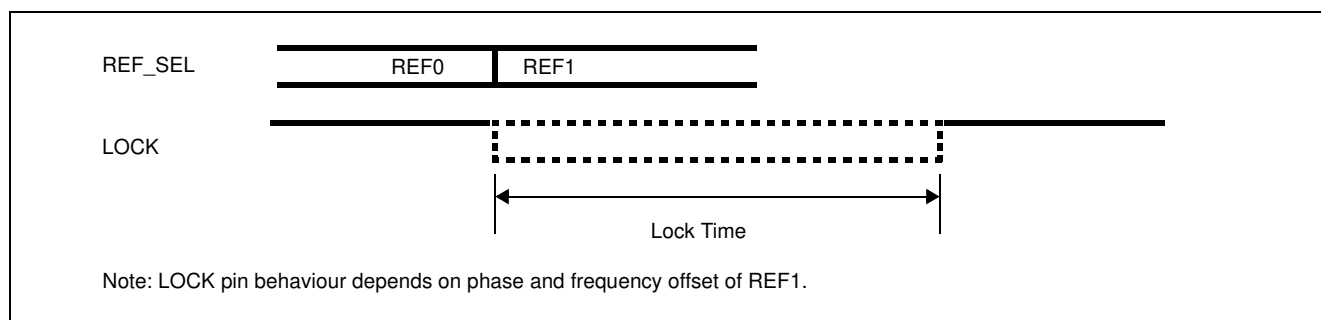
#### 4.5.1 Manual Reference Switching

In the manual modes of operation ( $\text{MODE\_SEL1:0} \neq 11$ ) the active reference input (REF0, REF1 or REF2) is selected by the REF\_SEL1 and REF\_SEL0 pins as shown in Table 5. When the logic value of the REF\_SEL pins is changed when the DPLL is in Normal mode, the ZL30102 will perform a hitless reference switch.

| REF_SEL1 | REF_SEL0 | Input Reference Selected |
|----------|----------|--------------------------|
| 0        | 0        | REF0                     |
| 0        | 1        | REF1                     |
| 1        | 0        | REF2                     |
| 1        | 1        | REF2                     |

**Table 5 - Manual Reference Selection**

When the REF\_SEL inputs are used in Normal mode to force a change from the currently selected reference to another reference, the action of the LOCK output will depend on the relative frequency and phase offset of the old and new references. Where the new reference has enough frequency offset and/or TIE-corrected phase offset to force the output outside the phase-lock-window, the LOCK output will de-assert, the lock-qualify timer is reset, and LOCK will stay de-asserted for the full lock-time duration. Where the new reference is close enough in frequency and TIE-corrected phase for the output to stay within the phase-lock-window, the LOCK output will remain asserted through the reference-switch process.

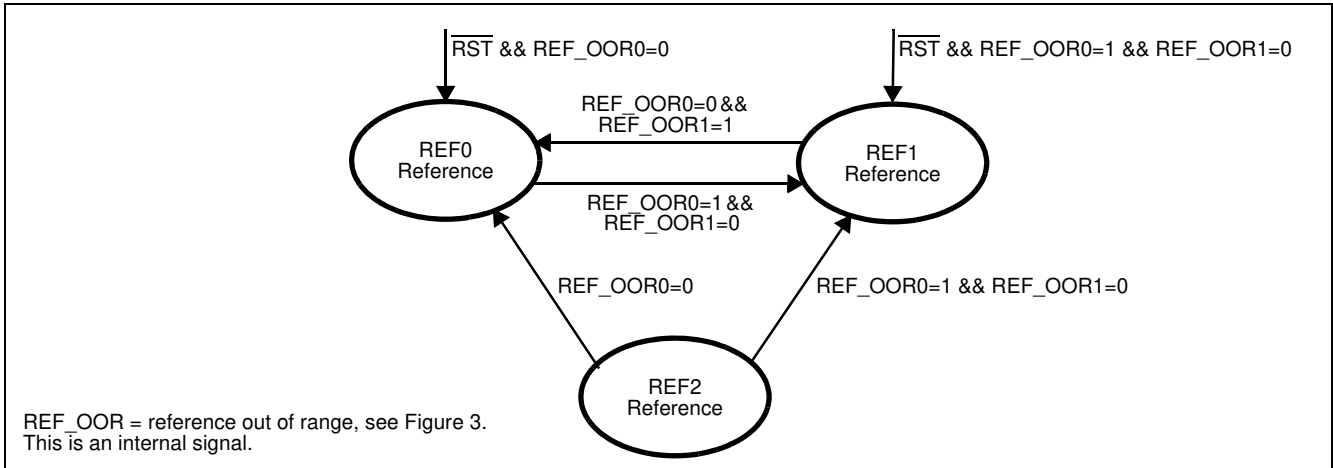


**Figure 12 - Reference Switching in Normal Mode**

### 4.5.2 Automatic Reference Switching

In the automatic mode of operation (MODE\_SEL1:0 = 11), the ZL30102 automatically selects a reference input that is not out-of-range (REF\_OOR=0, see Figure 3). The state machine can only select REF0 or REF1; REF2 cannot be selected in the Automatic mode (see Figure 13).

If the current reference (REF0 or REF1) used for synchronization fails, the state machine will switch to the other reference. If both references fail then the ZL30102 enters the Holdover mode without switching to another reference. When the ZL30102 comes out of reset or when REF2 is the current reference when the ZL30102 is put in the Automatic mode, then REF0 has priority over REF1. Otherwise there is no preference for REF0 or REF1 which is referred to as non-revertive reference selection.



**Figure 13 - Reference Selection in Automatic Mode (MODE\_SEL=11)**

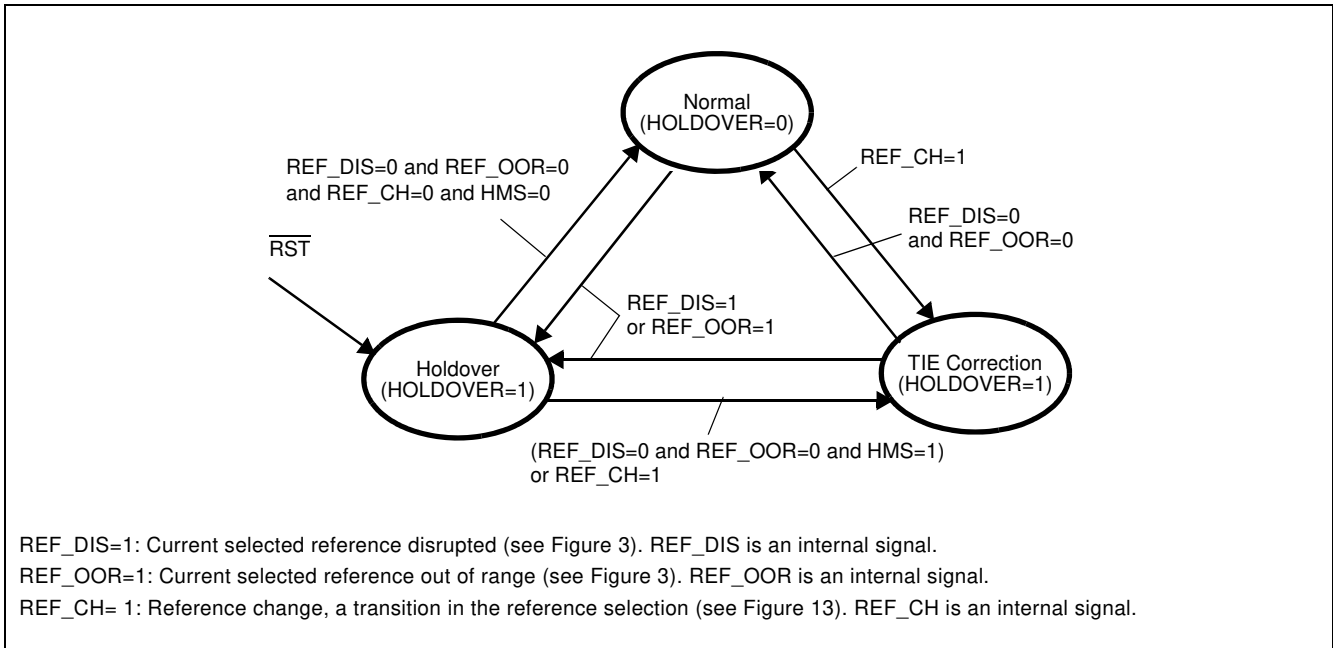
In the automatic mode of operation, both pins REF\_SEL1 and REF\_SEL0 are configured as outputs. The logic level on the REF\_SEL0 output indicates the current input reference being selected for synchronization (see Table 6).

| REF_SEL1<br>(output pin) | REF_SEL0<br>(output pin) | Input Reference |
|--------------------------|--------------------------|-----------------|
| 0                        | 0                        | REF0            |
| 0                        | 1                        | REF1            |

**Table 6 - The Reference Selection Pins in the Automatic Mode (MODE\_SEL=11)**



The mode selection state machine behaves differently in Automatic mode in that when both reference REF0 and reference REF1 are out of range (REF\_OOR=1), the state machine will select the Holdover state. In Normal mode the reference out of range (REF\_OOR) status is ignored by the state machine. This is illustrated in Figure 14.



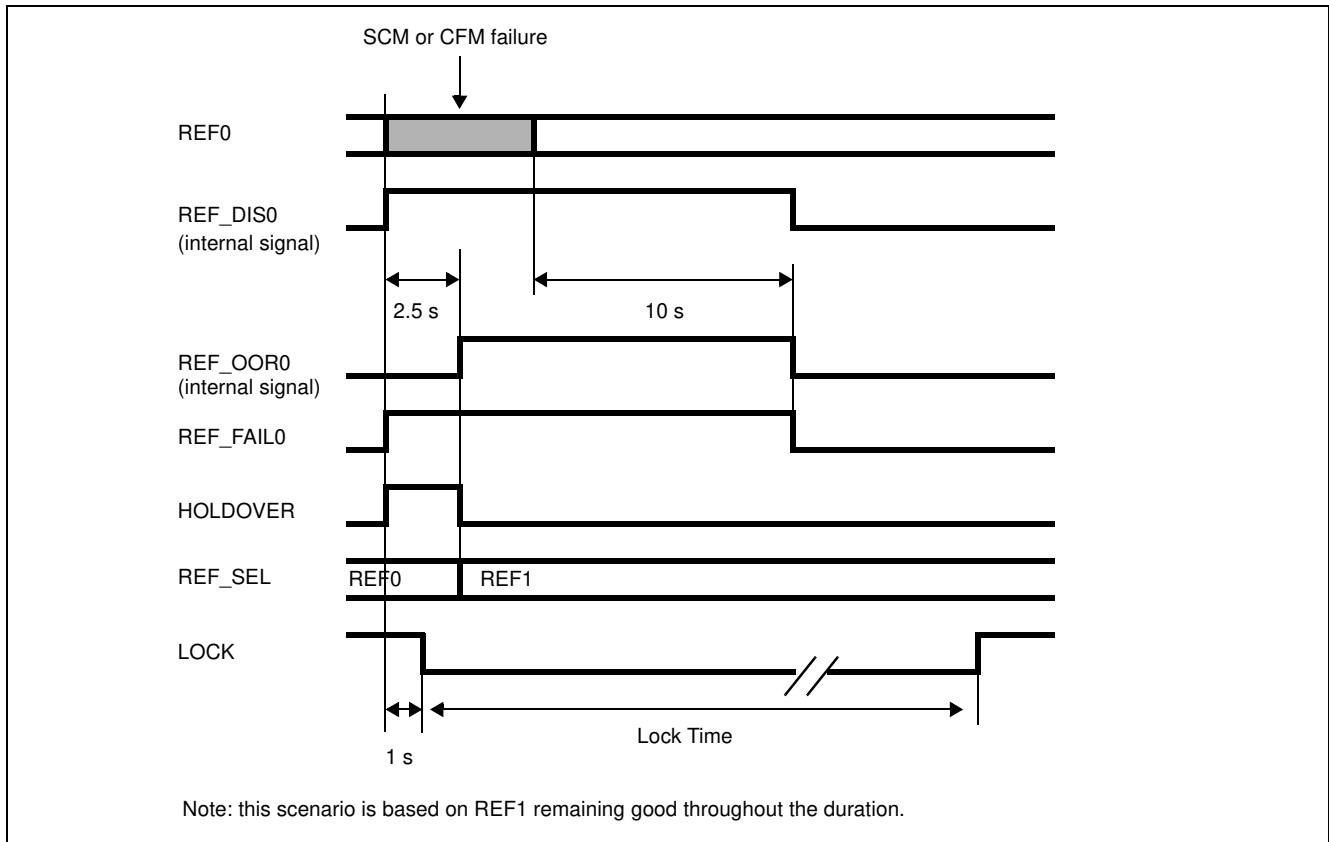
**Figure 14 - Mode Switching in Automatic Mode**

#### 4.5.2.1 Automatic Reference Switching - Coarse Reference Failure

When the currently-active input reference in Automatic mode fails in a coarse manner, the REF\_DIS internal signal places the device in holdover, with the HOLDOVER pin and the REF\_FAIL pin asserted. This can occur through triggering the Single Cycle Monitor, or the Coarse Frequency Monitor, in the Reference Monitor block. If the reference does not correct itself within the lock-disqualify duration (1 second) the LOCK pin is de-asserted. If the reference does not correct itself within the reference-disqualify duration (2.5 seconds) the HOLDOVER pin is de-asserted and the REF\_SEL outputs indicate that the device has switched to the other reference. The LOCK pin remains de-asserted for the full lock-time duration, regardless of the phase and frequency offset of the old and new references. Figure 15 illustrates this process.

If the reference corrects itself within the lock-disqualify duration (< 1 second) the HOLDOVER pin is de-asserted, and the REF\_FAIL pin is de-asserted. The LOCK pin remains asserted. No reference switching takes place, and the REF\_SEL outputs indicate that the device has remained locked to the old reference.

If the reference does not correct itself within the lock-disqualify duration (1 second), but does correct itself within the reference-disqualify duration (< 2.5 seconds) the HOLDOVER pin is de-asserted, the REF\_FAIL pin is de-asserted, and the REF\_SEL outputs indicate that the device has remained locked to the old reference. However the LOCK pin is de-asserted, the lock-qualify timer is reset, and the LOCK pin remains de-asserted for the full lock-time duration. See 7.2, "Performance Characteristics" on page 44 for lock-time duration.



**Figure 15 - Automatic Reference Switching - Coarse Reference Failure**

**4.5.2.2 Automatic Reference Switching - Reference Frequency Out-of-Range**

When the currently-active input reference in Automatic mode fails through a subtle frequency offset, the REF\_FAIL output is asserted as soon as the Precise Frequency Monitor indicates an out-of-range reference (10 to 20 seconds). The HOLDOVER output is briefly asserted (approximately three reference input cycles) and the REF\_SEL outputs indicate that the device has switched to the other reference. Where the new reference is close enough in frequency and TIE-corrected phase for the output to stay within the phase-lock-window, the LOCK output will remain asserted through the reference-switch process. Where the new reference has enough frequency offset and/or TIE-corrected phase offset to force the output outside the phase-lock-window, the LOCK output will deassert, the lock-qualify timer is reset, and LOCK will stay deasserted for the full lock-time duration. Figure 16 illustrates this process.