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ZL30105

T1/E1/SDH Stratum 3 Redundant System Clock Synchronizer for AdvancedTCA™ and H.110

Data Sheet

Features

April 2010

- Synchronizes to clock-and-sync-pair to maintain minimal phase skew between the master-clock and the redundant slave-clock
- Supports ITU-T G.813 option 1, G.823 for 2048 kbit/s and G.824 for 1544 kbit/s interfaces
- Supports Telcordia GR-1244-CORE Stratum 3/4/4E
- Supports ANSI T1.403 and ETSI ETS 300 011 for ISDN primary rate interfaces
- Accepts three input references and synchronizes to any combination of 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz inputs
- Provides a range of clock outputs: 1.544 MHz (DS1), 2.048 MHz (E1), 3.088 MHz, 16.384 MHz, and 19.44 MHz (SDH), and either 4.096 MHz and 8.192 MHz or 32.768 MHz and 65.536 MHz, and a choice of 6.312 MHz (DS2), 8.448 MHz (E2), 44.736 MHz (DS3) or 34.368 MHz (E3)
- Provides 5 styles of 8 kHz framing pulses and a 2 kHz multi-frame pulse
- Holdover frequency accuracy of $1x10^{-8}$
- Selectable loop filter 1.8 Hz, 3.6 Hz or 922 Hz
- Less than 24 ps_{rms} intrinsic jitter on the 19.44 MHz output clock, compliant with GR-253-CORE OC-3 and G.813 STM-1 specifications

Ordering Information		
ZL30105QDG1	64 pin TQFP*	Trays Bake & Drypack
	* Pb Free Matte Tin	
	-40°C to +85°C	

- Less than 0.6 ns_{pp} intrinsic jitter on all output clocks and frame pulses
- Manual or Automatic hitless reference switching between any combination of valid input reference frequencies
- Provides Lock, Holdover and selectable Out of Range indication
- Simple hardware control interface
- Selectable external master clock source: Clock Oscillator or Crystal

Applications

- Synchronization and timing control for multi-trunk SDH and T1/E1 systems such as DSLAMs, Gateways and PBXs
- Clock and frame pulse source for AdvancedTCA™- and other time division multiplex (TDM) buses

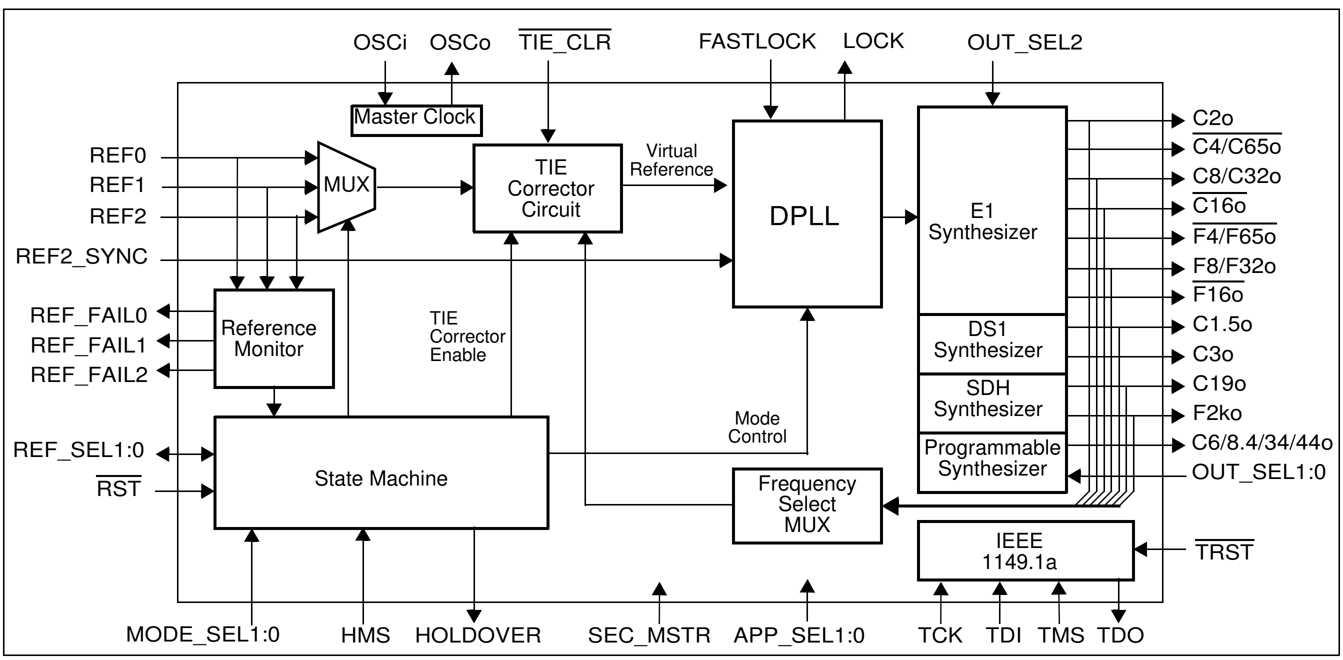

Figure 1 - Functional Block Diagram

Description

The ZL30105 SDH/PDH System Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization for SDH and T1/E1 transmission equipment. It provides advanced support for systems deploying redundant clocks.

The ZL30105 generates SBI, ST-BUS and other TDM clock and framing signals that are phase locked to one of three network references or to a system master-clock reference. It helps ensure system reliability by monitoring its references for frequency accuracy and stability and by maintaining tight phase alignment between the master-clock and slave-clock outputs even in the presence of high network jitter.

The ZL30105 is intended to be the central timing and synchronization resource for network equipment that complies with ITU-T, Telcordia, ETSI and ANSI network specifications.

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1.0 Change Summary

Changes from November 2005 Issue to April 2010 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Ordering Information Box	Leaded part number ZL30105QDG has been obsoleted and replaced by ZL30105QDG1.

Changes from July 2005 Issue to November 2005 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Features	Changed description for hitless reference switching.
33	Section 6.1	Removed power supply decoupling circuit and included reference to synchronizer power supply decoupling application note.

Changes from October 2004 Issue to July 2005 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
9	$\overline{\text{RST}}$ pin	Specified clock and frame pulse outputs forced to high impedance
38	Table “DC Electrical Characteristics*“	Corrected Schmitt trigger levels

Changes from June 2004 Issue to October 2004 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Text	Jitter changed to 24 ps from 20 ps
7	Figure 2	Added note specifying not e-Pad
35	Section 6.4	Corrected time-constant of example reset circuit
38	Table “Absolute Maximum Ratings*“	Corrected package power rating
38	Table “DC Electrical Characteristics*“	Corrected current consumption Corrected Schmitt trigger V_{t-} levels Corrected output voltage note to reflect two pad strengths
38	Section 7.1	Pulse widths corrected.
41	Table “AC Electrical Characteristics* - Input to output timing for REF0, REF1 and REF2 references when TIE_CLR = 0 (see Figure 26).“	Updated Min. Max. values.
48 - 50	Section 7.2	Changed jitter numbers

2.0 Physical Description

2.1 Pin Connections

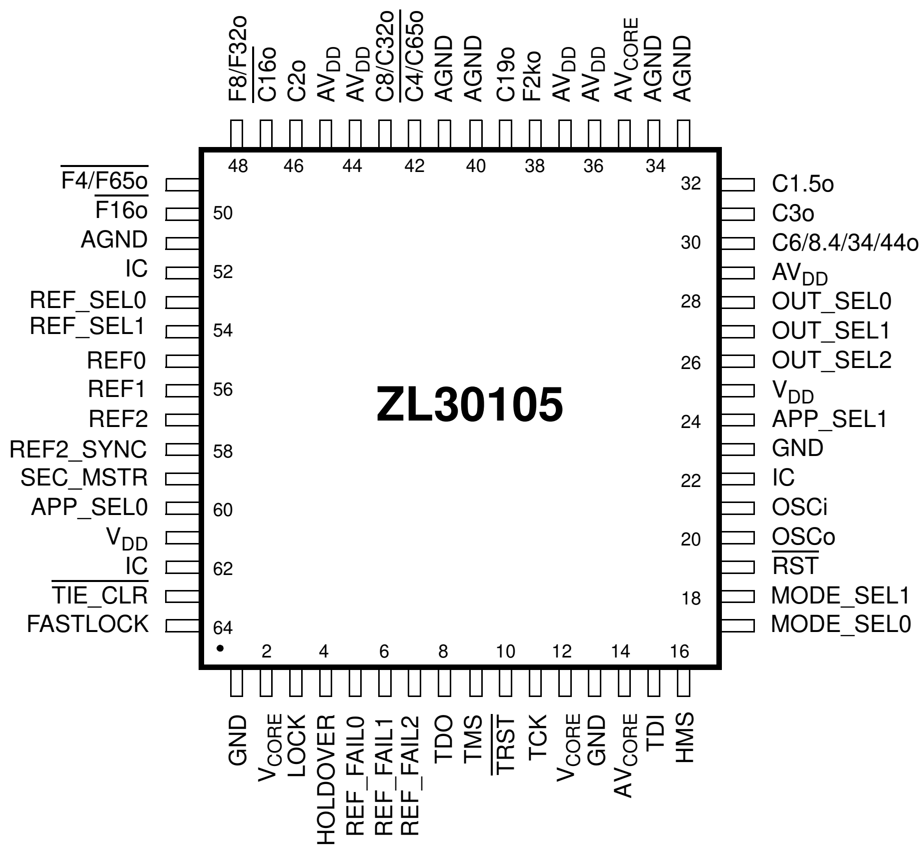


Figure 2 - Pin Connections (64 pin TQFP, please see Note 1)

Note 1: The ZL30105 uses the TQFP shown in the package outline designated with the suffix QD, the ZL30105 does not use the e-Pad TQFP.

2.2 Pin Description

Pin #	Name	Description
1	GND	**Ground.** 0 V
2	V_{CORE}	**Positive Supply Voltage.** +1.8 V_{DC} nominal
3	LOCK	**Lock Indicator (Output).** This output goes to a logic high when the PLL is frequency locked to the selected input reference.
4	HOLDOVER	**Holdover (Output).** This output goes to a logic high whenever the PLL goes into holdover mode.
5	REF_FAIL0	**Reference 0 Failure Indicator (Output).** A logic high at this pin indicates that the REF0 reference frequency has exceeded the out-of-range limit set by the APP_SEL pins or that it is exhibiting abrupt phase or frequency changes.
6	REF_FAIL1	**Reference 1 Failure Indicator (Output).** A logic high at this pin indicates that the REF1 reference frequency has exceeded the out-of-range limit set by the APP_SEL pins or that it is exhibiting abrupt phase or frequency changes.
7	REF_FAIL2	**Reference 2 Failure Indicator (Output).** A logic high at this pin indicates that the REF2 reference frequency has exceeded the out-of-range limit set by the APP_SEL pins or that it is exhibiting abrupt phase or frequency changes.
8	TDO	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
9	TMS	**Test Mode Select (Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
10	$\overline{TRST}$	**Test Reset (Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
11	TCK	**Test Clock (Input):** Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.
12	V_{CORE}	**Positive Supply Voltage.** +1.8 V_{DC} nominal
13	GND	**Ground.** 0 V
14	AV_{CORE}	**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal
15	TDI	**Test Serial Data In (Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
16	HMS	**Hitless Mode Switching (Input).** The HMS input controls phase accumulation during the transition from Holdover or Freerun mode to Normal mode on the same reference. A logic low at this pin will cause the ZL30105 to maintain the delay stored in the TIE corrector circuit when it transitions from Holdover or Freerun mode to Normal mode. A logic high on this pin will cause the ZL30105 to measure a new delay for its TIE corrector circuit thereby minimizing the output phase movement when it transitions from Holdover or Freerun mode to Normal mode.
17	MODE_SEL0	**Mode Select 0 (Input).** This input combined with MODE_SEL1 determines the mode of operation, see Table 4 on page 21.
18	MODE_SEL1	**Mode Select 1 (Input).** See MODE_SEL0 pin description.

Pin #	Name	Description
19	$\overline{RST}$	**Reset (Input).** A logic low at this input resets the device. On power up, the $\overline{RST}$ pin must be held low for a minimum of 300 ns after the power supply pins have reached the minimum supply voltage. When the RST pin goes high, the device will transition into a Reset state for 3 ms. In the Reset state all clock and frame pulse outputs will be forced into high impedance.
20	OSCo	**Oscillator Master Clock (Output).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCi. This output is not suitable for driving other devices. For clock oscillator operation, this pin must be left unconnected.
21	OSCi	**Oscillator Master Clock (Input).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCo. For clock oscillator operation, this pin must be connected to a clock source.
22	IC	**Internal Connection.** Leave unconnected.
23	GND	**Ground.** 0 V
24	APP_SEL1	**Application Selection 1 (Input).** This input combined with APP_SEL0 selects the application that the ZL30105 is optimized for, see Table 1 on page 20.
25	V_{DD}	**Positive Supply Voltage.** +3.3 V_{DC} nominal
26	OUT_SEL2	**Output Selection 2 (Input).** This input selects the signals on the combined output clock and frame pulse pins, see Table 3 on page 21.
27	OUT_SEL1	**Output Selection 1 (Input).** This input combined with OUT_SEL0 selects the signals on the combined output clock pin C6/8.4/34/44o, see Table 3 on page 21.
28	OUT_SEL0	**Output Selection 0 (Input).** See OUT_SEL1 description.
29	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal
30	C6/8.4/34/44o	**Clock 6.312 MHz, 8.448 MHz, 34.368 MHz or 44.736 MHz (Output).** This output is used in DS2, E2, E3 or DS3 applications. The output frequency is selected via the OUT_SEL1 and OUT_SEL0 pins, see Table 3 on page 21.
31	C3o	**Clock 3.088 MHz (Output).** This output is used in DS1 applications.
32	C1.5o	**Clock 1.544 MHz (Output).** This output is used in DS1 applications. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
33	AGND	**Analog Ground.** 0 V
34	AGND	**Analog Ground.** 0 V
35	AV_{CORE}	**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal
36	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal
37	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal
38	F2ko	**Multi Frame Pulse (Output).** This is a 2 kHz 51 ns active high framing pulse, which marks the beginning of a multi frame.
39	C19o	**Clock 19.44 MHz (Output).** This output is used in SDH applications.
40	AGND	**Analog Ground.** 0 V
41	AGND	**Analog Ground.** 0 V

Pin #	Name	Description
42	$\overline{C4}/\overline{C65}$o	**Clock 4.096 MHz or 65.536 MHz (Output).** This output is used for ST-BUS operation at 2.048 Mbit/s, 4.096 Mbit/s or 65.536 MHz (ST-BUS 65.536 Mbit/s). The output frequency is selected via the OUT_SEL2 pin, see Table 3 on page 21.
43	C8/C32o	**Clock 8.192 MHz or 32.768 MHz (Output).** This output is used for ST-BUS and GCI operation at 8.192 Mb/s or for operation with a 32.768 MHz clock. The output frequency is selected via the OUT_SEL2 pin, see Table 3 on page 21. In C8 mode, this clock output pad uses an included Schmitt input as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
44	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal
45	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal
46	C2o	**Clock 2.048 MHz (Output).** This output is used for standard E1 interface timing and for ST-BUS operation at 2.048 Mbit/s. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
47	$\overline{C16}$o	**Clock 16.384 MHz (Output).** This output is used for ST-BUS operation with a 16.384 MHz clock. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
48	F8/F32o	**Frame Pulse (Output).** This is an 8 kHz 122 ns active high framing pulse or it is an 8 kHz 31 ns active high framing pulse, which marks the beginning of a frame. The pulse width is selected via the OUT_SEL2 pin, see Table 3 on page 21.
49	$\overline{F4}/\overline{F65}$o	**Frame Pulse ST-BUS 2.048 Mbit/s or ST-BUS at 65.536 MHz clock (Output).** This output is an 8 kHz 244 ns active low framing pulse which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mbit/s and 4.096 Mbit/s. Or this output is an 8 kHz 15 ns active low framing pulse, typically used for ST-BUS operation with a clock rate of 65.536 MHz. The pulse width is selected via the OUT_SEL2 pin, see Table 3 on page 21.
50	$\overline{F16}$o	**Frame Pulse ST-BUS 8.192 Mbit/s (Output).** This is an 8 kHz 61 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mbit/s.
51	AGND	**Analog Ground.** 0 V
52	IC	**Internal Connection.** Connect this pin to ground.
53	REF_SEL0	**Reference Select 0 (Input/Output).** In the manual mode of operation, REF_SEL0 is an input. As an input REF_SEL0 combined with REF_SEL1 selects the reference input that is used for synchronization, see Table 6 on page 24. In the Automatic mode of operation, REFSEL0 is an output indicating which of the input references is the being selected. This pin is internally pulled down to GND.
54	REF_SEL1	**Reference Select 1 (Input/Output)**. See REF_SEL0 pin description.
55	REF0	**Reference (Input).** This is one of three (REF0, REF1 and REF2) input reference sources used for synchronization. One of seven possible frequencies may be used: 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz. This pin is internally pulled down to GND.

Pin #	Name	Description
56	REF1	**Reference (Input).** See REF0 pin description.
57	REF2	**Reference (Input).** See REF0 pin description.
58	REF2_SYNC	**REF2 Synchronization Frame Pulse (Input).** This is the 2 kHz or 8 kHz (multi) frame pulse synchronization input associated with the REF2 reference. While the PLL is locked to the REF2 input reference the output (multi) frame pulses are synchronized to this input. This pin is internally pulled down to GND.
59	SEC_MSTR	**Secondary Master Mode Selection (Input).** A logic low at this pin selects the Primary Master mode of operation with 1.8 Hz or 3.6 Hz DPLL loop filter bandwidth. A logic high selects Secondary Master mode which forces the PLL to clear its TIE corrector circuit and lock to the selected reference using a high bandwidth loop filter and a phase slope limiting of 9.5 ms/s.
60	APP_SEL0	**Application Selection (Input).** See APP_SEL1 pin description.
61	V_{DD}	**Positive Supply Voltage.** +3.3 V_{DC} nominal
62	IC	**Internal Connection.** Connect to GND.
63	$\overline{\text{TIE\_CLR}}$	**TIE Circuit Reset (Input).** A logic low at this input resets the Time Interval Error (TIE) correction circuit resulting in a realignment of input phase with output phase.
64	FASTLOCK	**Fast Lock (Input).** Set temporarily high to allow the ZL30105 to quickly lock to the input reference (one second locking time).

3.0 Functional Description

The ZL30105 is an SDH/PDH Synchronizer for Redundant System Clocks, providing timing and synchronization signals to interface circuits for the following types of primary rate digital transmission links, see Table 1:

- DS1 compliant with ANSI T1.403 and Telcordia GR-1244-CORE Stratum 4/4E
- E1 compliant with ITU-T G.703 and ETSI ETS 300 011
- PDH compliant with Telcordia GR-1244-CORE Stratum 3
- SDH compliant with ITU-T G.813 option 1 and Telcordia GR-253-CORE

Figure 1 is a functional block diagram of the ZL30105 which is described in the following sections.

3.1 Reference Select Multiplexer (MUX)

The ZL30105 accepts three simultaneous reference input signals and operates on their rising edges. One of them, the primary reference (REF0), the secondary reference (REF1) or the tertiary reference (REF2) signal is selected as input to the TIE Corrector Circuit based on the Reference Selection (REF_SEL1:0) inputs.

The use of the combined REF2 and REF2_SYNC inputs allows for a very accurate phase alignment of the output frame pulses to the 2 kHz or 8 kHz (multi) frame pulse supplied to the REF2_SYNC input. This feature supports the implementation of Primary and Secondary Master system clocks in AdvancedTCA or H.110 systems.

3.2 Reference Monitor

The input references are monitored by three independent reference monitor blocks, one for each reference. The block diagram of a single reference monitor is shown in Figure 3. For each reference clock, the frequency is detected and the clock is continuously monitored for three independent criteria that indicate abnormal behavior of the reference signal, for example; long term drift from its nominal frequency or excessive jitter. To ensure proper operation of the reference monitor circuit, the minimum input pulse width restriction of 15 nsec must be observed.

- **Reference Frequency Detector (RFD)**: This detector determines whether the frequency of the reference clock is 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz 8.192 MHz, 16.384 MHz or 19.44 MHz and provides this information to the various monitor circuits and the phase detector circuit of the DPLL.
- **Precise Frequency Monitor (PFM)**: This circuit determines whether the frequency of the reference clock is within the selected accuracy range, see Table 1.
- **Coarse Frequency Monitor (CFM)**: This circuit monitors the reference frequency over intervals of approximately 30 µs to quickly detect large frequency changes.
- **Single Cycle Monitor (SCM)**: This detector checks the period of a single clock cycle to detect large phase hits or the complete loss of the clock.

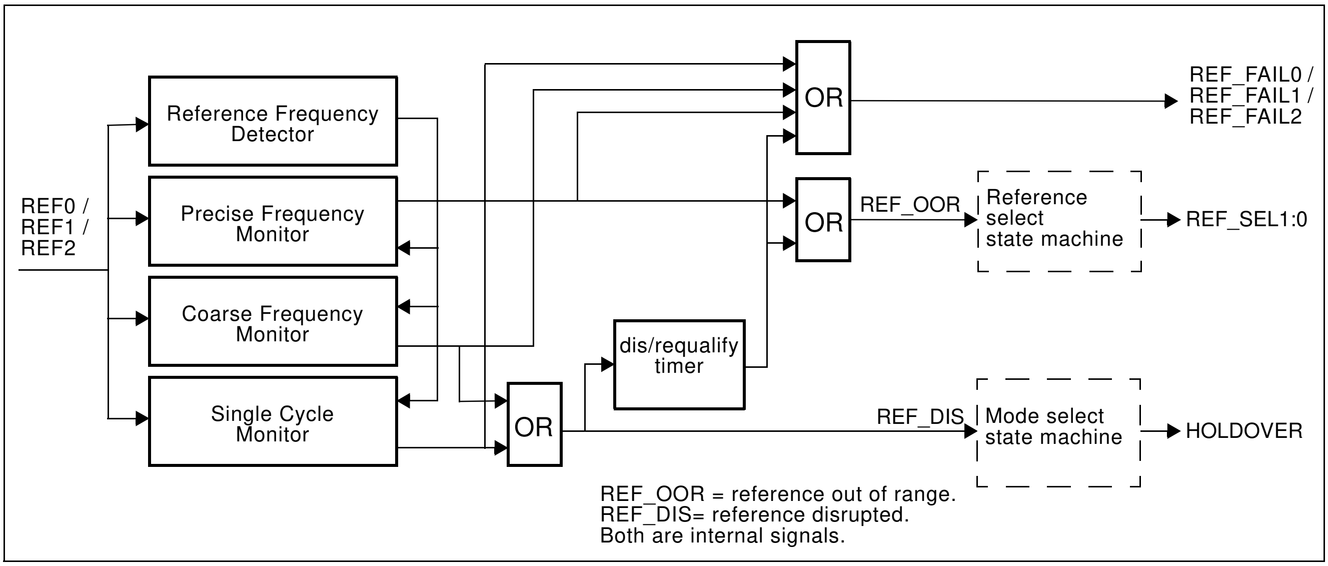


Figure 3 - Reference Monitor Circuit

Exceeding the thresholds of any of the monitors forces the corresponding REF_FAIL pin to go high. The single cycle and coarse frequency failure flags force the DPLL into Holdover mode and feed a timer that disqualifies the reference input signal when the failures are present for more than 2.5 s. The single cycle and coarse frequency failures must be absent for 10 s to let the timer re-qualify the input reference signal as valid. Multiple failures of less than 2.5 s each have an accumulative effect and will disqualify the reference eventually. This is illustrated in Figure 4 where REF0 experiences disruptions while REF1 is stable.

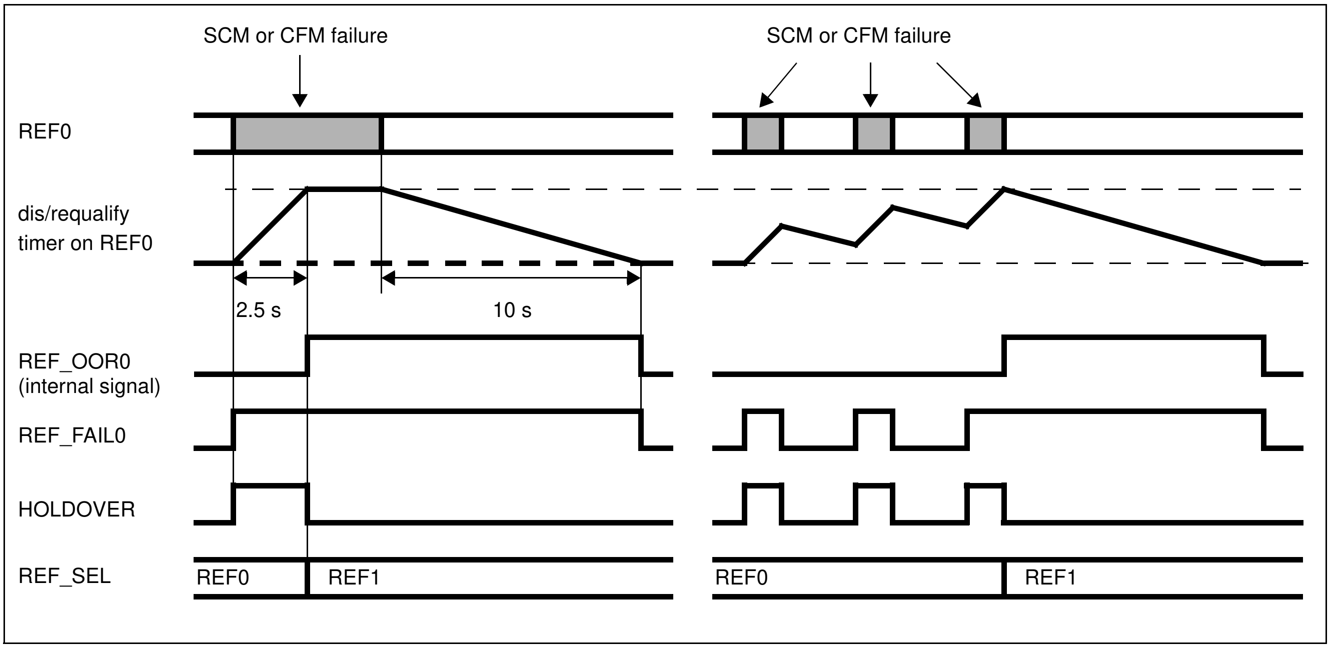


Figure 4 - Behaviour of the Dis/Re-qualify Timer

When the incoming signal returns to normal (REF_FAIL=0), the DPLL returns to Normal mode with the output signal locked to the input signal. Each of the monitors has a built-in hysteresis to prevent flickering of the REF_FAIL status pin at the threshold boundaries. The precise frequency monitor and the timer do not affect the mode (Holdover/Normal) of the DPLL.

If the device is set to Automatic mode (MODE_SEL1:0=11), then the state machine does not immediately switch to another reference. If the single cycle and/or coarse frequency failures persist for more than 2.5 s or the precise frequency monitor detects a failure, then the state machine will switch to another valid reference if that is available. If there no other reference available, it stays in Holdover mode.

The precise frequency monitor's failure thresholds are selected with the APP_SEL pins based on the ZL30105 applications, see Table 1. Figure 5, Figure 6 and Figure 7 show the out of range limits for various master clock accuracies. It will take the precise frequency monitor up to 10 s to qualify or disqualify the input reference.

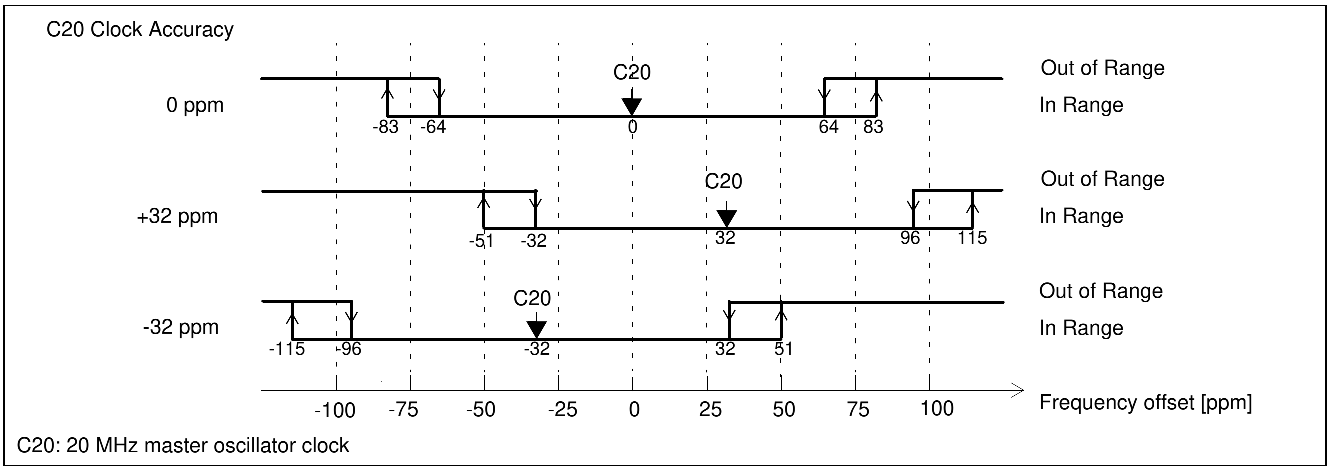


Figure 5 - DS1 Out-of-Range Thresholds for APP_SEL1:0=00

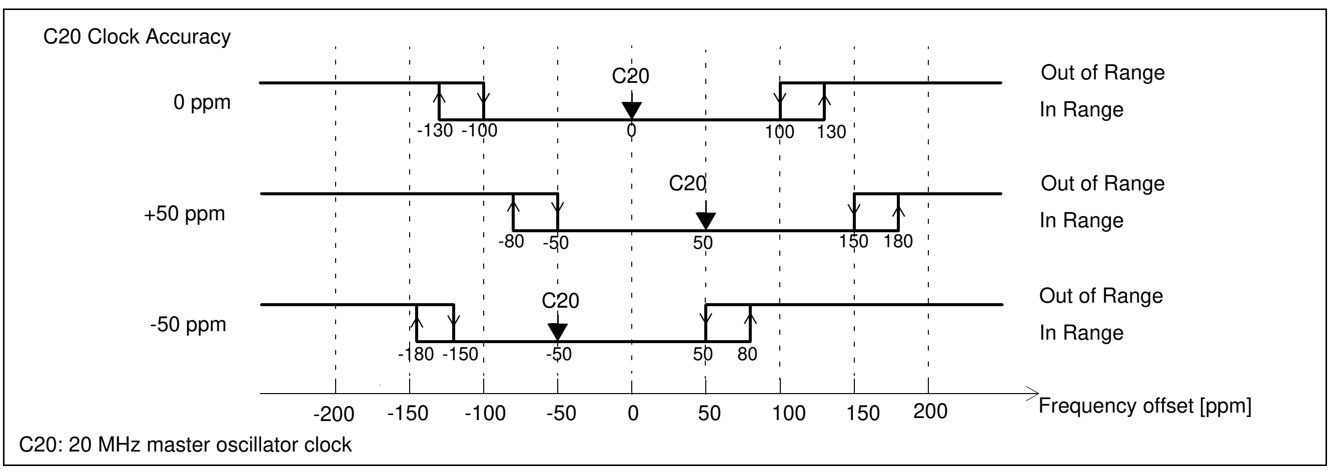


Figure 6 - E1 Out-of-Range Thresholds for APP_SEL=01

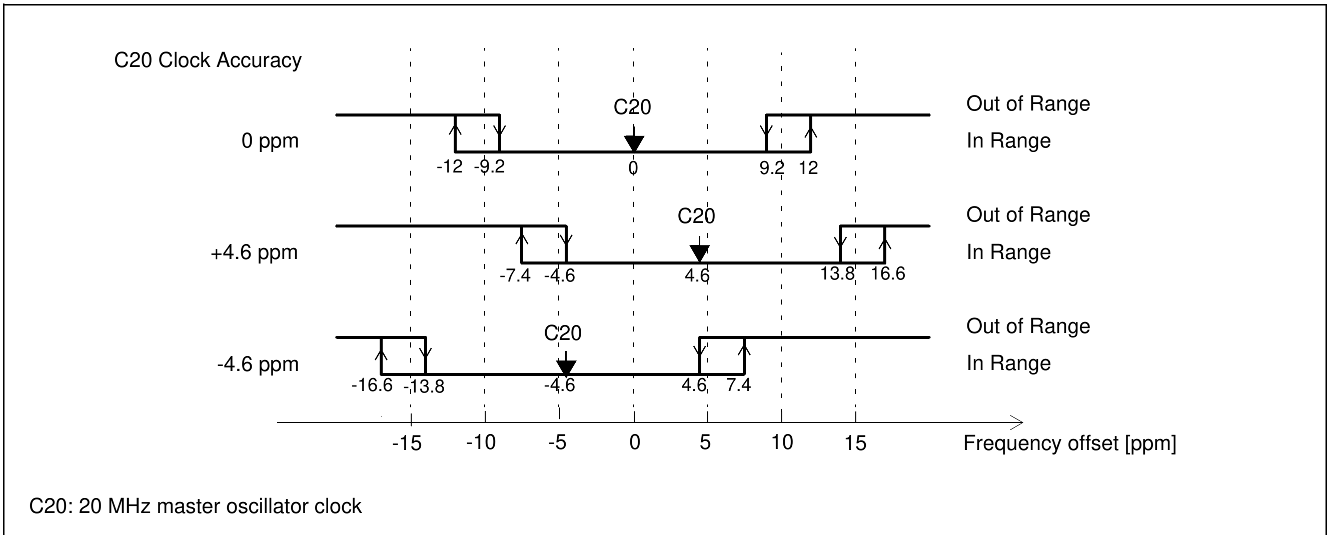


Figure 7 - Out-of-Range Thresholds for APP_SEL=10 and APP_SEL=11

In addition to the monitoring of the REF2 reference signal the companion REF2_SYNC input signal is also monitored for failure (see Figure 8).

Sync Ratio Monitor (SRM): This monitor detects if the REF2_SYNC signal is a 2 kHz or an 8 kHz signal. It also checks the number of REF2 reference clock cycles in a single REF2_SYNC frame pulse period to determine the integrity of the REF2_SYNC signal, for example there must be exactly 256 clock cycles of a 2.048 MHz REF2 reference clock in a single REF2_SYNC 8 kHz frame pulse period to validate the REF2_SYNC signal. If the REF2 and REF2_SYNC inputs are selected for synchronization and the Sync Ratio Monitor detects a failure, the DPLL will abandon the mechanism of aligning the output frame pulse to the REF2_SYNC pulse. Instead only the REF2 reference will be used for synchronization.

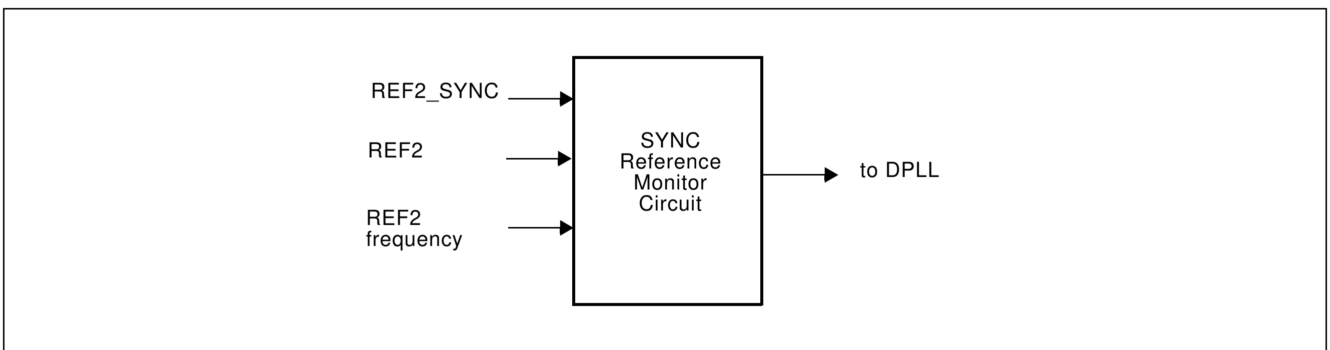


Figure 8 - REF2_SYNC Reference Monitor

3.3 Time Interval Error (TIE) Corrector Circuit

The TIE Circuit eliminates phase transients on the output clock that may occur during reference switching or the recovery from Holdover mode to Normal mode.

On recovery from Holdover mode (dependent on the HMS pin) or when switching to another reference input, the TIE corrector circuit measures the phase delay between the current phase (feedback signal) and the phase of the selected reference signal. This delay value is stored in the TIE corrector circuit. This circuit creates a new virtual reference signal that is at the same phase position as the feedback signal. By using the virtual reference, the PLL minimizes the phase transient it experiences when it recovers from Holdover mode.

The delay value can be reset by setting the TIE Corrector Circuit Clear pin (TIE_CLR) low for at least 15 ns. This results in a phase alignment between the input reference signal and the output clocks and frame pulses as shown in Figure 26. The speed of the phase alignment correction is limited by the selected loop filter bandwidth and the phase slope limit (see Table 2). Convergence is always in the direction of least phase travel. TIE_CLR can be kept low continuously; in that case the output clocks will always align with the selected input reference. This is illustrated in Figure 9.

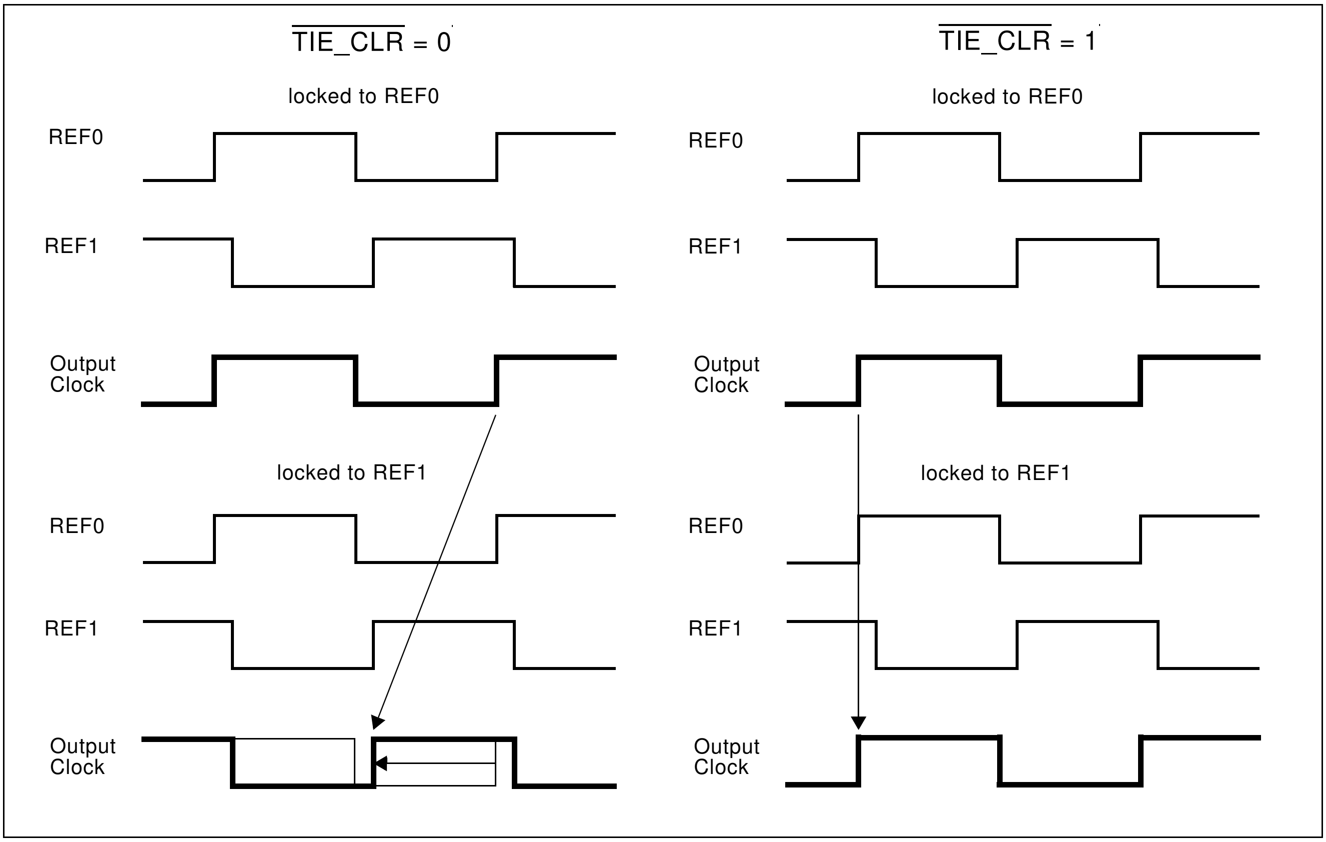


Figure 9 - Timing Diagram of Hitless Reference Switching

The Hitless Mode Switching (HMS) pin enables phase hitless returns from Freerun and Holdover modes to Normal mode in a single reference operation. A logic low at the HMS input disables the TIE circuit updating the delay value thereby forcing the output of the PLL to gradually move back to the original point before it went into Holdover mode. (see Figure 10). This prevents accumulation of phase in network elements. A logic high (HMS=1) enables the TIE circuit to update its delay value thereby preventing a large output phase movement after return to Normal mode. This causes accumulation of phase in network elements. In both cases the PLL's output can be aligned with the input reference by setting TIE_CLR low. Regardless of the HMS pin state, reference switching in the ZL30105 is always hitless unless TIE_CLR is kept low continuously.

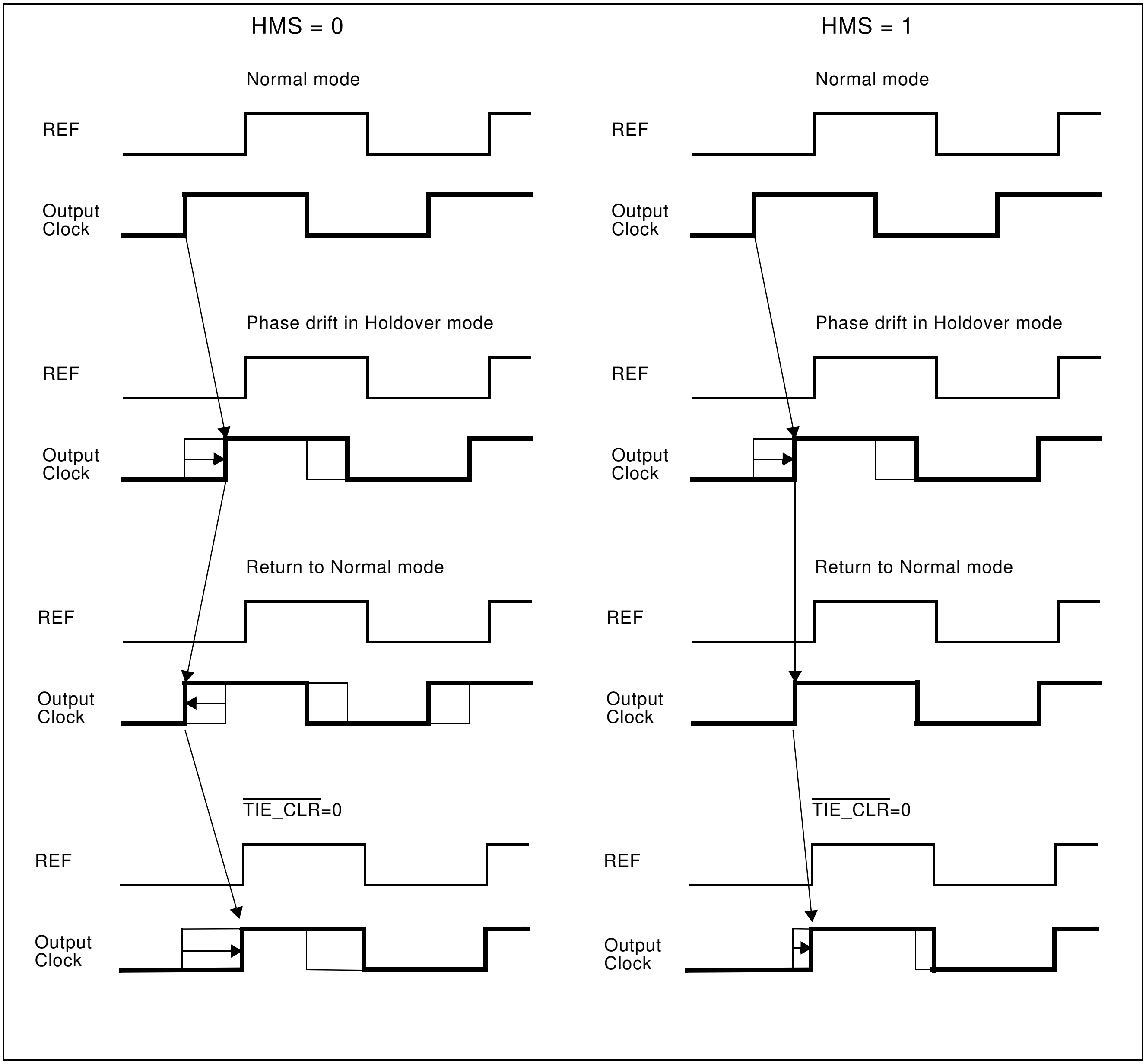


Figure 10 - Timing Diagram of Hitless Mode Switching

Examples:

HMS=1: When ten Normal to Holdover to Normal mode transitions occur and in each case the Holdover mode was entered for 2 seconds then the accumulated phase change (MTIE) could be as large as 330 ns.

- $Phase_{holdover\_drift}$ = 0.01 ppm x 2 s = 20 ns
- $Phase_{mode\_change}$ = 0 ns + 13 ns = 13 ns
- $Phase_{10\ changes}$ = 10 x (20 ns + 13 ns) = 330 ns

where:

- 0.01 ppm is the accuracy of the Holdover mode
- 0 ns is the maximum phase discontinuity in the transition from the Normal mode to the Holdover mode
- 13 ns is the maximum phase discontinuity in the transition from the Holdover mode to the Normal mode when a new TIE corrector value is calculated

HMS=0: When the same ten Normal to Holdover to Normal mode changes occur and in each case Holdover mode was entered for 2 seconds, then the overall MTIE would be 20 ns. As the delay value for the TIE corrector circuit is not updated, there is no 13 ns measurement error at this point. The phase can still drift for 20 ns when the PLL is in Holdover mode but when the PLL enters Normal mode again, the phase moves back to the original point so the phase is not accumulated.

3.4 Digital Phase Lock Loop (DPLL)

The DPLL of the ZL30105 consists of a phase detector, a limiter, a loop filter and a digitally controlled oscillator as shown in Figure 11. The data path from the phase detector to the limiter is tapped and routed to the lock detector that provides a lock indication which is output at the LOCK pin.

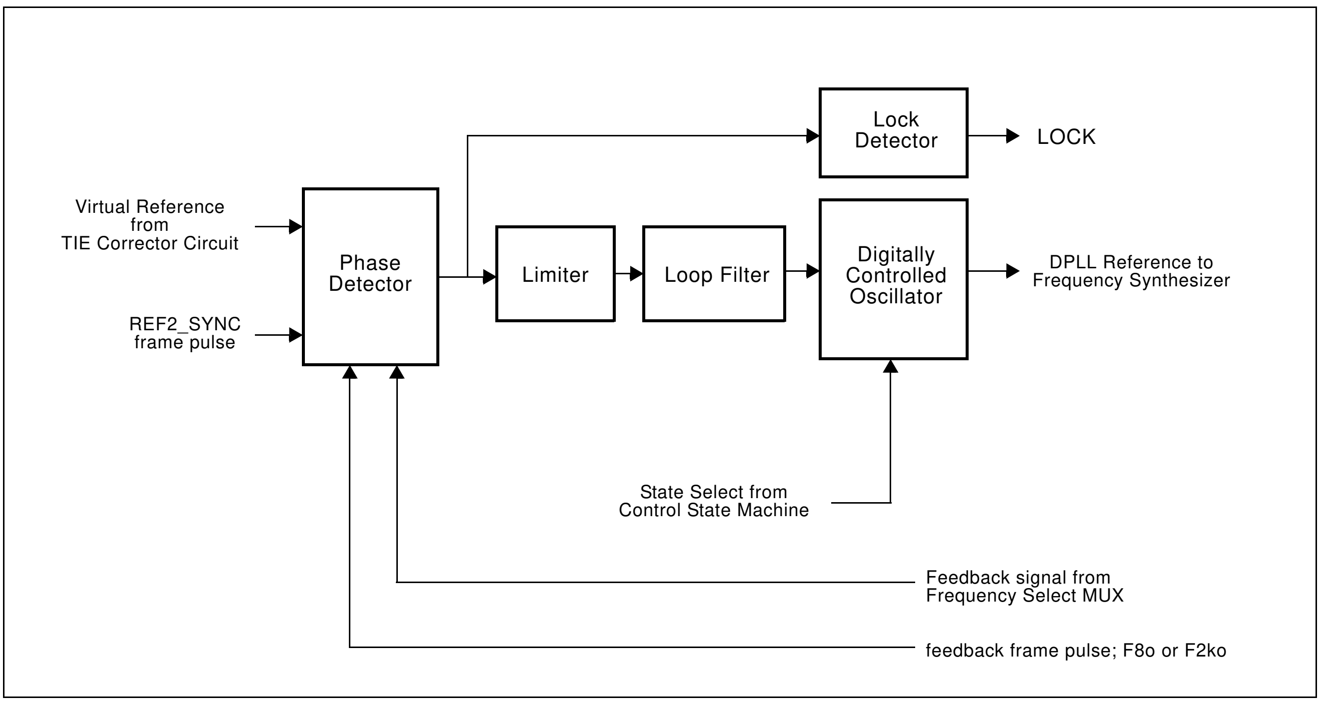


Figure 11 - DPLL Block Diagram

Phase Detector - the phase detector compares the virtual reference signal from the TIE corrector circuit with the feedback signal and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the limiter circuit.

Limiter - the limiter receives the error signal from the phase detector and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope compliant with the applicable standards. The phase slope limit is dependent on the APP_SEL1:0 and SEC_MSTR pins and is listed in Table 2.

Loop Filter - the loop filter is similar to a first order low pass filter with a bandwidth of 1.8 Hz or 3.6 Hz, suitable to provide Primary Master timing. When Secondary Master mode is selected (SEC_MSTR=1), the filter bandwidth is set to 922 Hz. For stability reasons, the loop filter bandwidth for 2 kHz and 8 kHz reference inputs is limited to a maximum of 14 Hz and 58 Hz respectively.

Digitally Controlled Oscillator (DCO) - the DCO receives the limited and filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the ZL30105.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Holdover Mode, the DCO is free running at a frequency equal to the frequency that the DCO was generating in Normal Mode. The frequency in Holdover mode is calculated from frequency samples stored 26 ms to 52 ms before the ZL30105 entered Holdover mode. This ensures that the coarse frequency monitor and the single cycle monitor have time to disqualify a bad reference before it corrupts the holdover frequency.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 20 MHz source.

Lock Indicator - the lock detector monitors if the output value of the phase detector is within the phase-lock-window for a certain time. The selected phase-lock-window guarantees the stable operation of the LOCK pin with maximum network jitter and wander on the reference input. If the DPLL goes into Holdover mode (auto or manual), the LOCK pin will initially stay high for 1 s in Primary Master mode. In Secondary Master mode, LOCK remains high for 0.1 s. If at that point the DPLL is still in holdover mode, the LOCK pin will go low; subsequently the LOCK pin will not return high for at least the full lock-time duration. In Freerun mode the LOCK pin will go low immediately.

3.5 Frequency Synthesizers

The output of the DCO is used by the frequency synthesizers to generate the output clocks and frame pulses which are synchronized to one of three reference inputs (REF0, REF1 or REF2). The frequency synthesizer uses digital techniques to generate output clocks and advanced noise shaping techniques to minimize the output jitter. The clock and frame pulse outputs have limited driving capability and should be buffered when driving high capacitance loads.

3.6 State Machine

As shown in Figure 1, the state machine controls the TIE Corrector Circuit and the DPLL. The control of the ZL30105 is based on the inputs MODE_SEL1:0, REF_SEL1:0 and HMS.

3.7 Master Clock

The ZL30105 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

4.0 Control and Modes of Operation

4.1 Application Selection

APP_SEL	Application	Applicable Standard	Out Of Range Limits
00	DS1	ANSI T1.403 Telcordia GR-1244-CORE Stratum 4/4E	64 - 83 ppm
01	E1	ITU-T G.703 ETSI ETS 300 011	100 - 130 ppm
10	PDH Stratum 3	Telcordia GR-1244-CORE Stratum 3	9.2 - 12 ppm
11	SDH	ITU-T G.813 Option 1 Telcordia GR-253-CORE	9.2 - 12 ppm

Table 1 - Application Selection and the Out of Range Limits

4.2 Loop Filter and Limiter Selection

The loop filter and limiter settings are selected through the APP_SEL and SEC_MSTR pins, see Table 2. The maximum loop filter bandwidth is also dependent on the frequency of the currently selected reference (REF0/1/2).

APP_SEL	SEC_MSTR	Detected REF Frequency	Loop Filter Bandwidth	Phase Slope Limiting
00, 01, 10	0	any	1.8 Hz	61 μ/s
11	0	any	3.6 Hz	7.5 μ/s
00, 01, 10, 11	1	2 kHz	14 Hz	9.5 ms /s
		8 kHz	58 Hz	9.5 ms /s
		1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz, 19.44 MHz	922 Hz	9.5 ms /s

Table 2 - Loop Filter and Limiter Settings

4.3 Output Clock and Frame Pulse Selection

The output of the DCO is used by the frequency synthesizers to generate the output clocks and frame pulses which are synchronized to one of three reference inputs (REF0, REF1 or REF2). These signals are available in two groups controlled by the OUT_SEL2:0 pins, see Table 3.

OUT_SEL2	Generated Clocks	Generated Frame Pulses
0	C2o, $\overline{\text{C4o}}$, C8o, $\overline{\text{C16o}}$	$\overline{\text{F4o}}$, F8o, $\overline{\text{F16o}}$
1	C2o, $\overline{\text{C16o}}$, C32, $\overline{\text{C65o}}$	$\overline{\text{F16o}}$, F32o, $\overline{\text{F65o}}$
OUT_SEL1:0		
00	C6o	
01	C8.4o	
10	C34o	
11	C44o	

Table 3 - Clock and Frame Pulse Selection with OUT_SEL Pin

4.4 Modes of Operation

The ZL30105 has three possible manual modes of operation; Normal, Holdover and Freerun. These modes are selected with mode select pins MODE_SEL1 and MODE_SEL0 as is shown in Table 4. Transitioning from one mode to the other is controlled by an external controller. The ZL30105 can be configured to automatically select a valid input reference under control of its internal state machine by setting MODE_SEL1:0 = 11. In this mode of operation, a state machine controls selection of references (REF0 or REF1) used for synchronization.

MODE_SEL1	MODE_SEL0	Mode
0	0	Normal (with automatic Holdover)
0	1	Holdover
1	0	Freerun
1	1	Automatic (Normal with automatic Holdover and automatic reference switching)

Table 4 - Operating Modes

4.4.1 Freerun Mode

Freerun mode is typically used when an independent clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun mode, the ZL30105 provides timing and synchronization signals which are based on the master clock frequency (supplied to OSCi pin) only, and are not synchronized to the reference input signals.

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32 ppm output clock is required, the master clock must also be ±32 ppm. See Applications - Section 6.2, “Master Clock“.

4.4.2 Holdover Mode

Holdover Mode is typically used for short durations while network synchronization is temporarily disrupted.

In Holdover Mode, the ZL30105 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal.

When in Normal Mode, and locked to the input reference signal, a numerical value corresponding to the ZL30105 output reference frequency is stored alternately in two memory locations every 26 ms. When the device is switched into Holdover Mode, the value in memory from between 26 ms and 52 ms is used to set the output frequency of the device. The frequency accuracy of Holdover Mode is 0.01 ppm.

Two factors affect the accuracy of Holdover mode. One is drift on the master clock while in Holdover mode, drift on the master clock directly affects the Holdover mode accuracy. Note that the absolute master clock (OSCi) accuracy does not affect Holdover accuracy, only the *change* in OSCi accuracy while in Holdover. For example, a ±32 ppm master clock may have a temperature coefficient of ±0.1 ppm per °C. So a ±10 °C change in temperature, while the ZL30105 is in Holdover mode may result in an additional offset (over the 0.01 ppm) in frequency accuracy of ±1 ppm. Which is much greater than the 0.01 ppm of the ZL30105. The other factor affecting the accuracy is large jitter on the reference input prior to the mode switch.

4.4.3 Normal Mode

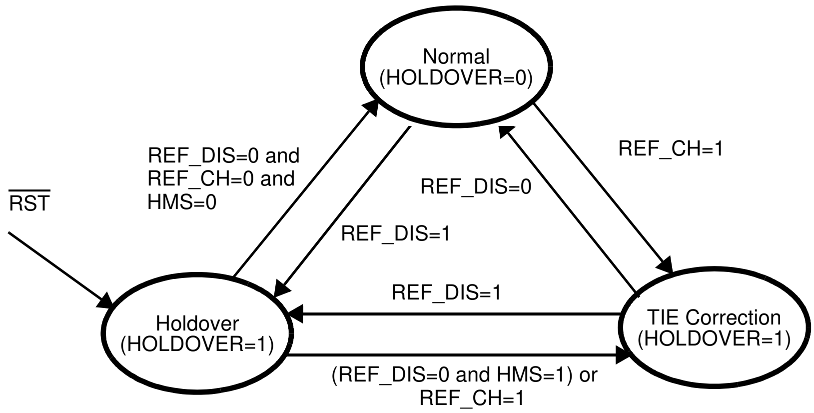
Normal mode is typically used when a system clock source, synchronized to the network is required. In Normal mode, the ZL30105 provides timing and frame synchronization signals, which are synchronized to one of three reference inputs (REF0, REF1 or REF2). The input reference signal may have a nominal frequency of 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz. The frequency of the reference inputs are automatically detected by the reference monitors.

When the ZL30105 comes out of RESET while Normal mode is selected by its MODE_SEL pins then it will initially go into Holdover mode and generate clocks with the accuracy of its freerunning local oscillator (see Figure 12). If the ZL30105 determines that its selected reference is disrupted (see Figure 3), it will remain in Holdover until the selected reference is no longer disrupted or the external controller selects another reference that is not disrupted. If the ZL30105 determines that its selected reference is not disrupted (see Figure 3) then the state machine will cause the DPLL to recover from Holdover via one of two paths depending on the logic level at the HMS pin. If HMS=0 then the ZL30105 will transition directly to Normal mode and it will align its output signals with its selected input reference (see Figure 10). If HMS=1 then the ZL30105 will transition to Normal mode via the TIE correction state and the phase difference between the output signals and the selected input reference will be maintained.

When the ZL30105 is operating in Normal mode, if it determines that its selected reference is disrupted (Figure 3) then its state machine will cause it to automatically go to Holdover mode. When the ZL30105 determines that its selected reference is not disrupted then the state machine will cause the DPLL to recover from Holdover via one of two paths depending on the logic level at the HMS pin (see Figure 12). If HMS=0 then the ZL30105 will transition directly to Normal mode and it will align its output signals with its input reference (see Figure 10). If HMS=1 then the ZL30105 will transition to Normal mode via the TIE correction state and the phase difference between the output signals and the input reference will be maintained.

If the reference selection changes because the value of the REF_SEL1:0 pins changes or because the reference selection state machine selected a different reference input, the ZL30105 goes into Holdover mode and returns to Normal mode through the TIE correction state regardless of the logic value on HMS pin.

ZL30105 provides a fast lock pin (FASTLOCK), which, when set high enables the PLL to lock to an incoming reference within approximately 1 s.



REF_DIS=1: Current selected reference disrupted (see Figure 3). REF_DIS is an internal signal.

REF_CH= 1: Reference change, a transition in the reference selection (see Figure 14) or a change in the REF_SEL pins. REF_CH is an internal signal.

Figure 12 - Mode Switching in Normal Mode

4.4.4 Automatic Mode

The Automatic mode combines the functionality of the Normal mode (automatic Holdover) with automatic reference switching. The automatic reference switching is described in more detail in section 4.5.2, “Automatic Reference Switching“.

4.5 Reference Switching

4.5.1 Manual Reference Switching

In the manual modes of operation (MODE_SEL1:0 ≠ 11) the active reference input (REF0, REF1 or REF2) is selected by the REF_SEL1 and REF_SEL0 pins as shown in Table 5. When the logic value of the REF_SEL pins is changed when the DPLL is in Normal mode, the ZL30105 will perform a hitless reference switch.

REF_SEL1	REF_SEL0	Input Reference Selected
0	0	REF0
0	1	REF1
1	0	REF2
1	1	REF2

Table 5 - Manual Reference Selection

When the REF_SEL inputs are used in Normal mode to force a change from the currently selected reference to another reference, the action of the LOCK output will depend on the relative frequency and phase offset of the old and new references. Where the new reference has enough frequency offset and/or TIE-corrected phase offset to force the output outside the phase-lock-window, the LOCK output will de-assert, the lock-qualify timer is reset, and LOCK will stay de-asserted for the full lock-time duration. Where the new reference is close enough in frequency and TIE-corrected phase for the output to stay within the phase-lock-window, the LOCK output will remain asserted through the reference-switch process.

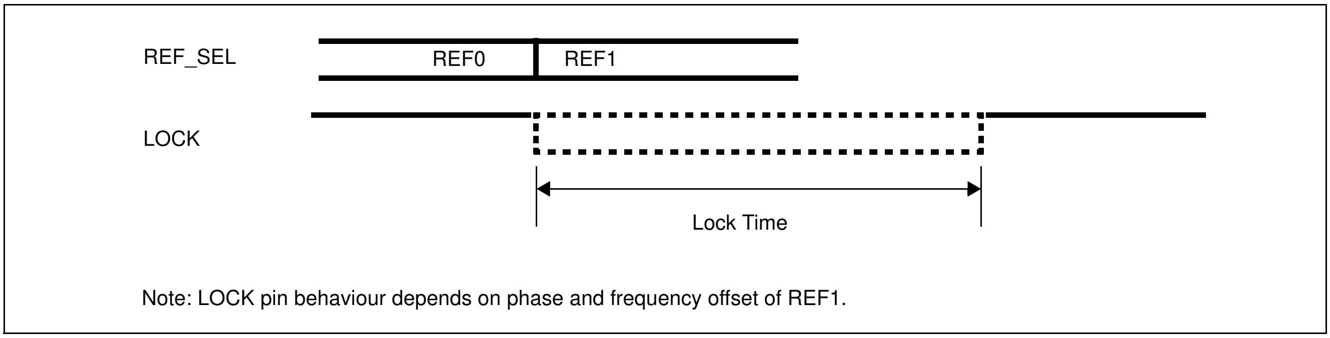


Figure 13 - Reference Switching in Normal Mode

4.5.2 Automatic Reference Switching

In the automatic mode of operation (MODE_SEL1:0 = 11), the ZL30105 automatically selects a reference input that is not out-of-range (REF_OOR=0, see Figure 3). The state machine can only select REF0 or REF1; REF2 cannot be selected in the Automatic mode (see Figure 14).

If the current reference (REF0 or REF1) used for synchronization fails, the state machine will switch to the other reference. If both references fail then the ZL30105 enters the Holdover mode without switching to another reference. When the ZL30105 comes out of reset or when REF2 is the current reference when the ZL30105 is put in the Automatic mode, then REF0 has priority over REF1. Otherwise there is no preference for REF0 or REF1 which is referred to as non-revertive reference selection.

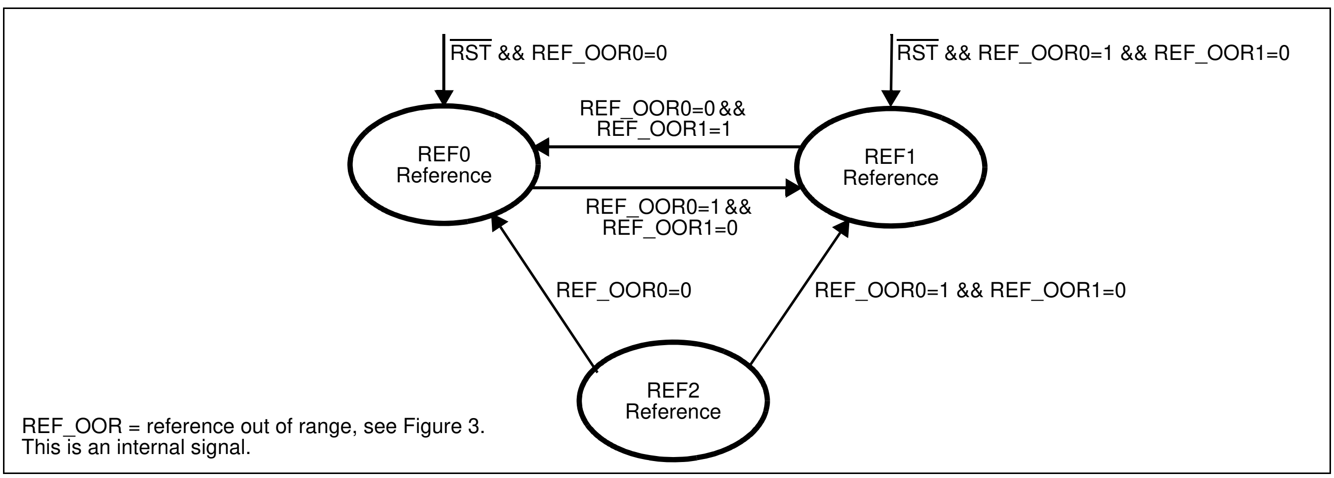


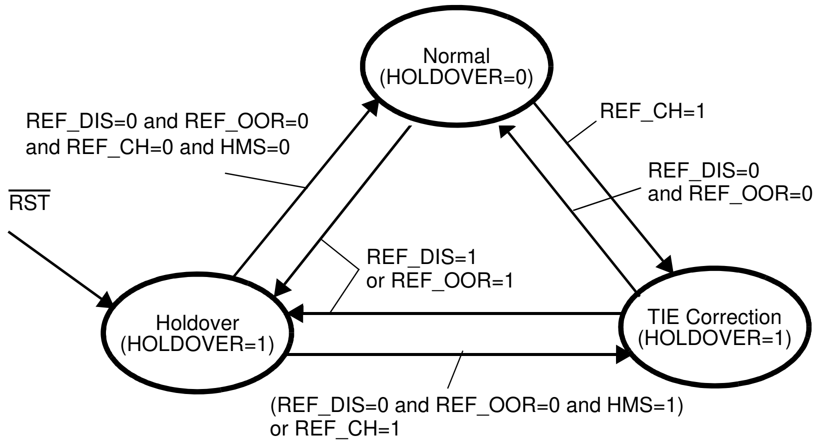
Figure 14 - Reference Selection in Automatic Mode (MODE_SEL=11)

In the automatic mode of operation, both pins REF_SEL1 and REF_SEL0 are configured as outputs. The logic level on the REF_SEL0 output indicates the current input reference being selected for synchronization (see Table 6).

REF_SEL1 (output pin)	**REF_SEL0** (output pin)	**Input Reference**
0	0	REF0
0	1	REF1

Table 6 - The Reference Selection Pins in the Automatic Mode (MODE_SEL=11)

The mode selection state machine behaves differently in Automatic mode in that when both reference REF0 and reference REF1 are out of range (REF_OOR=1), the state machine will select the Holdover state. In Normal mode the reference out of range (REF_OOR) status is ignored by the state machine. This is illustrated in Figure 15.



REF_DIS=1: Current selected reference disrupted (see Figure 3). REF_DIS is an internal signal.

REF_OOR=1: Current selected reference out of range (see Figure 3). REF_OOR is an internal signal.

REF_CH= 1: Reference change, a transition in the reference selection (see Figure 14). REF_CH is an internal signal.

Figure 15 - Mode Switching in Automatic Mode

4.5.2.1 Automatic Reference Switching - Coarse Reference Failure

When the currently-active input reference in Automatic mode fails in a coarse manner, the REF_DIS internal signal places the device in holdover, with the HOLDOVER pin and the REF_FAIL pin asserted. This can occur through triggering the Single Cycle Monitor, or the Coarse Frequency Monitor, in the Reference Monitor block. If the reference does not correct itself within the lock-disqualify duration (1 second) the LOCK pin is de-asserted. If the reference does not correct itself within the reference-disqualify duration (2.5 seconds) the HOLDOVER pin is de-asserted and the REF_SEL outputs indicate that the device has switched to the other reference. The LOCK pin remains de-asserted for the full lock-time duration, regardless of the phase and frequency offset of the old and new references. Figure 16 illustrates this process.

If the reference corrects itself within the lock-disqualify duration (< 1 second) the HOLDOVER pin is de-asserted, and the REF_FAIL pin is de-asserted. The LOCK pin remains asserted. No reference switching takes place, and the REF_SEL outputs indicate that the device has remained locked to the old reference.

If the reference does not correct itself within the lock-disqualify duration (1 second), but does correct itself within the reference-disqualify duration (< 2.5 seconds) the HOLDOVER pin is de-asserted, the REF_FAIL pin is de-asserted, and the REF_SEL outputs indicate that the device has remained locked to the old reference. However the LOCK pin is de-asserted, the lock-qualify timer is reset, and the LOCK pin remains de-asserted for the full lock-time duration. See 7.2, “Performance Characteristics“ on page 46 for lock-time duration.