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ZL30159
General Purpose Clock Rate Converter
Data Sheet

March 2015

Features

- Precision synthesizer generates any clock-rate from 1 Hz to 177.5 MHz with jitter below 1ps
- Programmable digital PLL synchronize to any clock rate from 1 Hz (1 pps) to 750 MHz
- Input reference configurable as single ended LVCMOS (up to 177.5 MHz) or differential LVPECL (up to 750 MHz)
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Programmable Digital PLL loop filter: 30 mHz, 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Two LVCMOS outputs —from 1 Hz (1 pps) to 177.5 MHz
- Operates from a single crystal resonator or clock oscillator

Ordering Information

ZL30159GGG2	64 Pin LBGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Customer defined default device configuration, including input/output frequencies, is available via OTP(One Time Programmable) memory
- Dynamically configurable via SPI/I2C interface and volatile configuration registers

Applications

- General purpose clock rate translator
- GPS receiver clock synthesizer

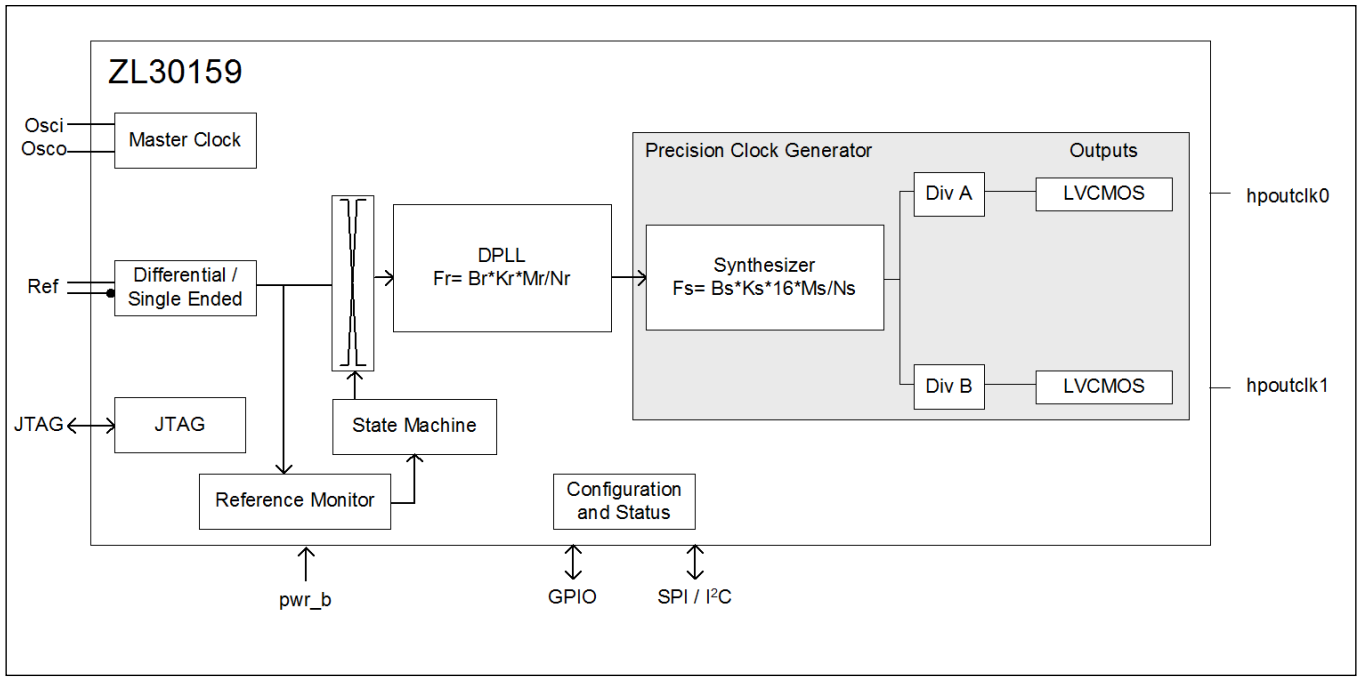

Figure 1 - Functional Block Diagram

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Change Summary

Below are the changes made May 2014 issue to March 2015 issue.

Page	Item	Change
1	Added Features bullet	Included availability of customer defined default configurations
12, 24, 24	Updated section 4.0, 5.0 and added 5.1	Updated to included the availability of Custom OTP configuration
83	12.0, “Package Markings“	Added section 12 for package markings

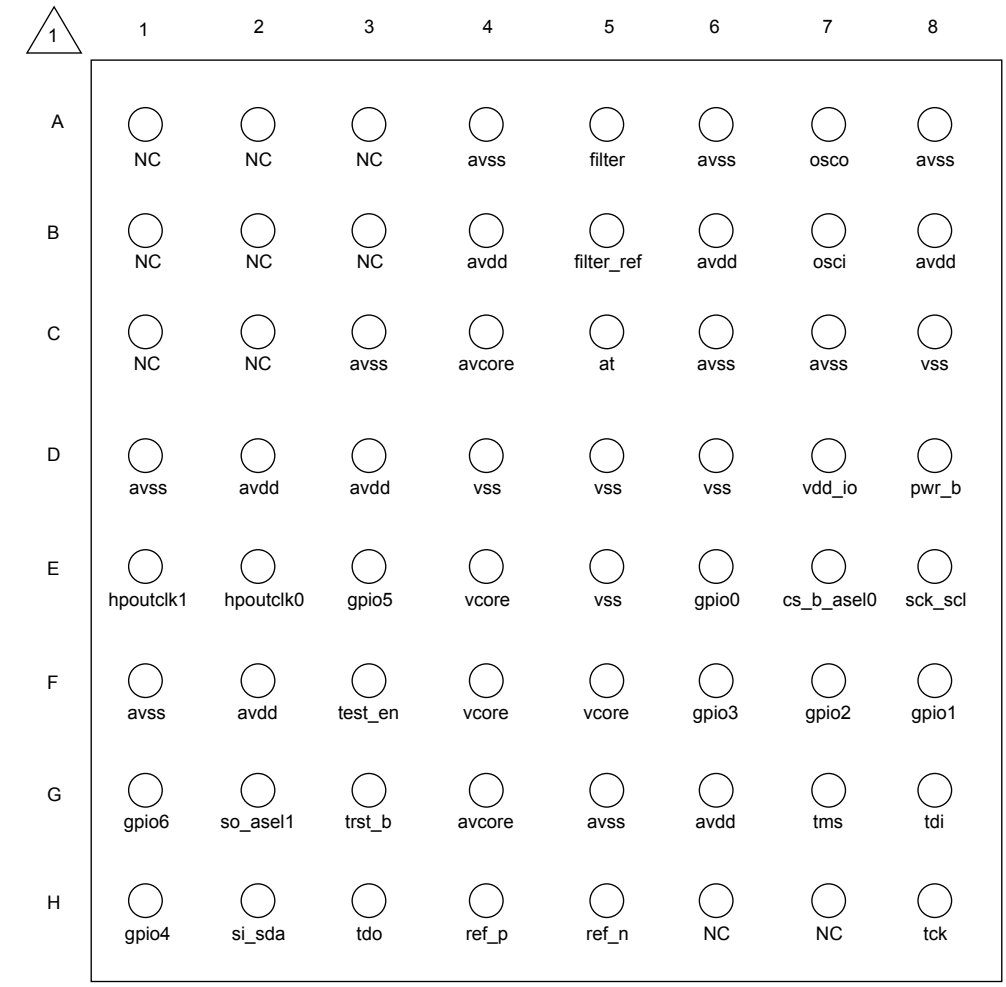
Below are the changes made from March 2013 issue to May 2014 issue.

Page	Item	Change
36 and 65	Register 0xC6: **chip_revision**	Updated chip revision regisetr to include revH id number
1, 11 ,14,15 ,46	30MHz loop filter	Numerous reference to 30MHz loop filter were corrected to read 30mHz
45	Register 0x30 : **dpll_ctrl**	Changed bits [1:0] to reserved bits with default = 0b00 (DPLL Pull-in and Hold-in range settings available at register 0xED)
57	Register 0x86:0x88: **synth_post_div_A**	Corrected description of bits 17:16
59	Register 0x89:0x8B: **synth_post_div_B**	Corrected description of bits 17:16
22	4.12, “Reset and Configuration Circuit“	Clarified power up conditions for gpio2 and gpio6
74	DC Electrical Characteristics* - High Performance Outputs	Corrected the Sym for line 2 in the table

Below are the changes made in March 2013 issue.

Page	Item	Change
Multiple	Zarlink logo and name reference	Updated to Microsemi® logo and name.
1	, “Ordering Information“	Removed GGG part number.

1.0 Pin Diagram



1 - A1 corner is identified by metallized markings.

2.0 Pin Description

All device inputs and output are LVCMOS unless it was specifically stated to be differential.

Ball #	Name	I/O	Description
Input Reference			
H4 H5	ref_p ref_n	I	**Input Reference.** Input reference used for synchronization. The positive and negative pair of this input accept a differential input signal. The ref_p input terminal accept a CMOS input reference. Maximum frequency limit on single ended input is 177.5 MHz, and 750 MHz on differential input.
Output Clocks			
E2 E1	hpoutclk0 hpoutclk1	O	**High Performance Output Clock 0 to 1.** This output can be configured to provide any one of the single ended high performance clock outputs. Maximum frequency limit on single ended LVCMOS outputs is 177.5 MHz
Control and Status			
D8	pwr_b	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The pwr_b pin should be held low for at least 2 ms. This pin is internally pulled-up to V_{DD}. **User can access device registers either 55 ms after pwr_b goes high, or after bit 7 in register at address 0x00 goes high which can be determined by polling address 0x00.**

Table 1 - Pin Description

Ball #	Name	I/O	Description
E6 F8 F7 F6 H1 E3 G1	gpio0 gpio1 gpio2 gpio3 gpio4 gpio5 gpio6	I/O	**General Purpose Input and Output pins.** These are general purpose pins managed by the internal processor based on device configuration. Recommended usage of GPIO include: • DPLL lock indicators • DPLL holdover indicators • Reference fail indicators • Reference select control or monitor • High performance LVCMOS output enable • Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR). • Microport interface protocol I2C or SPI • Master Clock frequency rate Pins gpio[5:0] are internally pulled down to GND and pin gpio6 is internally pulled up to V_{DD}. **After power on reset, device GPIO[0,1,3,4,5] configure some of device basic functions, GPIO[3] set I2C or SPI control mode, GPIO[1,0] set master clock rate selection. The GPIO[0,1,3] pins must be either pulled low or high with an external 1KΩ resistor as needed for their assigned functions at reset; or they must be driven low or high for 55 ms after reset, and released and used for normal GPIO functions.** **The GPIO[4,5] pins must be either pulled low with external 1KΩ resistors; or they must be driven low for 55 ms after reset, and then released and used for normal GPIO functions.**
Host Interface			
E8	sck_scl	I/O	**Clock for Serial Interface.** Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I2C mode. As an input this pin is internally pulled up to V_{DD}.
H2	si_sda	I/O	**Serial Interface Input.** Serial interface input stream. The serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when host interface is configured for I2C mode. This pin is internally pulled up to V_{DD}.
G2	so_asel1	I/O	**Serial Interface Output.** Serial interface output stream. As an output the serial stream holds the read data bits. This pin is also the I2C address select when host interface is configured for I2C mode.
E7	cs_b_asel0	I	**Chip Select for Serial Interface.** Serial interface chip select, this is an active low signal. This pin is also the I2C address select when host interface is configured for I2C mode.This pin is internally pulled up to V_{DD}.
APLL Loop Filter			
A5	filter	A	**External Analog PLL Loop Filter terminal.**

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
B5	filter_ref	A	**Analog PLL External Loop Filter Reference.**
JTAG (IEEE 1149.1) and Test			
F3	test_en	I	**Test Mode Enable.** A logic high at this pin enables device test modes. This pin is internally pulled down to GND. Connect this pin to GND.
C5	at	A-I/O	**Analog PLL Test.** Test pin for analog PLL. Leave unconnected.
H3	tdo	O	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G8	tdi	I	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
G3	trst_b	I	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to VDD. If this pin is not used then it should be connected to GND.
H8	tck	I	**Test Clock.** Provides the clock to the JTAG test logic. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
G7	tms	I	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
A7	osco	A-O	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osci. Not suitable for driving other devices. For clock oscillator operation, this pin is left unconnected.
B7	osci	I	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osco. For clock oscillator operation, this pin is connected to a clock source.
Power and Ground			
D7	V_{DD-IO}		**Positive Supply Voltage IO.** $3.3V_{DC}$ nominal.
E4 F4 F5	V_{CORE}		**Positive Supply Voltage.** $+1.8V_{DC}$ nominal.
B4 B6 B8 D2 D3 F2 G6	AV_{DD}		**Positive Analog Supply Voltage.** $+3.3V_{DC}$ nominal.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
C4 G4	AV_{CORE}		**Positive Analog Supply Voltage.** +1.8V_{DC} nominal.
C8 D4 D5 D6 E5	V_{SS}		**Ground.** 0 Volts.
A4 A6 A8 C3 C6 C7 D1 F1 G5	AV_{SS}		**Analog Ground.** 0 Volts.
No Connect			
A1 A2 A3 B1 B2 B3 C1 C2 H6 H7	NC		**Not connected to the die.** Connect to the GND.

Table 1 - Pin Description (continued)

3.0 Application Example

The device integrates a digital PLL and a high-speed low-jitter clock synthesizer. The digital PLL locks to reference frequencies as low as 1 Hz while maintaining loop stability and while maintaining the device's low-jitter generation. The digital PLL ensures automatic stand-by mode on reference fail (holdover) preventing bit errors on the transmission links. The digital PLL implements loop filters with settings as low as 30 mHz to clean noisy references; or as high as 896 Hz to closely track less noisy references. The high-speed low-jitter clock synthesizer generates clocks with frequencies as high as 177.5 MHz with typical jitter performance below 1 ps RMS. The digital PLL plus high-speed synthesizer architecture allows the device to easily convert between SONET/SDH and Ethernet frequencies, with or without FEC scaling or line coding. Figure 2 shows an example application where ZL30159 is used to generate 25 MHz and 125 MHz (or any other two frequencies) from 1pps (1 Hz) input provided by GPS receiver. For applications where ZL30159 is synchronized to 1pps signal, ZL30159 loop bandwidth has to be 30 mHz.

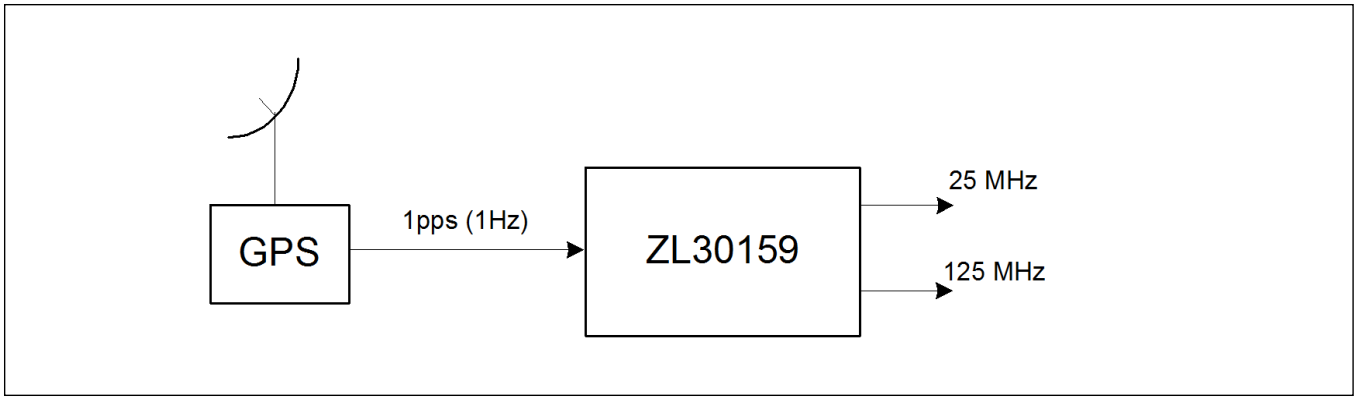


Figure 2 - Application Diagram

4.0 Functional Description

The functional block diagram of the device is shown in Figure 1. The ZL30159 is General Purpose Clock Rate Converter that can be configured by any of the following methods; power-up with its default configuration; power-up with a custom OTP (One Time Programmable) configuration; after power-up it can be dynamically configured via the SPI/I2C port. Configurations set via the SPI/I2C are volatile and will need to be rewritten if the device is reset or powered-down. The SPI/I2C port is also used to access the status registers. The ZL30159's detailed operation is described in the following sections.

4.1 Input Sources

The device has 2 input sources: one input reference (single ended or differential) and one oscillator clock source (oscillator or xtal).

The device master clock frequency is configured on reset via external voltage levels on GPIO[1:0] pins. The recommended frequency of the master clock is 24.576 MHz or 20 MHz.

The device synchronizes (locks) to any input reference which is a 1 Hz, 1 kHz multiple, or it synchronizes (locks) to any input reference which is an (M/N x 1 kHz) multiple (FEC rate converted) where M and N are 16 bits wide.

Input frequency is specified by programming four 16 bit registers: Base (B), Multiplier (K), M and N where input frequency is equal B * K * M/N. For example, to set the device to accept 1 Hz reference, the user will need to set B, K, M and N to 1. ZL30159 Evaluation Board GUI provides recommended B, K, M and N values for any required input reference frequency.

The device input reference frequency is programmed during initialization, change of input reference frequency can be supported if DPLL was forced in to Holdover mode before a frequency change.

The device accepts an input reference with maximum frequency of 177.5 MHz through single ended LVCMOS input (or 750 MHz frequency through differential inputs) and a minimum frequency of 1 Hz.

4.2 Input Reference Monitoring

The input reference is monitored by three reference monitor schemes. They indicate abnormal behavior of the reference signal, for example; drift from its nominal frequency or excessive jitter.

- **Loss of Signal Monitor (LOS)**: LOS is an external signal, fed to one of ZL30159 pins. LOS is typically generated by a PHY device whose recovered clock is fed to ZL30159 reference input. PHY device will generate LOS signal when it cannot reliably extract the clock from the line. User can set one of GPIO pins as LOS input by programming corresponding GPIO register.
- **Coarse Frequency Monitor (CFM)**: The CFM monitors input reference frequency for 1.25 ms so that it can quickly detect large changes in frequency. CFM limit for each input reference can be selected in corresponding scm_cfm_limit_ref registers with range from 0.1% to 50%. If the CFM limit is exceeded, then CFM failure is declared for corresponding reference.
- **Precise Frequency Monitor (PFM):** The PFM block measures the frequency accuracy of the reference over a 10 second interval. To ensure an accurate frequency measurement, the PFM measurement interval is re-initiated if phase or frequency irregularities are detected by the CFM. The PFM provides a level of hysteresis between the acceptance range and the rejection range to prevent a failure indication from toggling between valid and invalid for references that are on the edge of the acceptance range. PFM limit for each reference can be selected in pfm_range registers. When determining the frequency accuracy of the reference input, the PFM uses the external oscillator's output frequency (f_{ocsi}) as its point of reference. PFM limits can be set in pfm_range register at address 0xF7.

- **Single Cycle Monitor (SCM)**: This detector measures rising to rising edge and falling to falling edge periods. If either of them exceeds predefined SCM limit then SCM failure is declared. SCM limit for each

input reference can be selected in corresponding scm_cfm_limit_ref registers with range from 0.1% to 50%. The limits are input frequency dependent. Please refer to the description in scm_cfm_limit_ref registers

- **Guard Soak Timer (GST):** Timer associated with the CFM and SCM modules to disqualify the reference input signal (see Table 2)

The monitor failure indicator is flagged in the status register and have associated mask bit, as follows:

- Reference Fail Mask: RefFailMask<3:0> in register at address 0x09: these bits mask the LOS, SCM, CFM, GST failure indicators and Ref Fail PFM Mask in register at address 0xF5.
- Holdover Mask for the reference: HOMask<3:0> in register at address 0x34, these bits mask the he LOS, SCM, CFM, GST failure indicators and DPLL Holdover Mask on PFM in register at address 0xF4 that are used to put device into auto-holdover on reference failure.
- MSB bit for GST and LSB bit for LOS

The single cycle and coarse monitor failure flags feed a timer (Guard Soak Timer) that disqualifies the reference input signal when the failures are present for more than the period of time defined in Table 2.

Guard Soak Timer Control bits in control register	Time to disqualify a reference	Notes
00	minimum delay possible	
01	10 ms	
10	50 ms	default value
11	2.5 s	

Table 2 - Guard Soak Time To Disqualify A Reference

The Guard Soak Timer that is used for the CFM and SCM modules has a built-in decay time hysteresis according to Table 3 (Timer to Qualify a reference) to prevent flickering of status bits at the threshold boundaries.

The Timer to Qualify a reference is a multiple of the Guard Soak Timer. Table 3 shows the multiplication factor to multiply the Guard Soak Timer to calculate the time to qualify a reference.

Control bits to control the Timer to qualify a reference	Multiples of the Guard Soak Time to qualify a reference	Notes
00	2	
01	4	Default value
10	16	
11	32	

Table 3 - Guard Soak Time To Qualify A Reference

When a GPIO pin is used as a reference fail indicator, it indicates a valid reference if:

- The SCM does not detect phase hits, nor complete loss of clock or RefFailMask<1> is at logic “0”
- The CFM does not detect phase irregularity or RefFailMask<2> is at logic “0”
- The Guard Soak Time is triggered or RefFailMask<3> is at logic “0”

4.2.1 DPLL General Characteristics

Pull-in Hold-in range

The DPLL supports pull-in/hold-in of +/-52 ppm, +/-130 ppm or +/-400 ppm or +/-3900 ppm.

DPLL bandwidth (jitter/wander transfer)

The DPLL supports the following first order filtering cut-off frequencies (30 mHz, 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz and 896 Hz), DPLL bandwidth is determined during initialization. When changing any parameter such as loop bandwidth, phase slope limit, input/output frequency etc, user should first put the device into the holdover or free run mode, program required changes, and then put the device back to the normal mode. Same procedure should be followed during the initialization phase.

The DPLL locks to an input reference and provides stable low jitter output clock if the selected loop bandwidth is less than 1/30th the input reference frequency. As an example, a 19.44 MHz reference could deploy a bandwidth up to 896 Hz, and a 1 kHz input reference would deploy a loop bandwidth of 14 Hz. For 8 kHz reference we recommend a maximum loop bandwidth of 56 Hz. 1 Hz input reference, requires loop bandwidth of 30 mHz. Such narrow loop bandwidth (30 mHz) requires very stable master crystal oscillator (TCXO or OCXO)

On the power up when the device is fed with low frequency reference such as 1 Hz with 30mHz loop bandwidth, the frequency lock will be achieved relatively fast. However, the phase lock will take longer time because the device needs to pull the phase of the output clock for up to half a second before the input and output get aligned. To speed up the phase lock time user should cycle device between normal and holdover mode three times as described below:

- On the power up the device is fed with 1pps reference

- Initialise the device by programming it via SPI/I2C bus and set it to normal mode

- Loop three times:

    - Wait for 50 seconds

    - Set the device to the holdover mode

    - Wait for 5 milliseconds

    - Set the device to the normal mode

- End loop

Jitter/Wander Generation

Jitter generation performance (detailed in Table 9 -, “Jitter Generation Specifications - HPOUT Outputs“).

Wander generation of this device is applicable only when 30 mHz loop bandwidth is used. In this case wander generation is solely dependent on short term stability of master crystal oscillator. For wider loop bandwidths of 14 Hz or higher, wander generation of this device is negligible.

Phase Transients

The Microsemi device offers the following phase slope limiting options: 61 usec/sec, 7.5 usec/sec, 0.885 usec/sec or unlimited. If required phase slope limit is 0.885 usec/sec or 7.5 usec/sec, user should first set the device to unlimited phase slope and change it to required phase slope limit (0.885 usec/sec or 7.5 usec/sec) only after the device has achieved lock.

Holdover Stability

DPLL initial holdover accuracy is better than 50 ppb.

Input Tolerance Criteria

Input tolerance indicates that the device tolerates certain jitter, wander and phase transients at its input reference while maintaining outputs within an expected performance and without experiencing any alarms, or holdover conditions. Input tolerance is associated with input reference source characteristics and the standards associated with input reference type.

DPLL Monitoring

The DPLL provides lock and holdover indicators.

The lock time is dependent on employed loop bandwidth. The device has a lock time of less than 1 sec for all available DPLL loop bandwidth selections except 30 mHz.

The frequency lock time for 30 mHz loop bandwidth is up to 90 seconds. However, the phase lock is dependent on the input and output period—how far the output phase has to move to get phase aligned with the input phase. The slowest phase lock time will be for clock with maximum period (minimum frequency) which is 1 pps (1 Hz). For 1 pps, the phase lock time will be up to 20 minutes. To speed up the lock time for 1 pps clock, user should toggle the device though the holdover mode after 1 minute (normal mode - after 1 minute go to holdover mode and back to normal mode).

4.2.2 DPLL States

The device DPLL supports three states: Free-run, Normal (Locked) and Holdover. The Holdover and Free-run states are used to cope with reference impairments.

Each of these modes have a corresponding state in the internal State Machine described as follows:

Freerun State: the Freerun state is entered when synchronization to the reference is not required or is not possible. Typically this occurs immediately following system power-up. In the Freerun State, the device provides timing and synchronization signals which are based on the master clock frequency (supplied to osci pin) only, and are not synchronized to the reference input signals. The freerun accuracy of the output clock is equal to the accuracy of the master clock (osci). So if a ±20 ppm freerun output clock is required, the master clock must also be ±20 ppm.

Holdover State: the Holdover State is typically entered when input reference is temporarily disrupted. In the Holdover State, the device provides output clocks which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal. Initial holdover accuracy is a function of DPLL while holdover drift is reliant on the drift of the master clock (osci).

Normal State: the Normal State is entered when a valid reference clock is available for synchronization. In the Normal State the device provides output clocks which are synchronized to the input reference. From a reset condition - if a valid input reference is available - the device takes less than a second (lock time) to output signals which are synchronized (phase and frequency locked) to the reference input.

4.2.3 DPLL Rate Conversion Function and FEC Support

The DPLL supports rate conversion with a 16 bit forward divider and a 16 bit feedback divider.

The DPLL provides up scaling and down scaling functions.

The DPLL has the ability to switch from normal rate (before FEC is negotiated) to FEC rate and vice versa.

The DPLL supports simple rate conversion (i.e., take in 19.44 MHz and create 255/238 FEC SONET clock of 666.51 MHz), and supports double rate conversion (i.e., take in 19.44 MHz, create FEC 10 GbE clock of 644.5313, which is 66/64 rate converted 625 MHz, or create 690.5692 which is 255/238X66/64 rate converted 625 MHz)

The following is just an example of the frequencies that can be supported (many more frequencies can be supported):

- **GbE:**
  - 25 MHz
  - 125 MHz
- **XAUI (chip to chip interface, which is a common chassis to chassis interface)**:
  - 156.25 MHz or x2 or x4 version
- **OC-192/STM-64:**
  - 155.52 MHz or x2 or x4 version
  - 155.52 MHz x 255/237 (standard EFEC for long reach) or x2 or x4 version
  - 155.52 MHz x 255/238 (standard GFEC for long reach) or x2 or x4 version
- **10 GbE:**
  - 156.25 MHz which is 125 MHz x 10/8 or x2 or x4 version
  - 155.52 MHz x 66/64 or x2 or x4 version
  - Long reach 10GE might require the following frequencies with simple rate conversion: (156.25 MHz x 255/237) and (156.25 MHz x 255/238).
- The following frequencies with double rate conversion: (155.52 MHz x 66/64 x 255/237) or (155.52 MHz x 66/64 x 255/238) and (156.25 MHz x 66/64 x 255/238) or (156.25 MHz x 66/64 x 255/238). Also, user can use x2 or x4 version of the listed frequencies.
- Application Note ZLAN-267 explains how to generate the most common frequencies.

4.2.4 DPLL Input to Output And Output to Output Phase Alignment

Techniques offered for Phase Alignment

When the output clock is locked to a jitter free and wander free input clock, input to output latency is expected to have a typical error of 0 nsec.

The coarse and fine phase adjustments allow for input to output and output to output latency corrections to compensate for PCB load delay, as detailed in 4.6, “Output Drivers“.

4.3 Frequency Synthesis Engine

The device frequency synthesis engine is comprised of a hardware DCO and an analog jitter filtering APLL with built-in digital jitter attenuation scheme. The ultra low jitter frequency synthesis engine can generate output clocks which meet the jitter generation requirements detailed in Table 9 -, “Jitter Generation Specifications - HPOUT Outputs“.

The frequency synthesis engine’s APLL requires an external RC loop filter as described in section 4.13

The frequency synthesis engines can generate any clock which is (M/N X 1 kHz) multiple (FEC rate converted clock). The M and N are 16 bits wide.

When the DPLL is locked to the input reference, the DCO external control can be used. The DCO external control allows for the calibration of the DCO center frequency to adjust for external system oscillator center frequency.

4.4 Dividers and Skew Management

The device has 2 independent dividers associated with frequency synthesis engine.

The divider engines can generate output clocks between 1 Hz and 177.5 MHz with 50% duty cycle.

The divider modules generating the single ended output clocks provides the ability to manage the phase skew of the output clock by a coarse step equal to the internal high speed clock period.

The single ended generated output clocks can be stopped either on rising or falling edge (programmed through serial interface or GPIO).

4.5 Output Multiplexer

Figure 3 shows the multiplexing configuration that is supported.

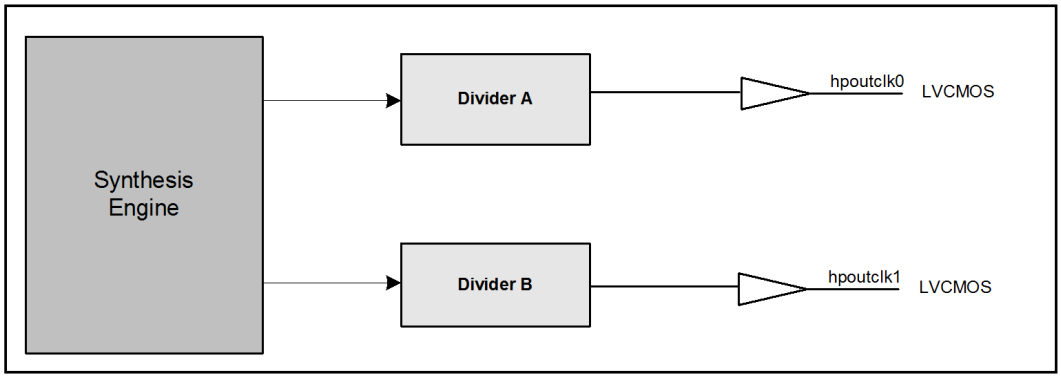


Figure 3 - Output Clocks Muxing Configuration

4.6 Output Drivers

The device has 2 high performance (HP) single ended (LVCMOS) outputs.

High Performance (HP) single ended driver (LVCMOS) supports the jitter specification detailed in Table 9 -, “Jitter Generation Specifications - HPOUT Outputs“ and a maximum speed of 177.5 MHz.

High performance LVCMOS outputs (hpoutclkx) should be terminated at the source with 22 Ω resistor as shown in Figure 4.

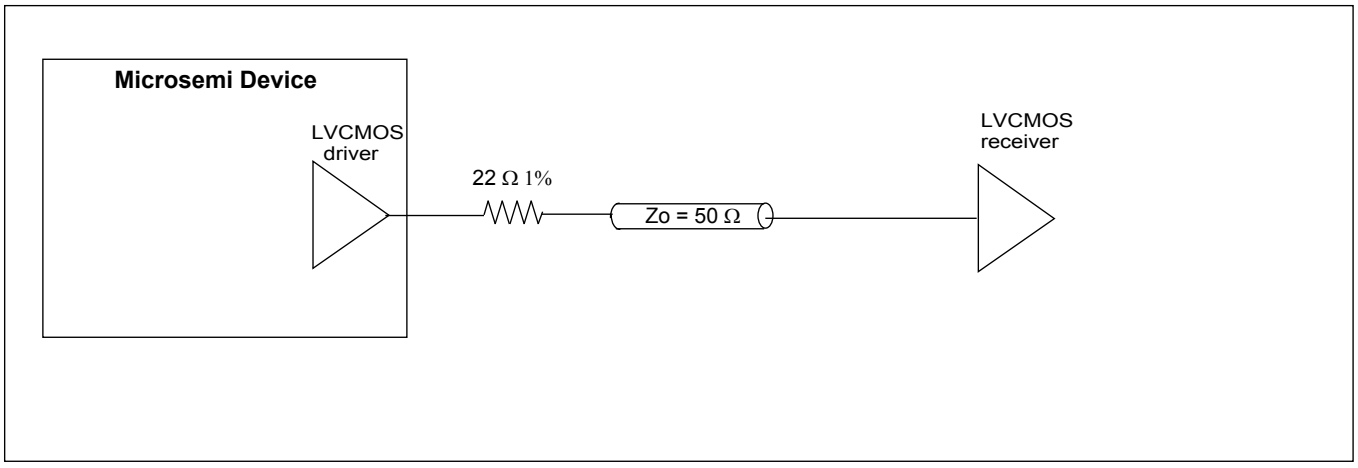


Figure 4 - Terminating HP LVCMOS Outputs

4.7 Input Buffers

ZL30159 has one reference input ref_p/ref_n that can work as either single ended or differential. By default ref is single ended. This can be changed by programming ref_config register at address 0x0A.

Input frequency range for differential input is: 1 kHz to 750 MHz; for single ended input is: 1 kHz to 177.5 MHz.

Differential reference input need to be properly terminated and biased as shown in Figure 5 and Figure 6 for LVPECL and Figure 7 and Figure 8 for LVDS drivers. When terminating LVPECL signal, it is necessary either to adjust termination resistors for DC coupling or to AC couple the LVPECL driver because ZL30159 differential input have different common mode (bias) voltage than LVPECL receivers. Thevenin termination (182 Ω and 68 Ω resistors) provide 50 ohm equivalent termination as well as biasing of the input buffer for DC coupled line. For AC

coupled line, Thevenin termination with 127 Ω and 82 Ω resistors should be used as shown in Figure 6. The value of the AC coupling capacitors will depend on the minimum reference clock frequency. The value of 10 nF is good for input clock frequencies above 100 MHz. For lower clock frequencies capacitor values will have to be increased.

Terminations for DC and AC coupled LVDS line are shown in Figure 7 and Figure 8 respectively. Differential input biasing is provided by LVDS driver in case of DC coupling (Figure 7), whereas for AC coupling (Figure 8) biasing is generated by 12 kΩ and 8.2 kΩ resistors. In both cases, the line is terminated with 100Ω.resistor.

For single ended CMOS input, ref_n input needs to be connected to the ground as shown in Figure 9. The value of series termination resistor will depend on CMOS output driver but the most common values are 33 Ω and 22 Ω.

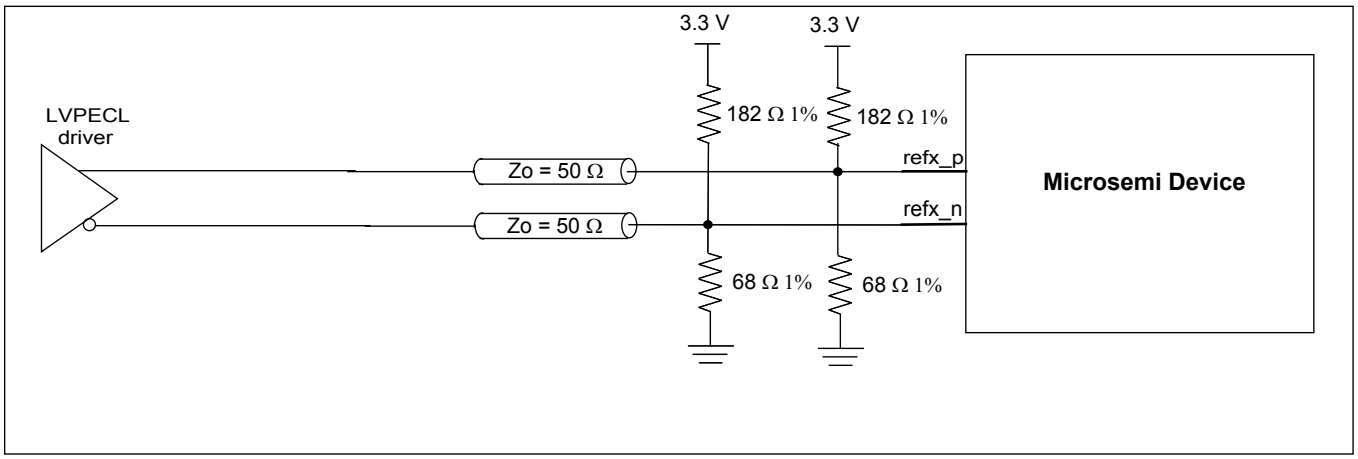


Figure 5 - Differential DC Coupled LVPECL Termination

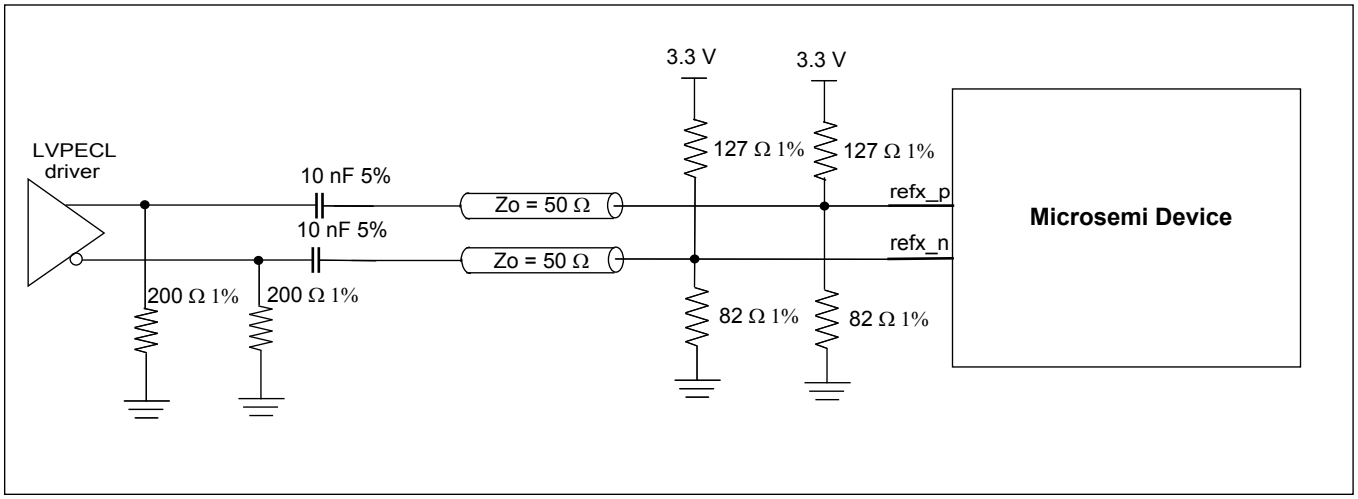


Figure 6 - Differential AC Coupled LVPECL Termination

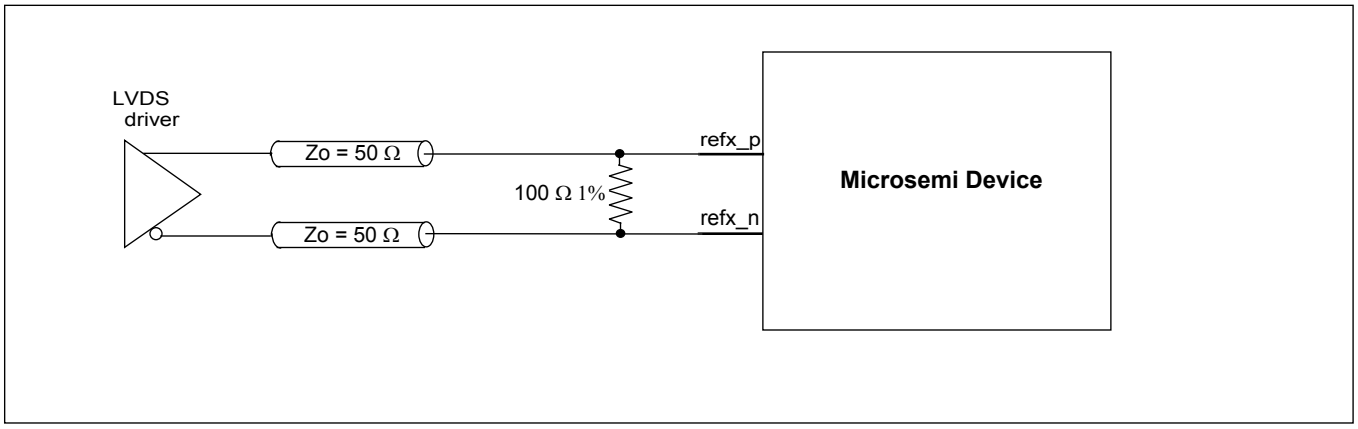


Figure 7 - Differential DC Coupled LVDS Termination

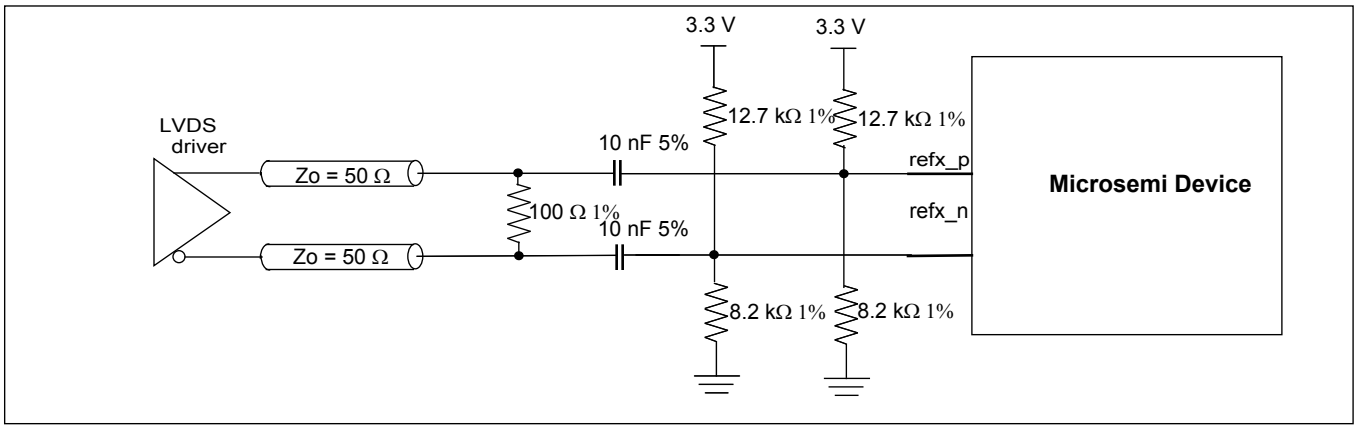


Figure 8 - Differential AC Coupled LVDS Termination

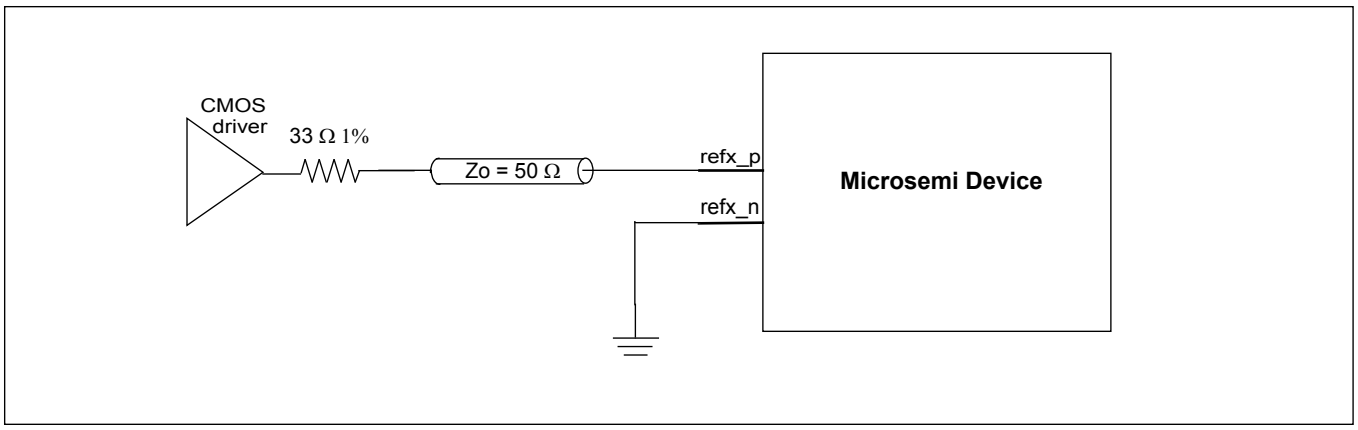


Figure 9 - Single Ended CMOS Termination

4.8 Master Clock Interface

The master oscillator determines the DPLL's free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL). Refer to application note ZLAN-68 for a list of recommended clock oscillators.

4.9 Clock Oscillator

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **osci** pin as shown in Figure 10. The connection to osci should be direct and not AC coupled. The **osco** pin must be left unconnected.

When using crystal resonator as the master timing source, connect crystal between **osci** and **osco** pins as shown in Figure 10. Crystal should have bias resistor of 1 MΩ and load capacitances C1 and C2. Value of load capacitances is dependent on crystal and should be as per crystal datasheet. Crystal should be a fundamental mode type -- not an overtone. See ZLAN-68 for crystal recommendation.

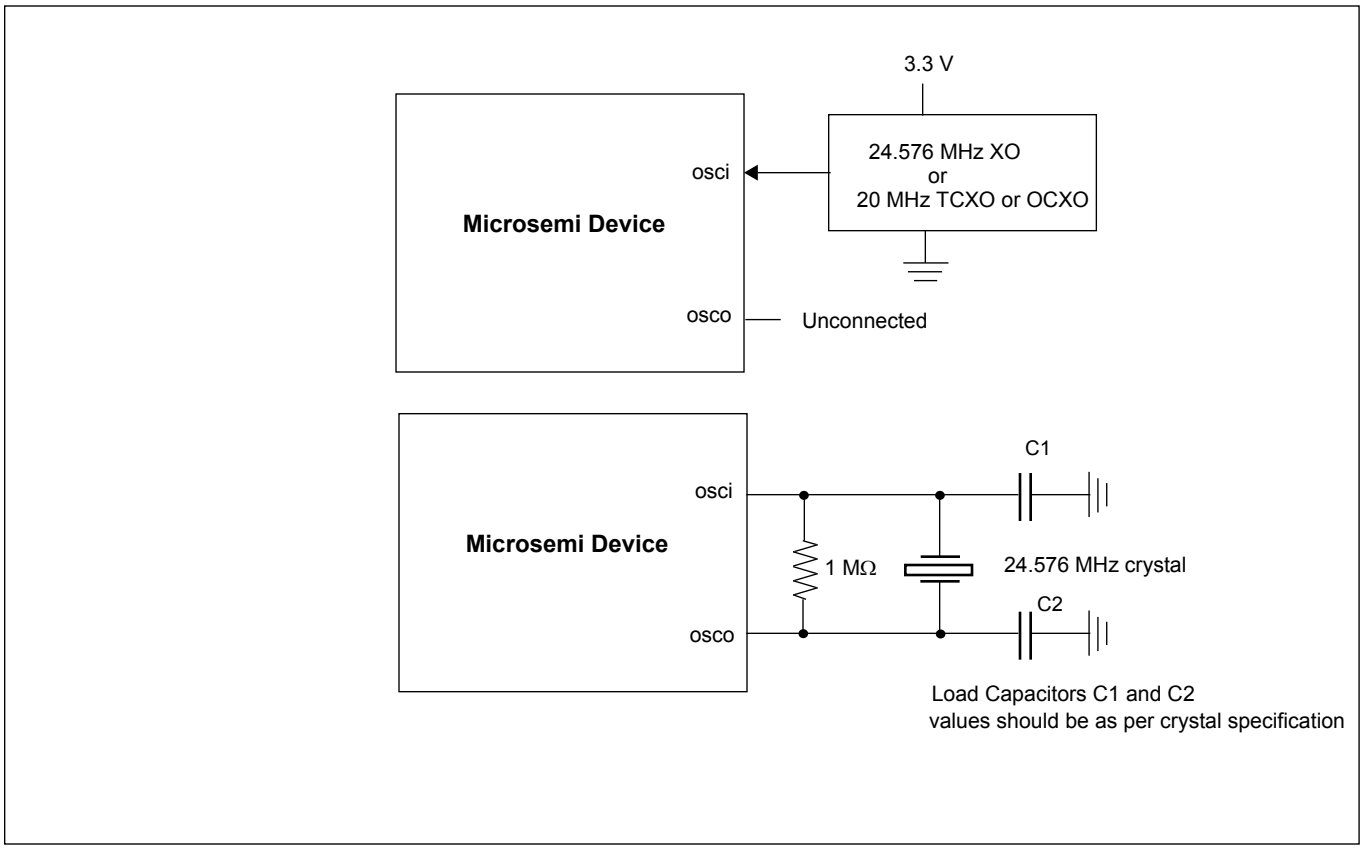


Figure 10 - Clock Oscillator Circuit

The device internal system clocks are generated off the device master clock input (Oscillator or a crystal employing an on-chip buffer/driver). The master clock selection is done at start-up using the available GPIO pins, right after pwr_b get de-asserted. GPIO[0,1] pins need to be held high for 55 ms after the de-assertion of pwr_b, after which time they can be released and used as any other GPIO. Alternatively, these pins can be pulled high with 1KΩ resistors.

GPIO [1:0]	Master Clock Frequency
00	reserved
01	reserved
10	20 MHz
11	24.576 MHz

Table 4 - Master Clock Frequency Selection

4.10 Power Up/Down Sequence

The 3.3 V power rail should be powered before or simultaneously with the 1.8 V power rail to prevent the risk of latch-up (latch-up occur when the 1.8 V supply exceeds the 3.3 V rail by more than 1.8 V).

The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

4.11 Power Supply Filtering

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Microsemi Application Note ZLAN-230.

4.12 Reset and Configuration Circuit

To ensure proper operation, the device must be reset by holding the pwr_b pin low for at least 2 ms after power-up when 3.3V and 1.8V supplies are stable. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 11. This circuit provides approximately 2 ms of reset low time. The pwr_b input has Schmidt trigger properties to prevent level bouncing.

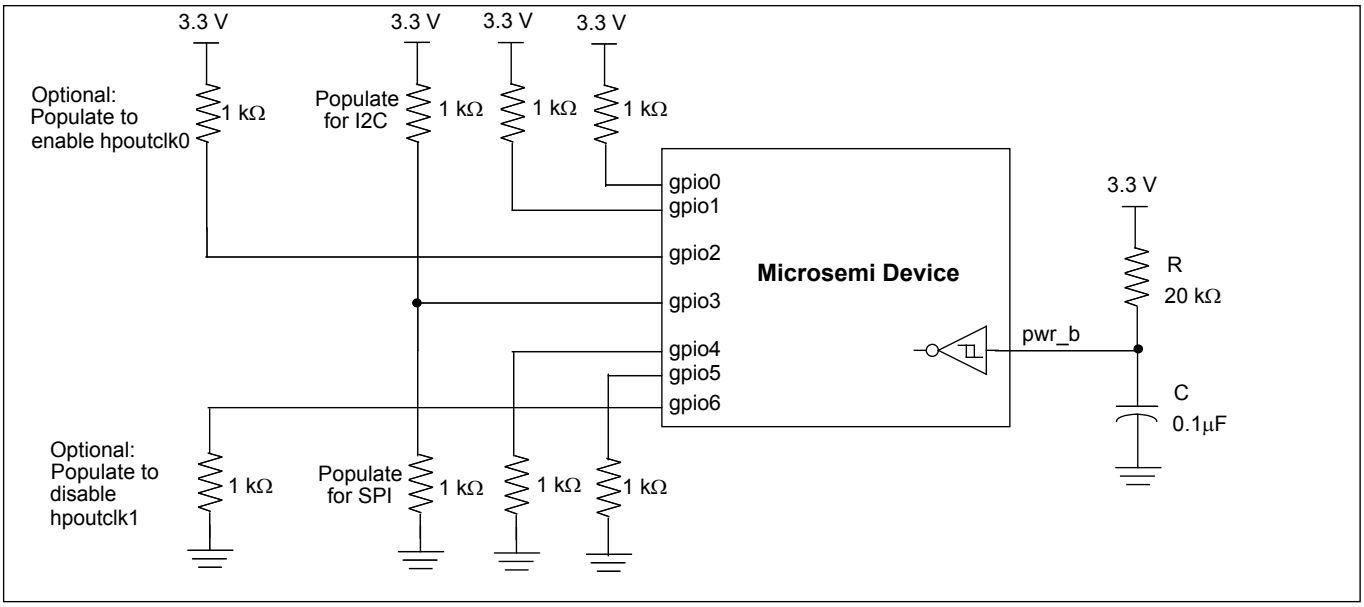


Figure 11 - Typical Power-Up Reset and Configuration Circuit with 24.576 MHz XO

General purpose pins gpio[0,1,3,4,5] are used to configure device on the power up. They have to be pulled up/down with 1 KΩ resistors as shown in Figure 11 or they can be pulsed low/high during the pwr_b low pulse and kept at the same level for at least 55 ms after pwr_b goes high. After 55 ms they can be released and used as general purpose I/O.

By default hpoutclk0 is disabled (gpio2 internal pull-down) and hpoutclk1 is enabled (gpio6 internal pull-up). During the prototype phase, a hardware designer can verify if the device is working properly even before the software driver is implemented just by pulling up gpio2 or gpio6 pin which enables hpoutclk0 output (generates 25 MHz by default) or hpclkout1 output (generates 125 MHz by default) respectively. This feature can also be used for systems where ZL30159 drives a master clock of an ethernet switch with embedded micro processor which needs 25 MHz (and/or 125 MHz) clock on the power up before it can initialize the other components on the board including ZL30159. The hpoutclk1 can be disabled at powerup by pulling down gpio6.

4.13 Ultra Low Jitter Synthesizer Filter Components and Recommended Layout

The APLL for the ultra low jitter synthesizer in the Microsemi device uses external components to help optimize its loop bandwidth. For optimal jitter performance, the following component values are recommended:

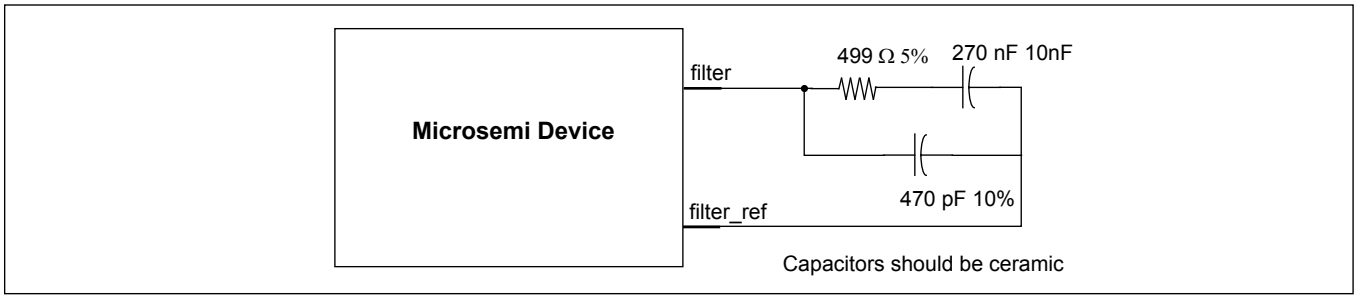


Figure 12 - APLL Filter Component Values

Recommended layout for loop filters is shown in Figure 13:

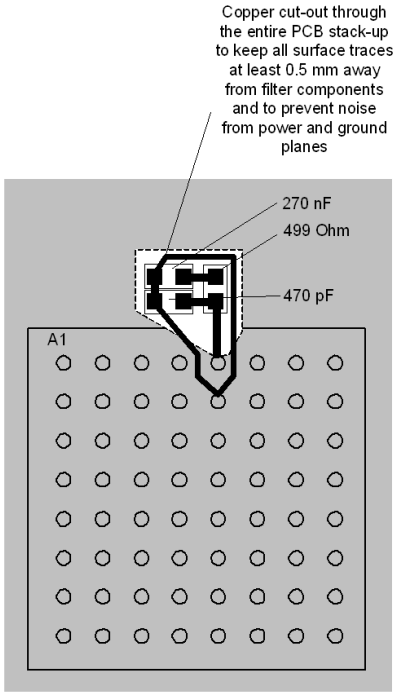


Figure 13 - Recommended Layout for Loop Filters

5.0 Configuration and Control

The ZL30159 configuration is composed of 253 x 8 bits. The configuration registers are assigned their values by any of the following three methods:

1) Default configuration
2) Custom OTP (One Time Programmable) configuration
3) SPI/I2C configuration

The SPI/I2C host interface allows field programmability of the device configuration registers. As an example, user might start the device at nominal SONET rate, then switch to an FEC rate once the link FEC rate is negotiated.

5.1 Custom OTP Configuration

At power-up the device sets its configuration registers to the user defined custom configuration values stored in it's OTP (One Time Programmable). Custom configurations can be generated using Microsemi's Clockcenter GUI software (ZLS30CLKCTR). For custom configured devices contact your local Microsemi Field Applications Engineer or Sales Manager.

5.2 GPIO Configuration and Programmability

The device GPIO is mapped by the SPI/I2C programmability. The following is an example of control and status signals that can be supported:

- DPLL lock indicators
- DPLL holdover indicators
- Reference fail indicators
- Reference control or monitor
- Output clock enable (per output)
- Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR).
- Output clock stop/start

The following table defines the function of the GPIO pin when configured as a control pin. Configuring the value in bit 7:0 in GPIO configuration registers enables the stated function.

Value	Name	Description
Default		
0x00	default	GPIO pin defined as an input. No function assigned.
Input References		
0x10	Ref external LOS signal	Ref external Loss Of Signal (LOS) - indicator to DPLLs that Ref has failed. Internally in the DPLL this signal is used for reference monitor indicator, or holdover entering and for ISR generation.
DPLL		
0x20	DPLL Time Interval Error (TIE) clear enable	This signal is OR-ed with the 'DPLL TIE clear enable' bit of the 'DPLL control' register. Functionality of this signal is explained in the 'DPLL control' register.

Value	Name	Description
Synthesizer Post Divider		
0x44	Stop output clock from Synthesizer Post Divider A bit1	This signal is OR-ed with the 'Synthesizer Post Divider A stop clock' bit1 in the 'Synthesizer Post Divider stop clock' register. Functionality of this signal is explained in above mentioned register.
0x45	Stop output clock from Synthesizer Post Divider A bit0	Same description as above.
0x46	Stop output clock from Synthesizer Post Divider B bit1	Same description as above.
0x47	Stop output clock from Synthesizer Post Divider B bit0	Same description as above.
High Performance CMOS Outputs		
0x70	Enable HPOUTCLK0	This signal is OR-ed with the 'Enable HPOUTCLK0' bit in the 'High performance CMOS output enable' register. Functionality of this signal is explained in above mentioned register.
0x72	Enable HPOUTCLK1	Same description as Enable HPOUTCLK0

The following table defines the function of the GPIO pin when configured as a status pin. Configuring the value in bit 7:0 in GPIO configuration registers enables the stated function.

Value	Name	Description
Interrupt		
0x80	Interrupt output signal	This bit will be high if the interrupt has been asserted.
Input References		
0x88	Ref - Signal not present in last second	This bit will be high if Ref signal was not toggling in the last second.
0x89	Ref Single Cycle Measurement (SCM) failure	This bit will be set if Ref SCM indicator is active (see 'Ref SCM and CFM limits' register for SCM limits).
0x8A	Ref Coarse Frequency Measurement (CFM) failure	This bit will be set if Ref CFM indicator is active (see 'Ref SCM and CFM limits' register for CFM limits).
0x8B	Ref Guard Soak Timer (GST) indicator	Ref Guard Soak Timer (GST) indicator
0x8C	Ref failure indicator	This bit will be set if either Ref external LOS signal is high, or Ref SCM, CFM or GST indicator is high, and appropriate mask bit in the 'Ref failure mask' register is set to 1 (not masked).
DPLL Filters		
0xA8	DPLL Normal mode indicator	This bit will be set when the DPLL is in normal locking mode (not holdover, not freerun)
0xA9	DPLL holdover mode indicator	This bit will be set when the DPLL is in holdover mode
0xAD	DPLL out of pull-in/hold-in range indication	This bit will be set when DPLL frequency is beyond pull-in/hold-in range limit, specified in the 'DPLL control' register
0xAF	DPLL Lock Indication 0	This bit will be set when DPLL phase error is less then 36us during 10s period.