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### Features

- Fully compliant SEC (G.813) and EEC (G.8262) flexible rate conversion digital phase locked loop (DPLL)
- Two programmable DPLLs/Numerically Controlled Oscillators (NCOs) synchronize to any clock rate from 1 Hz to 750 MHz
- Four programmable synthesizers generate any clock rate from 1 Hz to 750 MHz with maximum jitter below 0.62 ps RMS
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- DPLLs filter jitter from 0.1 mHz up to 1 kHz
- Automatic hitless reference switching and digital holdover on reference fail
- Nine input references configurable as single ended or differential and two single ended input references
- Any input reference can be fed with sync (frame pulse) or clock

**Ordering Information**

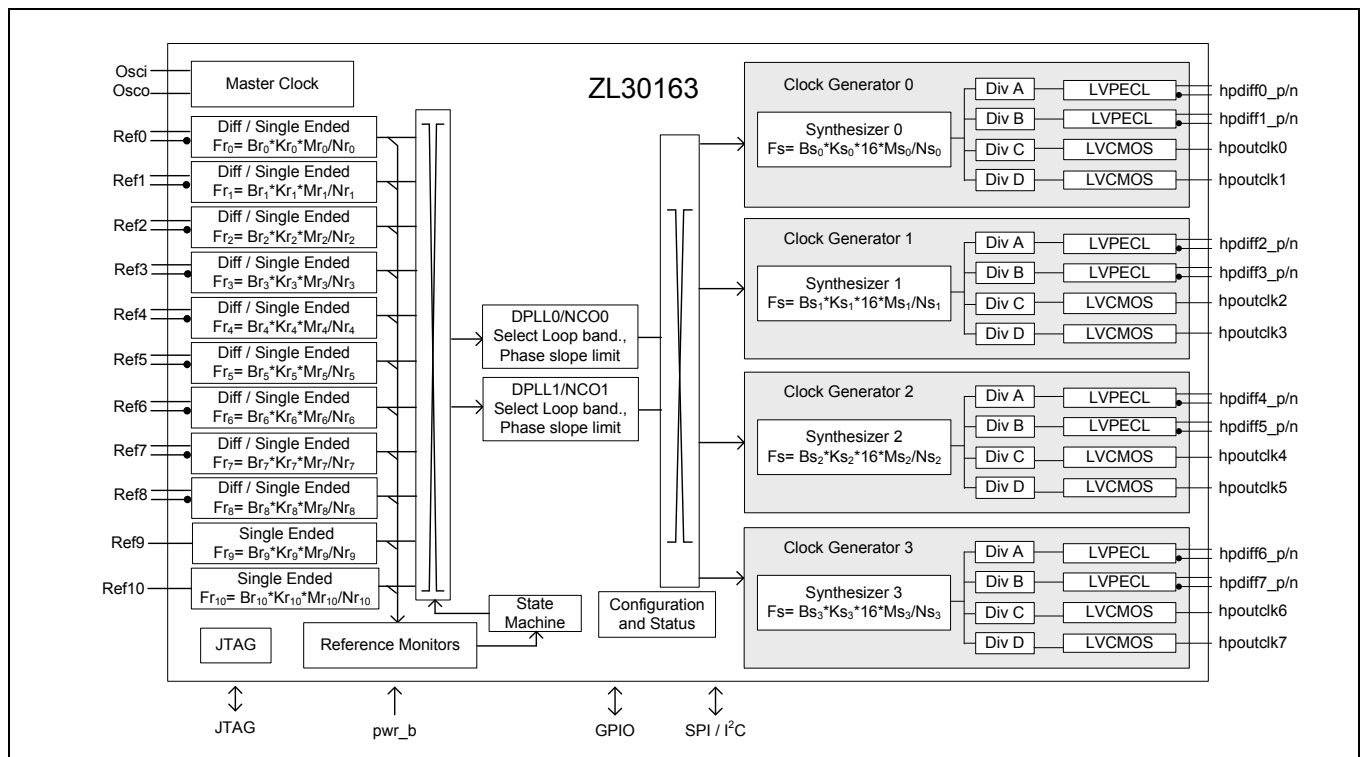
ZL30163GDG2    144 Pin LPGA    Trays

Pb Free Tin/Silver/Copper  
**-40°C to +85°C**  
 Package Size: 13 x 13 mm

- Programmable DPLLs can synchronize to sync pulse and sync pulse/clock pair
- Eight LVPECL outputs and eight LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Field programmable via the SPI/I<sup>2</sup>C interface

### Applications

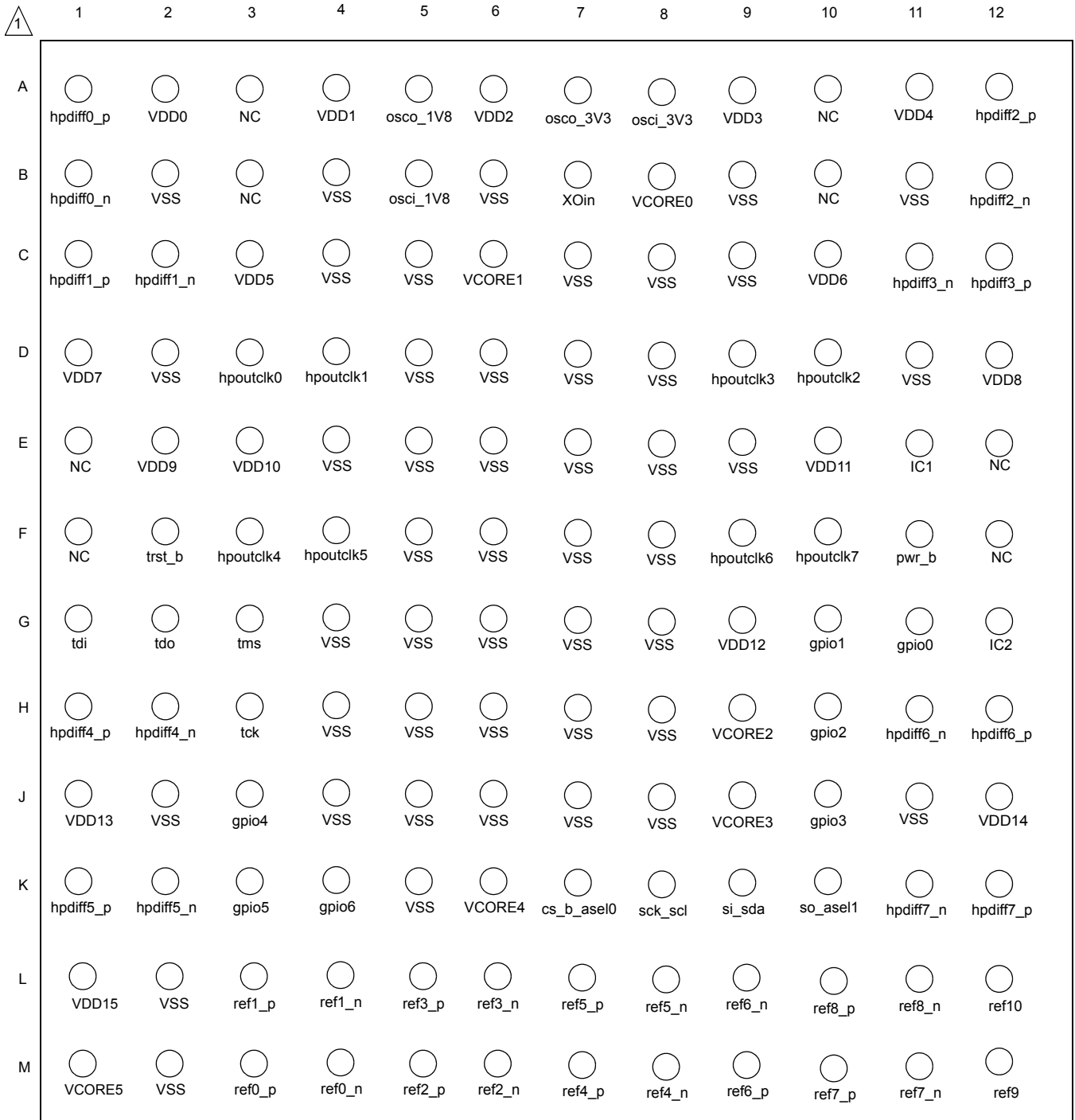
- SyncE/SONET/SDH Timing Cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fibre Channel, XAUI



**Figure 1 - Functional Block Diagram**

### 1.0 Pin Diagram

**TOP VIEW**



**1** - A1 corner is identified by metallized markings.

**Figure 2 - Package Description**



## 2.0 Pin Description

All device inputs and outputs are LVCMOS unless it is specifically stated to be differential. For the I/O column, there are digital inputs (I), digital outputs (O), analog inputs (A-I) and analog outputs (A-O).

Ball #	Name	I/O	Description
<b>Input Reference</b>			
M3 M4 L3 L4 M5 M6 L5 L6 M7 M8 L7 L8 M9 L9 M10 M11 L10 L11	ref0_p ref0_n ref1_p ref1_n ref2_p ref2_n ref3_p ref3_n ref4_p ref4_n ref5_p ref5_n ref6_p ref6_n ref7_p ref7_n ref8_p ref8_n	I	<p><b>Input References 0 to 8.</b> Input reference sources used for synchronization. The positive and negative pair of these inputs accepts a differential input signal. The refx_p input terminal accepts a CMOS input reference. These inputs can be used as an external feedback input.</p> <p>Maximum frequency limit on single ended inputs is 177.5 MHz, and 750 MHz on differential inputs.</p>
M12 L12	ref9 ref10	I	<p><b>Input References 9 and 10.</b> Input reference sources used for synchronization. These inputs are the same as inputs 0 to 8, but only single ended. These inputs can be used as an external feedback input.</p> <p>Maximum frequency limit is 177.5 MHz.</p>
<b>Output Clocks</b>			
D3 D4 D10 D9 F3 F4 F9 F10	hpoutclk0 hpoutclk1 hpoutclk2 hpoutclk3 hpoutclk4 hpoutclk5 hpoutclk6 hpoutclk7	O	<p><b>High Performance Output Clocks 0 to 7.</b> These outputs can be configured to provide any one of the single ended high performance clock outputs.</p> <p>Maximum frequency limit on single ended LVCMOS outputs is 177.5 MHz.</p>

**Table 1 - Pin Description**

Ball #	Name	I/O	Description
A1 B1 C1 C2 A12 B12 C12 C11 H1 H2 K1 K2 H12 H11 K12 K11	hpdiff0_p hpdiff0_n hpdiff1_p hpdiff1_n hpdiff2_p hpdiff2_n hpdiff3_p hpdiff3_n hpdiff4_p hpdiff4_n hpdiff5_p hpdiff5_n hpdiff6_p hpdiff6_n hpdiff7_p hpdiff7_n	O	<p><b>High Performance Differential Output Clocks 0 to 7 (LVPECL).</b> These outputs can be configured to provide any one of the available high performance differential output clocks.</p> <p>Maximum frequency limit on differential outputs is 750 MHz.</p>
<b>Control and Status</b>			
F11	pwr_b	I	<p><b>Power-on Reset.</b> A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The <b>pwr_b</b> pin should be held low for 2 ms after all power supplies are stabilized. This pin is internally pulled-up to <math>V_{DD}</math>. User can access device registers either 125 ms after <b>pwr_b</b> goes high, or after bit 7 in register at address 0x000 goes high (which can be determined by polling).</p>

**Table 1 - Pin Description (continued)**

Ball #	Name	I/O	Description
G11 G10 H10 J10 J3 K3 K4	gpio0 gpio1 gpio2 gpio3 gpio4 gpio5 gpio6	I/O	<p><b>General Purpose Input and Output pins.</b> These are general purpose I/O pins.</p> <p>Example GPIO functions include:</p> <ul style="list-style-type: none"> <li>• DPLL lock indicators</li> <li>• DPLL holdover indicators</li> <li>• Reference fail indicators</li> <li>• Reference select control or monitor</li> <li>• Differential output clock enable</li> <li>• High performance LVCMOS outputs enable</li> <li>• Host Interrupt Output to flag status changes</li> </ul> <p>All GPIO functions are listed in 5.2, “GPIO Configuration”.</p> <p>Pins 5:0 are internally pulled down to GND and pin 6 is internally pulled up to <math>V_{DD}</math>.</p> <p>Unused GPIO pins can be left unconnected.</p> <p>After power on reset, device GPIO[0, 1, 3] configure basic device function. GPIO3 sets I<sup>2</sup>C or SPI control mode, GPIO[1, 0] sets master clock rate selection. The GPIO[0, 1, 3] pins must be either pulled low or high with an external 1 k<math>\Omega</math> resistor for their assigned functions at reset; or they must be driven low or high for 125 ms after reset, and released and then used for normal GPIO functions.</p> <p>The GPIO4 pin must be either pulled low with an external 1 k<math>\Omega</math> resistor; or it must be driven low for 125 ms after reset, and then released and used for normal GPIO functions.</p> <p>GPIO[5, 6] are not used during power up.</p>
<b>Host Interface</b>			
K8	sck_scl	I/O	<p><b>Clock for Serial Interface.</b> Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I<sup>2</sup>C mode. As an input this pin is internally pulled up to <math>V_{DD}</math>.</p>
K9	si_sda	I/O	<p><b>Serial Interface Input.</b> The input serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when the host interface is configured for I<sup>2</sup>C mode. This pin is internally pulled up to <math>V_{DD}</math>.</p>
K10	so_ase1	I/O	<p><b>Serial Interface Output.</b> As an output, the serial stream holds the read data bits. This pin is also a part of the I<sup>2</sup>C address select when the host interface is configured for I<sup>2</sup>C mode.</p>
K7	cs_b_ase0	I	<p><b>Chip Select for Serial Interface.</b> As serial interface chip select, this is an active low signal. This pin is also a part of the I<sup>2</sup>C address select when the host interface is configured for I<sup>2</sup>C mode. This pin is internally pulled up to <math>V_{DD}</math>.</p>
<b>JTAG (IEEE 1149.1) and Test</b>			
G12	IC2	I	<p><b>Internal Connection.</b> Connect this pin to GND.</p>
E11	IC1	A-I/O	<p><b>Internal Connection.</b> Leave unconnected.</p>

**Table 1 - Pin Description (continued)**

Ball #	Name	I/O	Description
G2	tdo	O	<b>Test Serial Data Out.</b> JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G1	tdi	I	<b>Test Serial Data In.</b> JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to $V_{DD}$ . If this pin is not used then it should be left unconnected.
F2	trst_b	I	<b>Test Reset.</b> Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be held low or pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to $V_{DD}$ . If this pin is not used then it should be connected to GND.
H3	tck	I	<b>Test Clock.</b> Provides the clock for the JTAG test logic. This pin is internally pulled up to $V_{DD}$ . If this pin is not used then it should be connected to GND.
G3	tms	I	<b>Test Mode Select.</b> JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to $V_{DD}$ . If this pin is not used then it should be left unconnected.
<b>Master Clock</b>			
Note: The <b>osci_1V8/osco_1V8</b> pins are preferred to connect a crystal to the device. The <b>XOin</b> pin is preferred to connect a crystal oscillator (XO) to the device.			
A7	osco_3V3	A-O	<b>3.3V Crystal Master Clock Output.</b> For the alternative connection method for a crystal, the crystal is connected from this pin to <b>osci_3V3</b> . Not suitable for driving other devices. For clock oscillator operation or the use of a crystal between <b>osci_1V8</b> and <b>osco_1V8</b> , this pin should be left unconnected.
A8	osci_3V3	I	<b>3.3V Crystal Master Clock Input.</b> For the alternative connection method for a crystal, the crystal is connected from this pin to <b>osco_3V3</b> . For clock oscillator operation or the use of a crystal between <b>osci_1V8</b> and <b>osco_1V8</b> , this pin should be grounded.
A5	osco_1V8	A-O	<b>1.8V Crystal Master Clock Output.</b> For the primary connection method for a crystal, the crystal is connected from this pin to <b>osci_1V8</b> . Not suitable for driving other devices. For clock oscillator operation or the use of a crystal between <b>osci_3V3</b> and <b>osco_3V3</b> , this pin should be left unconnected.
B5	osci_1V8	I	<b>1.8V Crystal Master Clock Input.</b> For the primary connection method for a crystal, the crystal is connected from this pin to <b>osco_1V8</b> . For clock oscillator operation or the use of a crystal between <b>osci_3V3</b> and <b>osco_3V3</b> , this pin should be grounded.
B7	XOin	I	<b>XO Master Clock Output.</b> For clock oscillator operation, this pin is connected to the output of the oscillator. For crystal operation using either method, this pin should be grounded.
<b>Power and Ground</b>			

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
B8 C6 H9 J9 K6 M1	V <sub>CORE0</sub> V <sub>CORE1</sub> V <sub>CORE2</sub> V <sub>CORE3</sub> V <sub>CORE4</sub> V <sub>CORE5</sub>		<p><b>Positive Supply Voltage.</b> +1.8V<sub>DC</sub> nominal.</p> <p>These pins should not be connected together on the board. Please refer to ZLAN-327 for recommendations</p>
A2 A4 A6 A9 A11 C3 C10 D1 D12 E2 E3 E10 G9 J1 J12 L1	V <sub>DD0</sub> V <sub>DD1</sub> V <sub>DD2</sub> V <sub>DD3</sub> V <sub>DD4</sub> V <sub>DD5</sub> V <sub>DD6</sub> V <sub>DD7</sub> V <sub>DD8</sub> V <sub>DD9</sub> V <sub>DD10</sub> V <sub>DD11</sub> V <sub>DD12</sub> V <sub>DD13</sub> V <sub>DD14</sub> V <sub>DD15</sub>		<p><b>Positive Supply Voltage.</b> +3.3V<sub>DC</sub> nominal.</p> <p>These pins should not be connected together on the board. Please refer to ZLAN-327 for recommendations</p>

**Table 1 - Pin Description (continued)**



Ball #	Name	I/O	Description
B2 B4 B6 B9 B11 C4 C5 C7 C8 C9 D2 D11 E4 E9 G4 H4 H5 H6 H7 H8 J2 J4 J5 J6 J7 J8 J11 K5 L2 M2 D5 D6 D7 D8 E5 E6 E7 E8 F5 F6 F7 F8 G5 G6 G7 G8	V <sub>SS</sub>		<b>Ground. 0 Volts.</b>

**Table 1 - Pin Description (continued)**

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Ball #	Name	I/O	Description
A3 A10 B3 B10 E1 E12 F1 F12	NC		<b>No Connect.</b> These pins should be left open.

**Table 1 - Pin Description (continued)**

### 3.0 Mechanical Drawing

**NOTES :**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. SOLDER BALL POSITION DESIGNATION PER JE5D 95-1, SPP-010.
3. THIS DIMENSION INCLUDES STAND-OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.57	1.76	1.95	.062	.069	.076
A1	0.4	0.5	0.6	.016	.020	.024
A2		0.56			.022	
A3		0.70			.028	
b	0.5	0.6	0.7	.020	.024	.028
D	12.90	13.00	13.10	.508	.512	.516
D1		11.00			.433	
E	12.90	13.00	13.10	.508	.512	.516
E1		11.00			.433	
e		1.00			.039	

**Microsemi Corp**

TITLE: 144 LBGGA PACKAGE OUTLINE  
BODY SIZE 0.3 X 1.3 X1.76MM MAX  
PITCH: 1.0MM

DATE: 22-0017	REV: 4
REV: 84-06-25-225	SIZE: A4
SHEET: 1	OF: 1

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