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ZL30169

Tiny 3-Input, 3-Output
Clock Translator for OTN

Product Brief

June 2014

Features

- **Input clocks**
  - Three inputs, two differential/CMOS, one CMOS
  - Any input frequency from 1kHz to 1250MHz (1kHz to 300MHz for CMOS)
  - Inputs continually monitored for activity and frequency accuracy
  - Automatic or manual reference switching

- **Low-bandwidth DPLL**
  - Programmable bandwidth, 14Hz to 500Hz
  - Attenuates jitter up to several UI
  - Free-run or holdover on loss of all inputs
  - Hitless reference switching
  - High-resolution holdover averaging
  - Digitally controlled phase adjustment

- **Low-jitter fractional-N APLL and 3 outputs**
  - Any output frequency from <1Hz to 1035MHz
  - High-resolution fractional frequency conversion with 0ppm error
  - Easy-to-configure, encapsulated design requires no external VCXO or loop filter components
  - Each output has independent dividers
  - Output jitter is typically 0.16 to 0.28ps RMS (12kHz-20MHz integration band)
  - Outputs are CML or 2xCMOS, can interface to LVDS, LVPECL, HSTL, SSTL and HCSL

Ordering Information

ZL30169LDG1	32 Pin QFN	Trays	
ZL30169LDF1	32 Pin QFN	Tape and Reel	

Matte Tin

Package size: 5 x 5 mm

-40°C to +85°C

- In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)
- Per-output supply pin with CMOS output voltages from 1.5V to 3.3V
- Precise output alignment circuitry and per-output phase adjustment
- Per-output enable/disable and glitchless start/stop (stop high or low)

- **General Features**
  - Automatic self-configuration at power-up from internal EEPROM; up to four configurations pin-selectable
  - Numerically controlled oscillator mode
  - Zero-delay mode with external feedback
  - SPI or I2C processor Interface
  - Easy-to-use evaluation software

Applications

- Telecom OTN and FEC frequency conversion
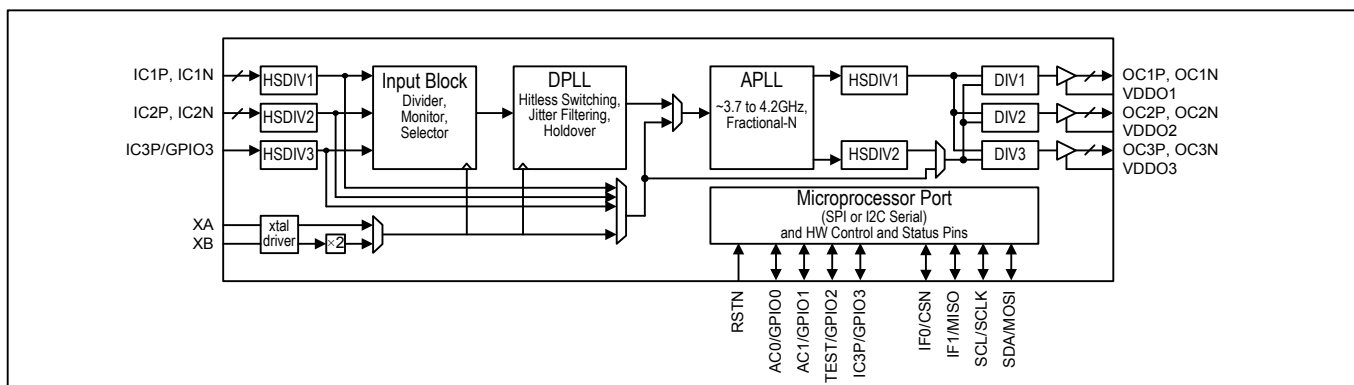- Frequency conversion and frequency synthesis in a wide variety of equipment types

Figure 1 - Functional Block Diagram
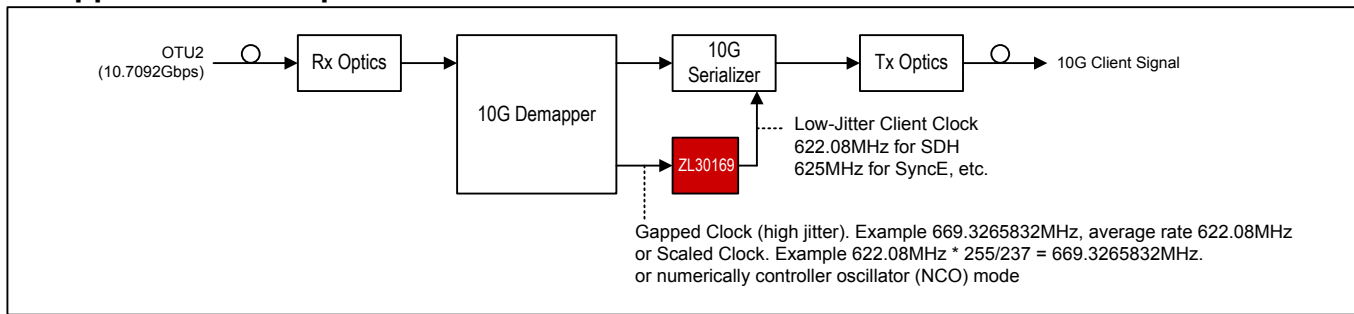
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1. Application Examples

Figure 2 - OTU2 Demapper Clock Translation and/or Jitter Attenuation

2. Detailed Features

2.1 Input Block Features

- Three input clocks, two differential or single-ended, one single-ended
- Input clocks can be any frequency from 1kHz up to 1250MHz (differential) or 300MHz (single-ended)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the selected reference after a few missing clock cycles
- Frequency measurement and monitoring with 1ppm resolution and accept/reject hysteresis
- Optional input clock invalidation on GPIO assertion to react to LOS signals from PHYs

2.2 DPLL Features

- Very high-resolution DPLL architecture
- State machine automatically transitions between tracking and freerun/holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 14Hz to 500Hz
- Less than 0.1dB gain peaking
- Programmable phase-slope limiting
- Programmable frequency rate-of-change limiting
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching with <200ps output clock phase transient
- Output phase adjustment in 10ps steps
- High-resolution frequency and phase measurement
- Fast detection of input clock failure and transition to holdover mode
- Holdover frequency averaging with programmable averaging time and delay time
- Better than 100ppb initial holdover accuracy

2.3 APLL Features

- Very high-resolution fractional scaling (i.e. non-integer multiplication)
- Any-to-any frequency conversion with 0ppm error
- Two high-speed dividers (integers 4 to 15, half divides 4.5 to 7.5)
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Bypass mode supports system testing

2.4 Output Clock Features

- Three low-jitter output clocks
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1035MHz (250MHz max for CMOS outputs)
- Output jitter is typically 0.16 to 0.28ps RMS (12kHz to 20MHz)

- In CMOS mode, an additional divider allows the OCxN pin to be an integer divisor of the OCxP pin (example: OC3P 125MHz, OC3N 25MHz)
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL and CMOS components
- Supported telecom frequencies include SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Sophisticated output-to-output phase alignment
- Per-output phase adjustment with high resolution and unlimited range
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

2.5 General Features

- SPI or I^{2}C serial microprocessor interface
- Automatic self-configuration at power-up from internal EEPROM memory; pin control to specify one of four stored configurations
- Numerically controlled oscillator (NCO) mode allows system software to steer DPLL frequency with resolution better than 0.01ppb
- Zero-delay buffer configuration using an external feedback path
- Four general-purpose I/O pins each with many possible status and control options
- Input and output frame sync signals
- Can operate as DPLL+APLL for jitter filtering and hitless switching or as APLL only
- Local oscillator can be fundamental-mode crystal or low-cost XO
- Internal compensation for local oscillator frequency error

2.6 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the ZL30169 quick and easy
- Generates configuration scripts to be stored in internal EEPROM
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without a ZL30169 evaluation board