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ZL30182

Dual-Channel Any-to-Any Clock Rate Translator

Product Brief

September 2015

Ordering Information

ZL30182LFG7	64 Pin LGA	Trays
ZL30182LFF7	64 Pin LGA	Tape and Reel

Ni Au

Package size: 5 x 10 mm

-40°C to +85°C

Features

- **Two Independent Channels**
- **Three Input Clocks Per Channel**
  - Three inputs, two differential/CMOS, one CMOS
  - Any input frequency from 1kHz to 1250MHz (1kHz to 300MHz for CMOS)
  - Inputs continually monitored for activity and frequency accuracy
  - Automatic or manual reference switching
- **Low-Bandwidth DPLL Per Channel**
  - Programmable bandwidth, 5Hz to 500Hz
  - Attenuates jitter up to several UI
  - Freerun or holdover on loss of all inputs
  - Hitless reference switching
  - High-resolution holdover averaging
  - Digitally controlled phase adjustment
- **Low-Jitter Fractional-N APLL and 3 Outputs Per Channel**
  - Any output frequency from <1Hz to 1035MHz
  - High-resolution fractional frequency conversion with 0ppm error
  - Easy-to-configure, encapsulated design requires no external VCXO or loop filter components
  - Each output has independent dividers
  - Output jitter is typically 0.16 to 0.28ps RMS (12kHz-20MHz integration band)
  - Outputs are CML or 2xCMOS, can interface to LVDS, LVPECL, HSTL, SSTL and HCSL
  - In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)
  - Per-output supply pin with CMOS output voltages from 1.5V to 3.3V
  - Precise output alignment circuitry and per-output phase adjustment
  - Per-output enable/disable and glitchless start/stop (stop high or low)
- **General Features**
  - Automatic self-configuration at power-up from internal EEPROM; up to four configurations pin-selectable
  - Numerically controlled oscillator mode
  - Zero-delay mode with external feedback
  - SPI or I^2C processor Interface
  - Easy-to-use evaluation software

Applications

- Telecom OTN and SONET/SDH/SyncE cards
- Frequency conversion and jitter attenuation in a wide variety of equipment types

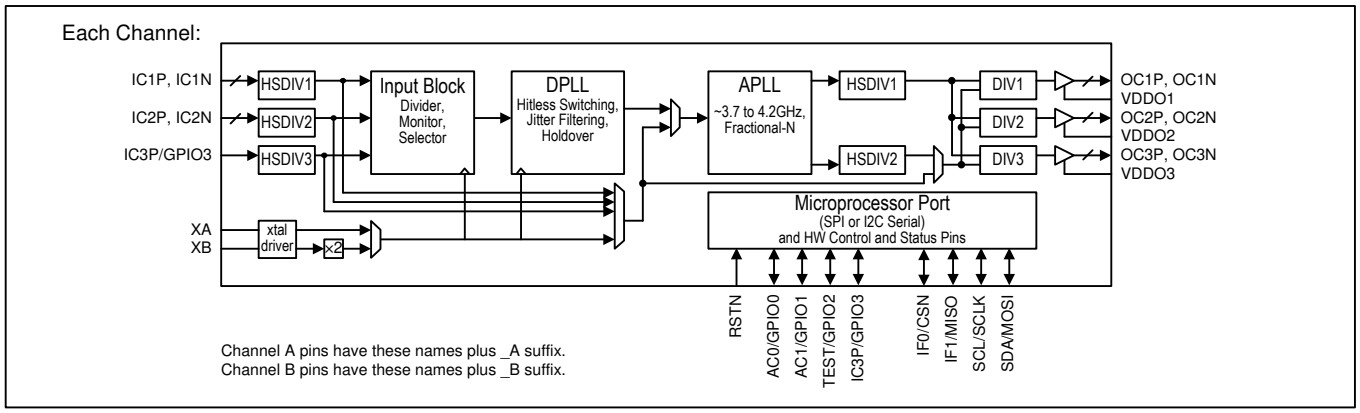


Figure 1 - Functional Block Diagram

1. Application Examples

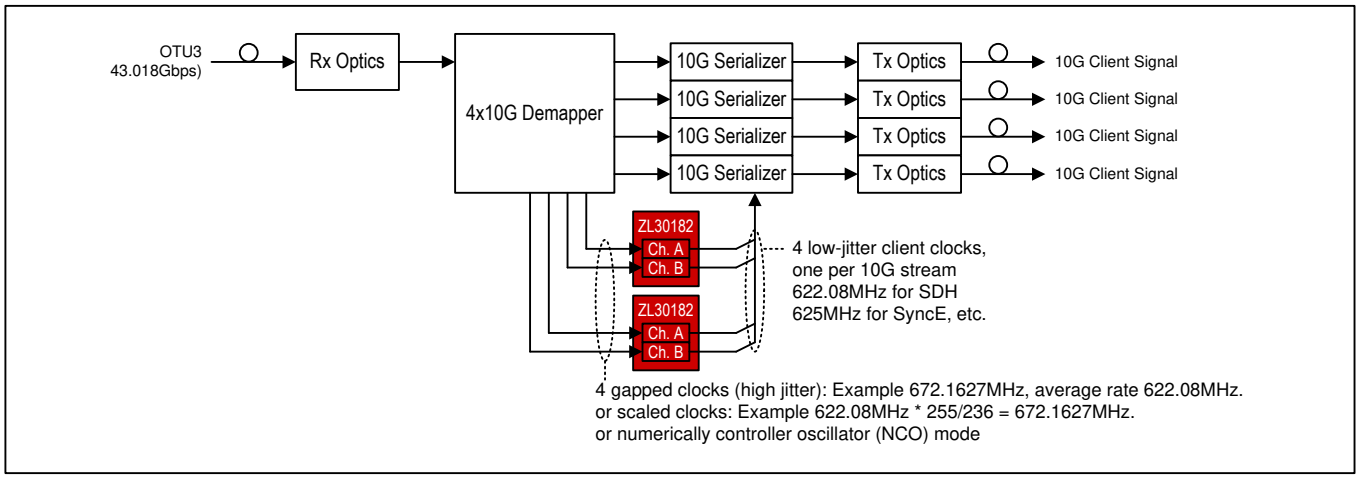


Figure 2 – OTU3 Demux/Demapper Clock Translation and/or Jitter Attenuation

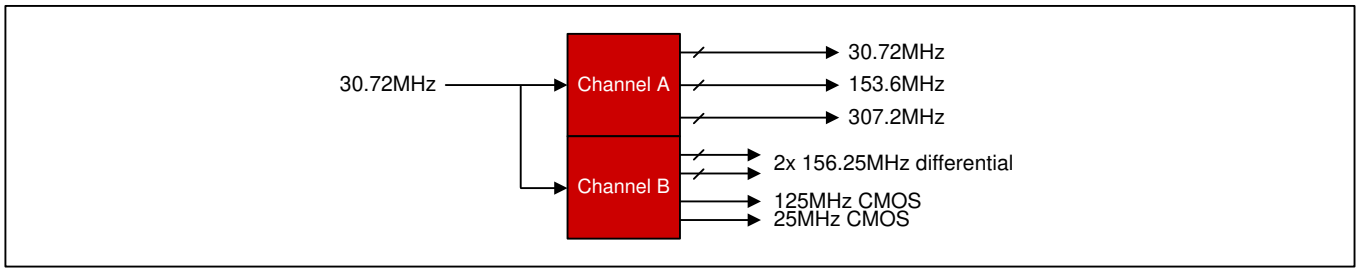


Figure 3 – Base Station Frequency Conversion with Jitter Attenuation

2. Detailed Features

2.1 Input Block Features

- Three input clocks per channel, two differential or single-ended, one single-ended
- Input clocks can be any frequency from 1kHz up to 1250MHz (differential) or 300MHz (single-ended)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the input after a few missing clock cycles
- Frequency measurement and monitoring with 1ppm resolution and accept/reject hysteresis
- Optional input clock invalidation on GPIO assertion to react to LOS signals from PHYs

2.2 DPLL Features

- One DPLL per channel
- Very high-resolution DPLL architecture
- State machine automatically transitions between tracking and freerun/holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 5Hz to 500Hz
- Less than 0.1dB gain peaking
- Programmable damping factor to balance lock time with peaking
- Programmable phase-slope limiting
- Programmable frequency rate-of-change limiting
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching with <200ps output clock phase transient
- Output phase adjustment in 10ps steps

- High-resolution frequency and phase measurement
- Fast detection of input clock failure and transition to holdover mode
- Holdover frequency averaging with programmable averaging time and delay time
- Better than 50ppb initial holdover accuracy

2.3 APLL Features

- APLL with very high-resolution fractional scaling (i.e. non-integer) per channel
- Any-to-any frequency conversion with 0ppm error
- Two high-speed dividers (integers 4 to 15, half divides 4.5 to 7.5)
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Bypass mode supports system testing

2.4 Output Clock Features

- Three low-jitter output clocks per channel
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1035MHz (250MHz max for CMOS and HSTL outputs)
- Output jitter is typically 0.16 to 0.28ps RMS (12kHz to 20MHz)
- In CMOS mode, an additional divider allows the OCxN pin to be an integer divisor of the OCxP pin (example: OC3P 125MHz, OC3N 25MHz)
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Can produce PCIe clocks (PCIe gen. 1, 2 and 3)
- Sophisticated output-to-output phase alignment
- Per-output phase adjustment with high resolution and unlimited range
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

2.5 General Features

- SPI or I^2C serial microprocessor interface per channel
- Automatic self-configuration at power-up from internal EEPROM memory; pin control to specify one of four stored configurations
- Each channel can be configured for numerically controlled oscillator (NCO) mode, which allows system software to steer frequency with resolution better than 0.01ppb
- Zero-delay buffer configuration using an external feedback path
- Four general-purpose I/O pins per channel each with many possible status and control options
- Output frame sync signals
- Each channel's local oscillator can be fundamental-mode crystal or low-cost XO
- Internal compensation for local oscillator frequency error

2.6 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the ZL30182 quick and easy
- Generates configuration scripts to be stored in internal EEPROM
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without a ZL30182 evaluation board

3. Pin Diagram

The device is packaged in a 5x10mm 64-pin LGA.

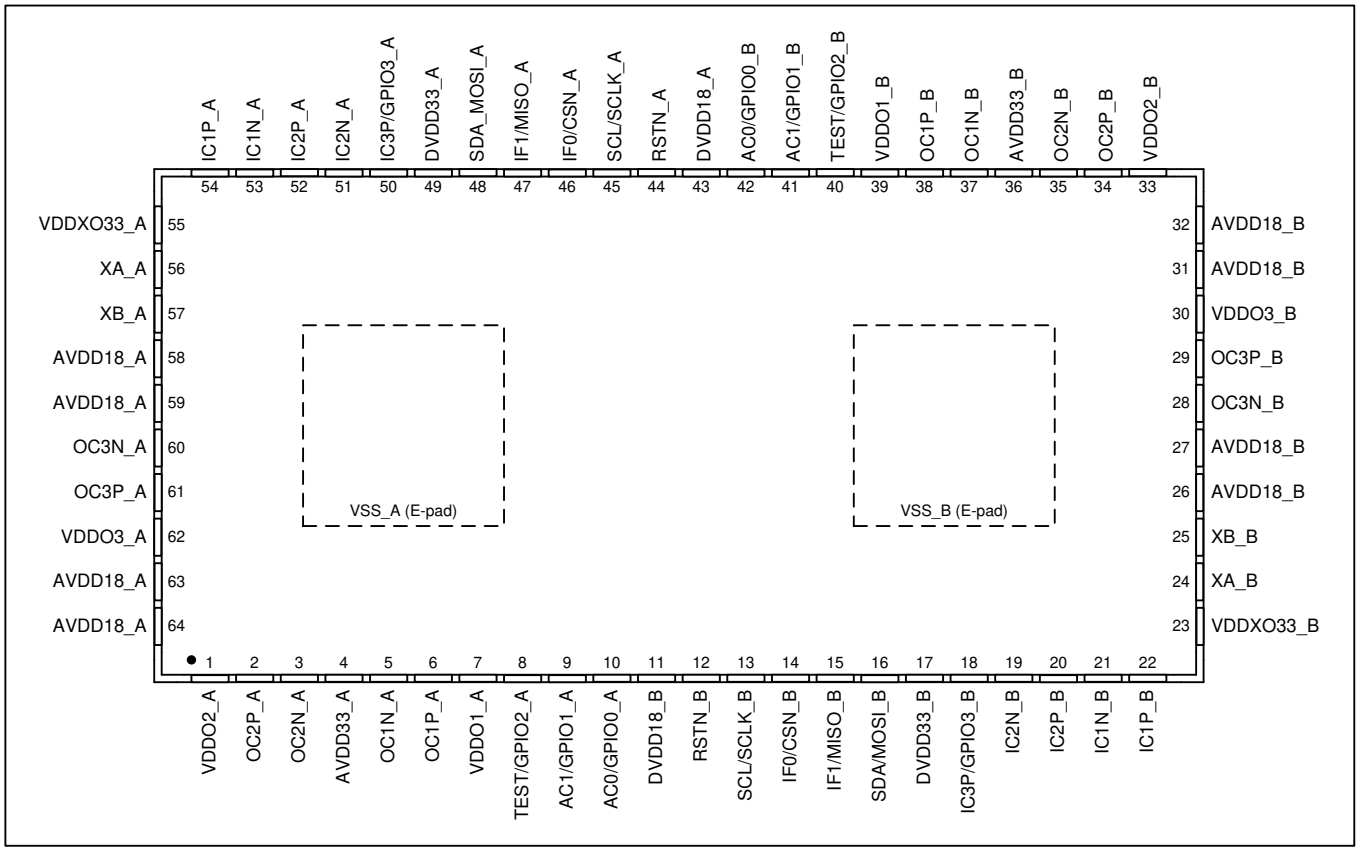
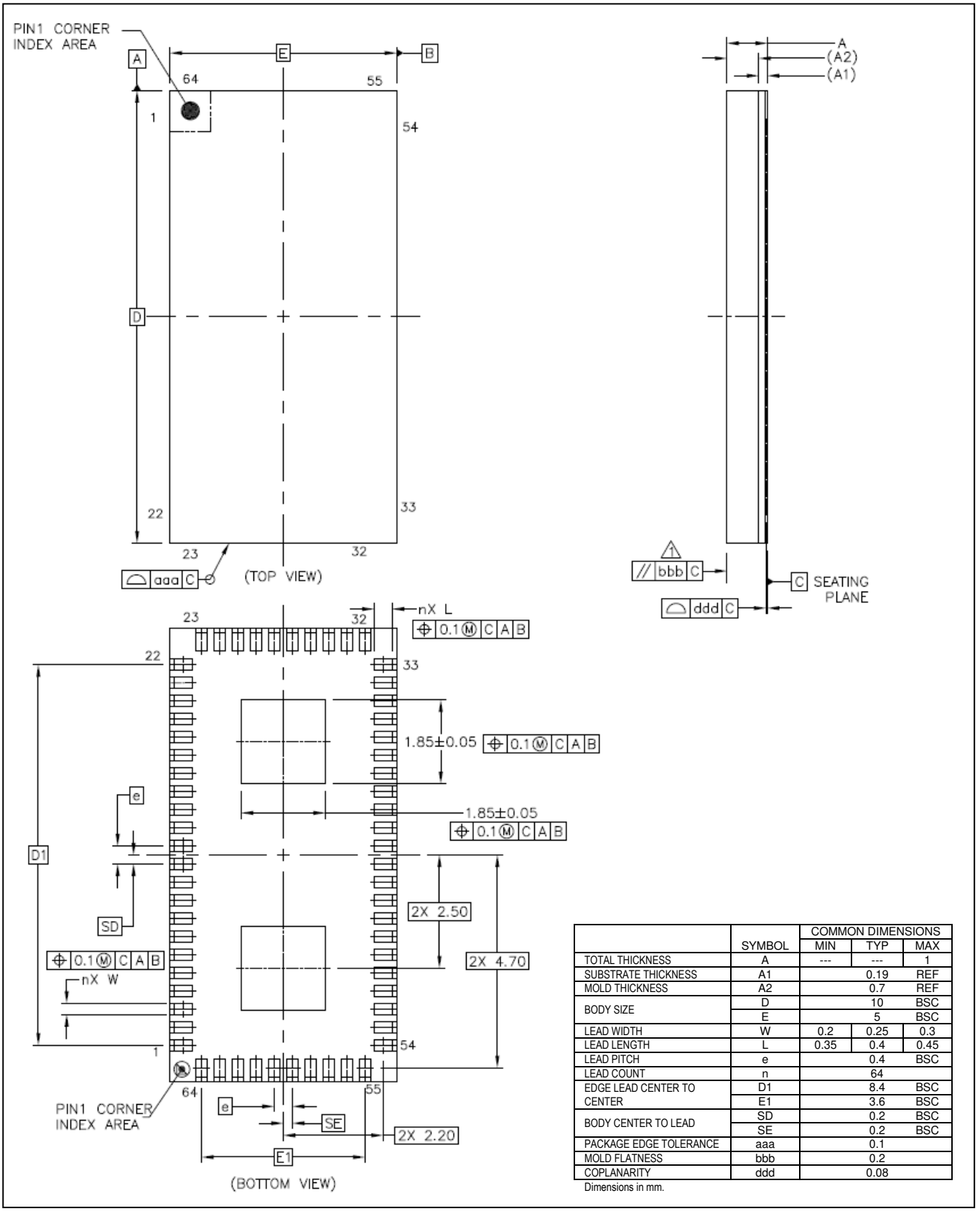


Figure 4 - Pin Diagram

4. Mechanical Drawing



	SYMBOL	COMMON DIMENSIONS		
		MIN	TYP	MAX
TOTAL THICKNESS	A	---	---	1
SUBSTRATE THICKNESS	A1		0.19	REF
MOLD THICKNESS	A2		0.7	REF
BODY SIZE	D		10	BSC
	E		5	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		64	
EDGE LEAD CENTER TO CENTER	D1		8.4	BSC
	E1		3.6	BSC
BODY CENTER TO LEAD	SD		0.2	BSC
	SE		0.2	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	

Dimensions in mm.

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