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ZL30230
Four Channel Universal Clock Generator

Data Sheet

March 2015

Features

- Generates clock signals at power-up per user defined custom OTP (One Time Programmable) configuration
- Dynamically configurable via SPI/I2C interface and volatile configuration registers
- Four independently programmable clock generators output any clock rate from 1 kHz to 750 MHz (precision) / 350 MHz (general purpose)
- Precision clock generators output clocks with jitter below 0.7 ps RMS for 10 G PHYs
- General purpose clock generators output a wide range of digital bus clocks
- Operates from a single crystal resonator, clock oscillator or voltage controlled oscillator
- Supports programmable frequency offsets for clock margining; or for use as a digitally controlled oscillator
- Eight LVPECL outputs; max rate 750 MHz
- Four LVCMOS outputs; max rate 177.5 MHz

Ordering Information

ZL30230GGG2 100 Pin LBGA* 11mmx11mm Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Eight outputs configurable as LVCMOS at 3.3/2.5/1.8 or 1.5 V, max rate160 MHz; or LVDS/LVPECL/HCSL, max rate 350 MHz

Applications

- Timing for NPUs, FPGAs, Ethernet switches and PCIe switches
- Timing for 10 Gigabit CDRs, Rapid-IO, PCIe, Serial MII, Star Fabric, Fibre Channel, XAUI
- Processor clock, Processor bus clock, SDRAM clock, DDR clock

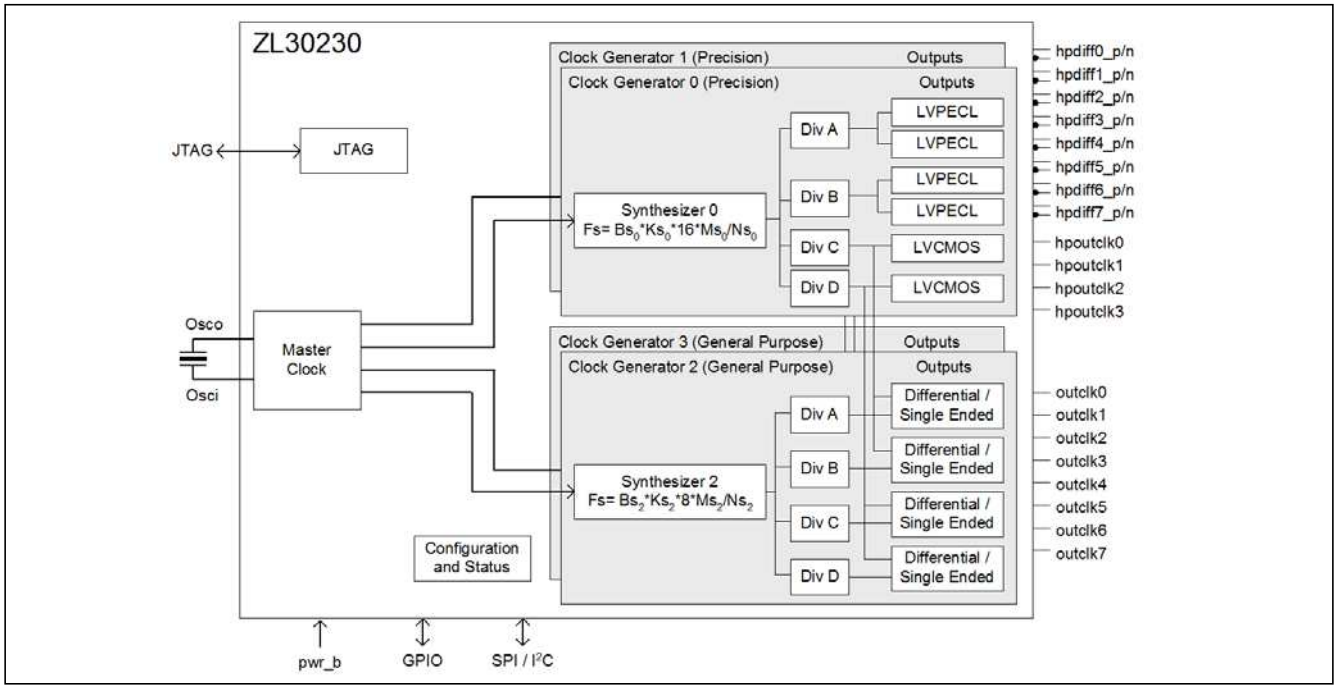

Figure 1 - Functional Block Diagram

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Change Summary

Below are the changes from the June 2012 issue to the March 2015 issue.

Page	Item	Change
1	Ordering Information	Removed ZL30230GGG (leaded version) from the ordering information
23	Custom OTP Configuration	Removed reference to ZLAN-301
118	13.0, “Package Markings“	Added section 13 for package markings

Below are the changes from the January 2012 issue to the June 2012 issue.

Page	Item	Change
36 and 91	Register 0xC6 - Chip_revision_2	Updated chip_revision to 0x03
111	Output to output alignment	Updated limits for $t_{OUT2OUTD}$ to +/- 1 ns

Below are the changes from the December 2011 issue to the January 2012 issue.

Page	Item	Change
31	Procedure for writing registers	Added a new procedure to update registers
32	Reading from Sticky Read registers	Updated Sticky read Procedure
32	Time between two write accesses to the same register	Changed wait time from 200ms to 8ms, added 0x0D as register not requiring wait time
39	Register 0x00 - id_reg	Updated chip_revision bits
39	Register 0x0D - Sticky_r_lock	Updated Description
36, 91	Register 0xC6 - Chip_revision_2	Added register 0xC6

Below are the changes from the July 2011 issue to the December 2011 issue.

Page	Item	Change
32	Reading from Sticky Read registers	Updated Sticky read Procedure
39	Register 0x00 - id_reg	updated ready_indication description
39	Register 0x0D - sticky_r_lock	added register
87	Register 0xB7 - synth2_stop_clock	Bits[3:2] - changed outclk2 to outclk1 Bits[5:4] - changed outclk3 to outclk2
103	Register 0xF7 - spurs_suppression	updated spurs_suppression description
117	Mechanical Drawing	repalced drawing to reflect correct package description

Below are the changes from the June 2011 issue to the July 2011 issue.

Page	Item	Change
1	Feature	OTP feature is added
1, 9,14, 16, 23, 23, 111	All items related the maximum rate of differential output clocks	The maximum rate is updated from 720 MHz to 750MHz
9, 10, 20, 21, 27, 39	All items related waiting time after pwr_b pin goes high during reset procedure	Waiting time after pwr_b pin goes high is changed from 30 ms to 50 ms
14	Section 4.0	Updated for OTP feature
23	Section 5.0	• Section 5.1, 5.1.1, 5.1.2, 5.1.3 and 5.1.4 are updated for three configuration methods:Default configuration, OTP configuration, and SPI/I2C configuration • Original section 5.1.1, 5.1.2, 5.1.3, and 5.1.4 are changed to section 5.2, 5.3, 5.4, and 5.5
31	Section 7.0	For page_register at address 0x7F, there is no waiting time required between two write accesses.
33	Table-5	• Table description is updated for OTP feature • Register 0x01, 0x0E and 0x0F are added • Heading of first column is changed from “Page_Addr” to “Reg_Addr"
39	Section 8.0	Detailed description for new register 0x01, 0x0E, and 0x0F are added
55	Detailed Register Map	"Page_Address" is changed to "Register_Address" for registers which addresses are from 0x80 to 0x91
56	Register synth0_post_div_C	Bit[15:0]: note added for odd post divider
58	Register synth0_post_div_D	Bit[15:0]: note added for odd post divider
61	Register synth1_post_div_C	Bit[15:0]: note added for odd post divider
63	Register synth1_post_div_D	Bit[15:0]: note added for odd post divider
105	DC Electrical Characteristics -Power Core	• "Power for Each Synthesis Engine” is changed to “Current for Each Synthesis Engine” • “PSYN” is changed to “ISYN”
108	DC Electrical Characteristics - High Performance Outputs	Note added for differential output voltage when differential frequency is higher than 720MHz

Page	Item	Change
105	DC Electrical Characteristics	All "AV_{DD-IO}" symbols are replaced with "AV_{DD}"
115	Output Clocks Jitter Generation	Jitter measurement filter for 77.76MHz is changed from "12kHz-5MHz" to "12kHz-20MHz"
116	Section 11.0	Note added for Tjmax

Below are the changes from the January 2011 issue to the June 2011 issue

Page	Item	Change
1	Ordering Information	Corrected package description in ordering information to LBGA.
115	Section 10.1	Section name was renamed to "Output Clocks RMS Jitter Generation".
116	Section 10.2	Table 12 was created for cycle-to-cycle jitter generation.
110	Section 12.0	Replaced drawing to reflect correct package description.

Below are the changes from the November 2010 issue to the January 2011 issue.

Page	Item	Change
6	Figure 2	Names of pin B5, B6, H5, and H6 are changed from AVcore to Vcore
10	Table 1	Names of pin B5, B6, H5, and H6 are changed from AVcore to Vcore, and they are merged to the same entry with pin D5, G5, and G6. Layout application note is referred
25	6.1 Serial Peripheral Interface	SPI burst mode operation description is added
27	Figure 17	Example of a Burst Mode Operation is added
98	Table - Recommended Operating Conditions	Row 2, AVcore is removed from the "Sym" column
104	Table - AC Electrical Characteristics* - Outputs	Row 3, clock duty cycle is changed from "43%-57%" to "45%-55%"
104	Table - AC Electrical Characteristics* - Outputs	Row 4, note "From 0.2AVDD-IO to 0.8AVDD-IO" is removed

1.0 Pin Diagram

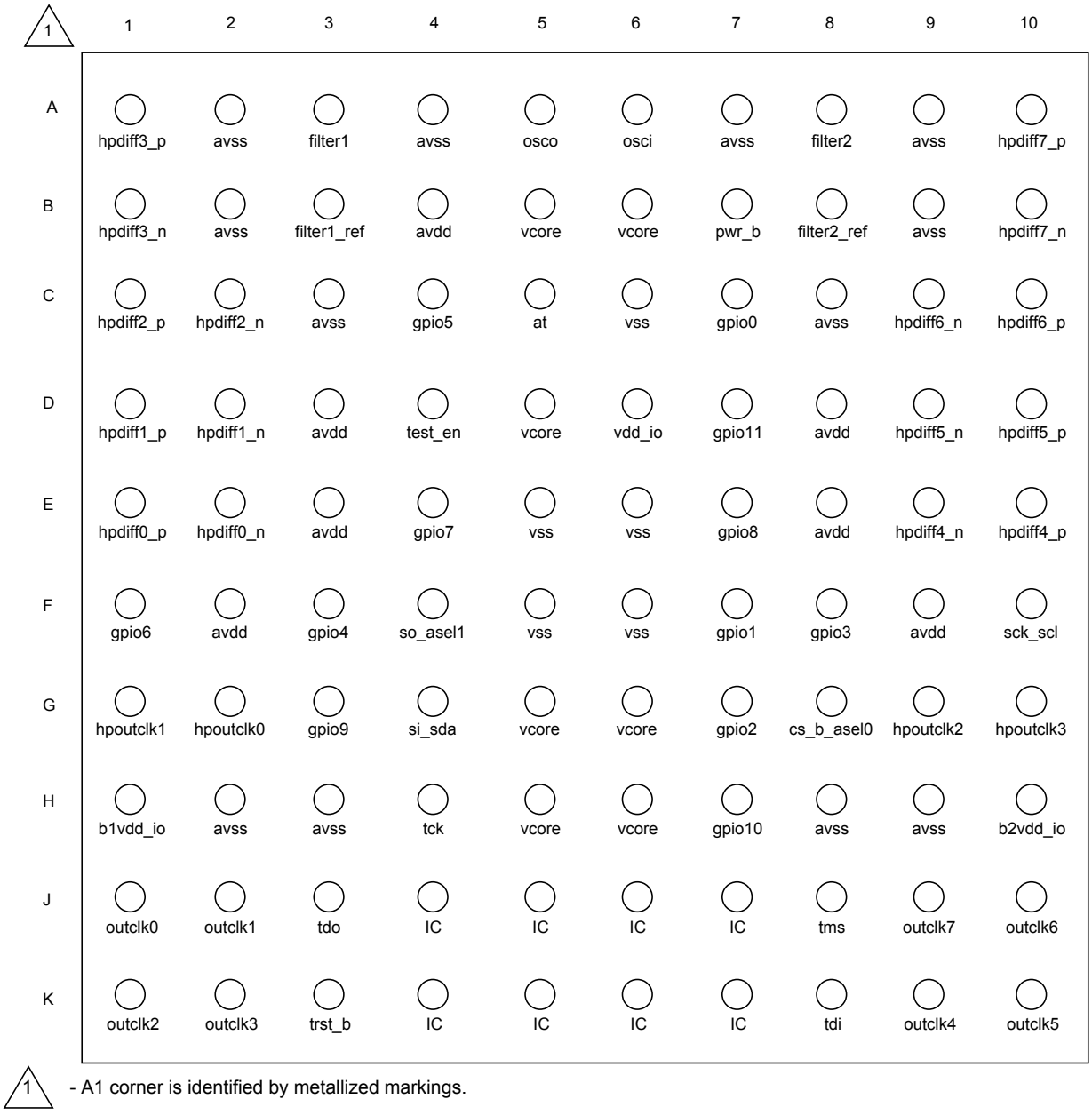

Figure 2 - Package Description

2.0 Pin Description

All device inputs and output are LVCMOS unless it was specifically stated to be differential.

Ball #	Name	I/O	Description
Output Clocks			
J1 J2 K1 K2 K9 K10 J10 J9	outclk0 outclk1 outclk2 outclk3 outclk4 outclk5 outclk6 outclk7	O	**Output Clock 0 to 7.** Configurable output clocks. These can be configured as single ended or differential (0&1, 2&3, 4&5, 6&7) Maximum frequency limit on single ended LVCMOS outputs is 160 MHz, and 350 MHz on differential outputs.
G2 G1 G9 G10	hpoutclk0 hpoutclk1 hpoutclk2 hpoutclk3	O	**High Performance Output Clock 0 to 3.** This output can be configured to provide any one of the single ended high performance clock outputs. Maximum frequency limit on single ended LVCMOS outputs is 177.5 MHz
E1 E2 D1 D2 C1 C2 A1 B1 E10 E9 D10 D9 C10 C9 A10 B10	hpdiff0_p hpdiff0_n hpdiff1_p hpdiff1_n hpdiff2_p hpdiff2_n hpdiff3_p hpdif3_n hpdiff4_p hpdiff4_n hpdiff5_p hpdiff5_n hpdiff6_p hpdiff6_n hpdiff7_p hpdif7_n	O	**High Performance Differential Output Clock 0 to 7 (LVPECL).** This output can be configured to provide any one of the available high performance differential output clocks. Maximum frequency limit on differential outputs is 750 MHz
Control and Status			
B7	pwr_b	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The pwr_b pin should be held low for 2 ms. Following a reset, the input reference source and output clocks are phase aligned. This pin is internally pulled-up to V_{DD}. **User can access device registers either 50 ms after pwr_b goes high, or after bit 7 in register at address 0x00 goes high which can be determined by polling the register at address 0x00.**

Table 1 - Pin Description

Ball #	Name	I/O	Description
C7 F7 G7 F8 F3 C4 F1 E4 E7 G3 H7 D7	gpio0 gpio1 gpio2 gpio3 gpio4 gpio5 gpio6 gpio7 gpio8 gpio9 gpio10 gpio11	I/O	**General Purpose Input and Output pins.** These are general purpose pins managed by the internal processor based on device configuration. Other status and control pins could be muxed to become part of the available GPIO pins. Recommended usage of GPIO include: • Differential output clock enable (per output or as a bank of 2 or 4 outputs) • High performance LVCMOS outputs enable • Microport interface protocol I2C or SPI • Master Clock frequency rate Pins 5:0 are internally pulled down to GND and pins 11:6 are internally pulled up to V_{DD}. If not used GPIO can be kept unconnected. **After power on reset, device GPIO[0,1,3,4,5] configure some of device basic functions, GPIO[3] set I2C or SPI control mode, GPIO[1,0] set master clock rate selection. The GPIO[0,1,3] pins must be either pulled low or high with an external 1 KΩ resistor as needed for their assigned functions at reset; or they must be driven low or high for 50 ms after reset, and released and used for normal GPIO functions.** **The GPIO[4,5] pins must be either pulled low with external 1KΩ resistors; or they must be driven low for 50 ms after reset, and then released and used for normal GPIO functions.**
Host Interface			
F10	sck_scl	I/O	**Clock for Serial Interface.** Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I2C mode. As an input this pin is internally pulled up to V_{DD}.
G4	si_sda	I/O	**Serial Interface Input.** Serial interface input stream. The serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when host interface is configured for I2C mode. This pin is internally pulled up to V_{DD}.
F4	so_asel1	I/O	**Serial Interface Output.** Serial interface output stream. As an output the serial stream holds the read data bits. This pin is also the I2C address select when host interface is configured for I2C mode.
G8	cs_b_asel0	I	**Chip Select for Serial Interface.** Serial interface chip select, this is an active low signal. This pin is also the I2C address select when host interface is configured for I2C mode.This pin is internally pulled up to V_{DD}.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
APLL Loop Filter			
A3	filter1	A	**External Analog PLL1 Loop Filter terminal.**
B3	filter1_ref	A	**Analog PLL1 External Loop Filter Reference.**
A8	filter2	A	**External Analog PLL2 Loop Filter terminal.**
B8	filter2_ref	A	**Analog PLL2 External Loop Filter Reference.**
JTAG (IEEE 1149.1) and Test			
D4	test_en	I	**Test Mode Enable.** A logic high at this pin enables device test modes. This pin is internally pulled down to GND. Connect this pin to GND.
C5	at	A-I/O	**Analog PLL Test.** Test pin for analog PLL.
J3	tdo	O	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
K8	tdi	I	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
K3	trst_b	I	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to VDD. If this pin is not used then it should be connected to GND.
H4	tck	I	**Test Clock.** Provides the clock to the JTAG test logic. This pin is internally pulled up to V_{DD}. This pin is internally pulled up to VDD. If this pin is not used then it should be connected to GND.
J8	tms	I	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
A5	osco	A-O	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osci. Not suitable for driving other devices. For clock oscillator operation, this pin is left unconnected.
A6	osci	I	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osco. For clock oscillator operation, this pin is connected to a clock source.
Miscellaneous			
J4 K4 J5 K5 K6 J6 K7 J7	IC		**Internal Connect.** Connect to GND.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
Power and Ground			
D6	V_{DD-IO}		**Positive Supply Voltage IO.** 3.3V_{DC} nominal.
H1	B1V_{DD-IO}		**Bank 1 Positive Supply Voltage IO.** Output group specific +3.3/2.5/1.8/1.5V_{DC} nominal.
H10	B2V_{DD-IO}		**Bank 2 Positive Supply Voltage IO.** Output group specific +3.3/2.5/1.8/1.5V_{DC} nominal.
B5 B6 D5 G5 G6 H5 H6	V_{CORE}		**Positive Supply Voltage.** +1.8V_{DC} nominal. These pins should not be connected together on the board. Please refer to ZLAN-269 for recommendations
B4 D3 D8 E3 E8 F2 F9	AV_{DD}		**Positive Analog Supply Voltage.** +3.3V_{DC} nominal.
C6 E5 E6 F5 F6	V_{SS}		**Ground.** 0 Volts.
A2 A4 A7 A9 B2 B9 C3 C8 H2 H3 H8 H9	AV_{SS}		**Analog Ground.** 0 Volts.

Table 1 - Pin Description (continued)

3.0 Application Example

The device has multiple independent clock synthesizers, all locked to the external xtal or oscillator. The device will generate all the clocks that drive the different components on the PCB.

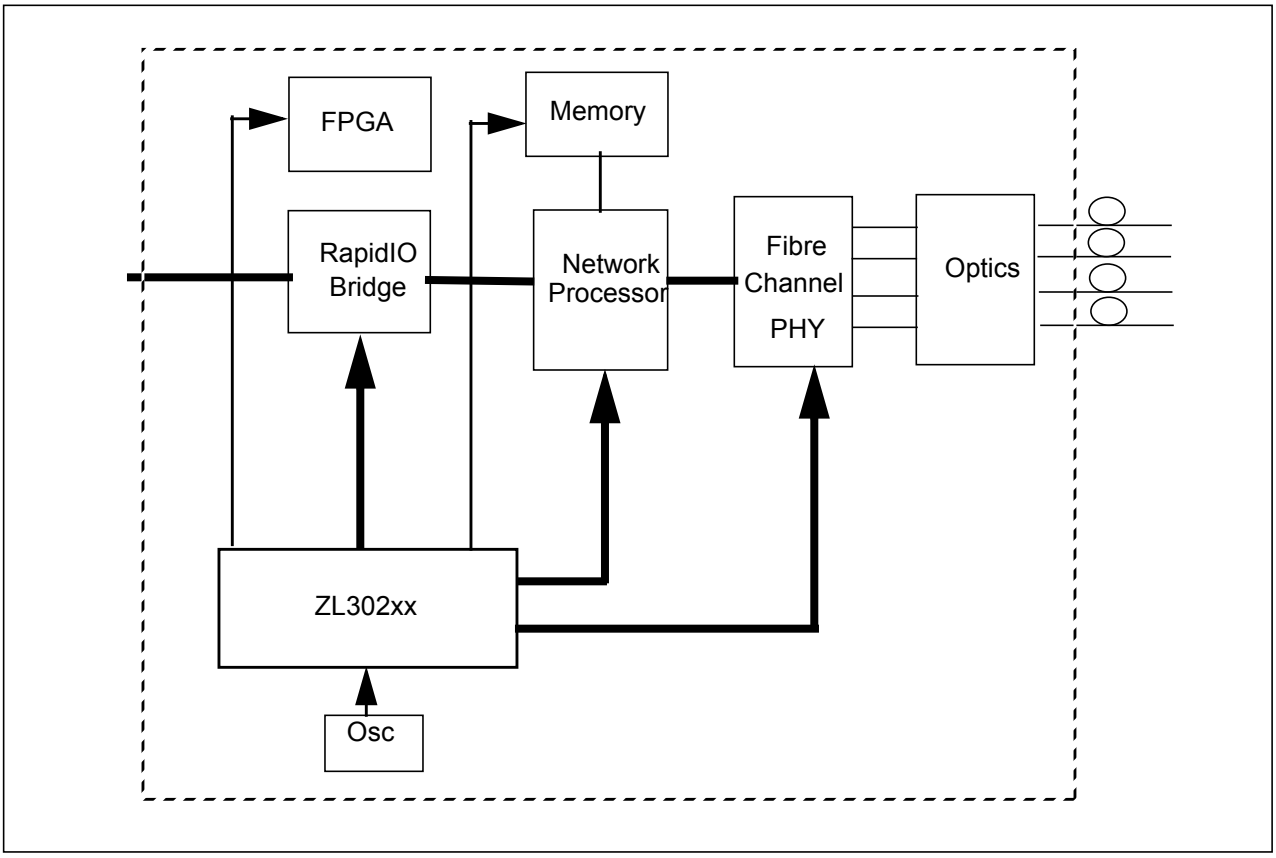

Figure 3 - Application Diagram

4.0 Functional Description

The functional block diagram of the ZL30230 is shown in Figure 1.

The ZL30230 is a programmable clock generator that can be configured by any of the following methods: power-up with its default configuration; power-up with a custom OTP (One Time Programmable) configuration; after power-up it can be dynamically configured via the SPI/I2C port. Configurations set via the SPI/I2C port are volatile and will need to rewritten if the device is reset or powered-down. The SPI/I2C port is also used to access the status registers.

The ZL30230 has four independently programmable clock generators. Two of the clock generators output precision clocks of up to 750MHz with jitter below 0.7ps RMS; and two of the clock generators output general purpose clocks of up to 350MHz with jitter below 20ps RMS. The ZL30230 uses a single master clock based on a crystal resonator, a clock oscillator or a voltage controlled oscillator. All of the clocks output by the ZL30230 will have the same PPM (Parts Per Million) frequency accuracy as the master clock source.

The ZL30230 precision synthesizers can be programmed to generate any frequency between 1,000MHz and 1,500MHz; and the general purpose synthesizers can be programmed to generate any frequency between 500MHz and 750MHz. The frequency resolution of the synthesizers is much less than 1 PPB (Parts Per Billion).

Each synthesizer is followed by four independently programmable 23 bit even/odd post dividers. For skew management purposes, the post dividers feeding the single ended or configurable outputs can impose a phase shift on their output clock signals with resolution equal to a single period of their respective synthesizers' clocks.

All of the ZL30230 clock generators have the same PPM frequency accuracy as the master clock source and therefore the frequency relationships between the clock generators can be programmed exactly. It is possible, for example, to have one generator output 625MHz for 10GBASE-T while another generator outputs 625MHz * 66/64 * 255/237 for 10GBASE-T over OTN (Optical Transport Network). The clock generators will not drift or slip with respect to each other.

Clocks from the two precision clock generators can be output on LVPECL or LVCMOS outputs, and they can be routed to configurable outputs that can be differential (LVPECL, LVDS, or HCSL) or single ended (LVCMOS or LVTTL) with programmable slew rates.

Clocks from the two general purpose clock generators can be output on configurable outputs that can be differential (LVPECL, LVDS, or HCSL) or single ended (LVCMOS or LVTTL); the single ended outputs have programmable slew rates.

The ZL30230 provides ten GPIO pins that can be used as enable pins for the hpout and hpdiff outputs; they can also be used enable or stop the output clocks from the post dividers on a falling or rising edge.

The detailed operation of the ZL30230 is described in the following sections.

4.1 Frequency Synthesis Engine

The device frequency synthesis engine is comprised of a hardware DCO and an analog jitter filtering APLL with built-in digital jitter attenuation scheme. It has two ultra low jitter frequency synthesis engines that can generate output clocks which meet the jitter generation requirements detailed in section 10.0, “Performance Characterization“.

4.2 Dividers and Skew Management

The device has 4 independent dividers associated with each frequency synthesis engine.

The divider engines associated with the high performance differential outputs generate output clocks between 1 kHz and 750 MHz with 50% duty cycle. The other divider engines generate output clocks between 1 kHz and 177.5 MHz for high performance LVCMOS outputs and 160 MHz for single ended configurable outputs with 50% duty cycle. When configurable outputs are in differential mode, the maximum frequency is 350 MHz.

The divider modules generating the single ended output clocks provides the ability to manage the phase skew of the output clock by a coarse step equal to the internal high speed clock period.

The single ended generated output clocks can be stopped either on rising or falling edge (programmed through serial interface or GPIO).The device can be configured to adjust the phase skew of single ended clocks in steps of sub high speed synthesizer clock cycle.

4.3 Output Multiplexer

Figure 4 shows the multiplexing configuration supported.

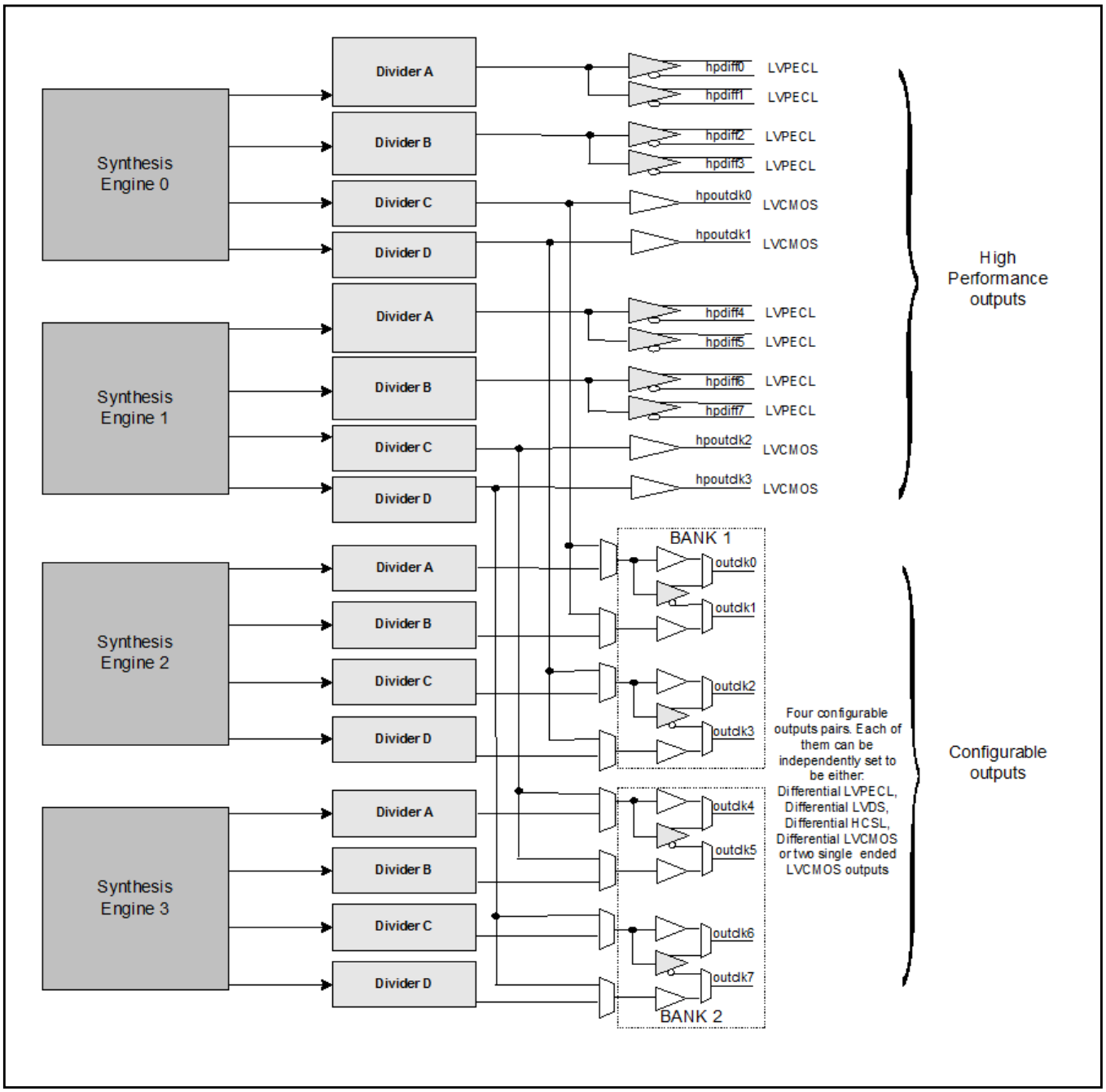

Figure 4 - Output Clock Muxing Configuration

4.4 Output Drivers

The device has 8 high performance (HP) differential (LVPECL) outputs.

The device has 4 high performance (HP) single ended (LVCMOS) outputs.

The device also has 2 banks of configurable output drivers. Each bank can be set as a 4 single ended drivers (LVCMOS or LVTTL) or as a 2 differential output drivers (LVPECL, LVDS, HSTL or HCSL). Each output bank has its own power supply pins, such that each bank of 4 single ended drivers can be set to operate in 3.3 V, 2.5 V, 1.8 V or 1.5 V mode.

High Performance (HP) single ended driver (LVCMOS) supports the jitter specification detailed in section 10.0, “Performance Characterization“ and a maximum speed of 177.5 MHz.

The high performance (HP) differential driver (LVPECL) supports the jitter specification detailed in section 10.0, “Performance Characterization“ and a maximum speed of 750 MHz.

LVPECL outputs should be terminated as shown in Figure 5. Terminating resistors provide 50 Ω equivalent Thevenin termination as well as biasing for the output LVPECL driver. Terminating resistors should be placed as close as possible to input pins of the LVPECL receiver. If the LVPECL receiver has internal biasing then AC coupling capacitors should be added.

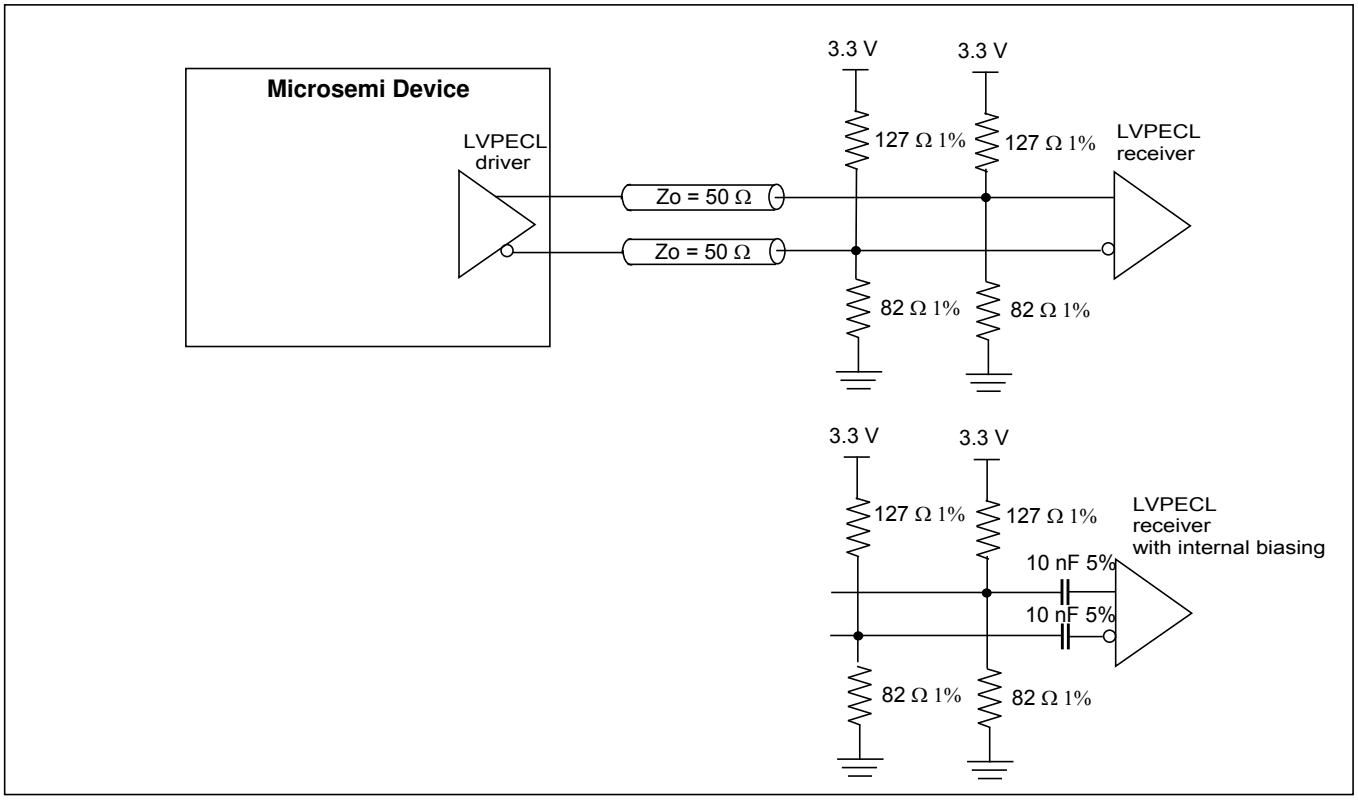

Figure 5 - Terminating LVPECL Outputs

If the transmission line is required to be AC coupled then the termination shown in Figure 6 should be implemented. 200 Ω resistors are used to provide DC biasing for LVPECL driver. Both AC coupling capacitor and biasing resistors should be placed as close as possible to output pins.

Thevenin termination (127 Ω and 82 Ω resistors) provide 50 Ω termination as well as biasing of the input LVPECL receiver. If the LVPECL receiver has internal DC biasing then the line should be terminated with 100 Ω termination resistor between positive and negative input. In both cases termination resistors should be places as close as possible to the LVPECL receiver pins. Some LVPECL receivers have internal biasing and termination. In this case no external termination should be present.

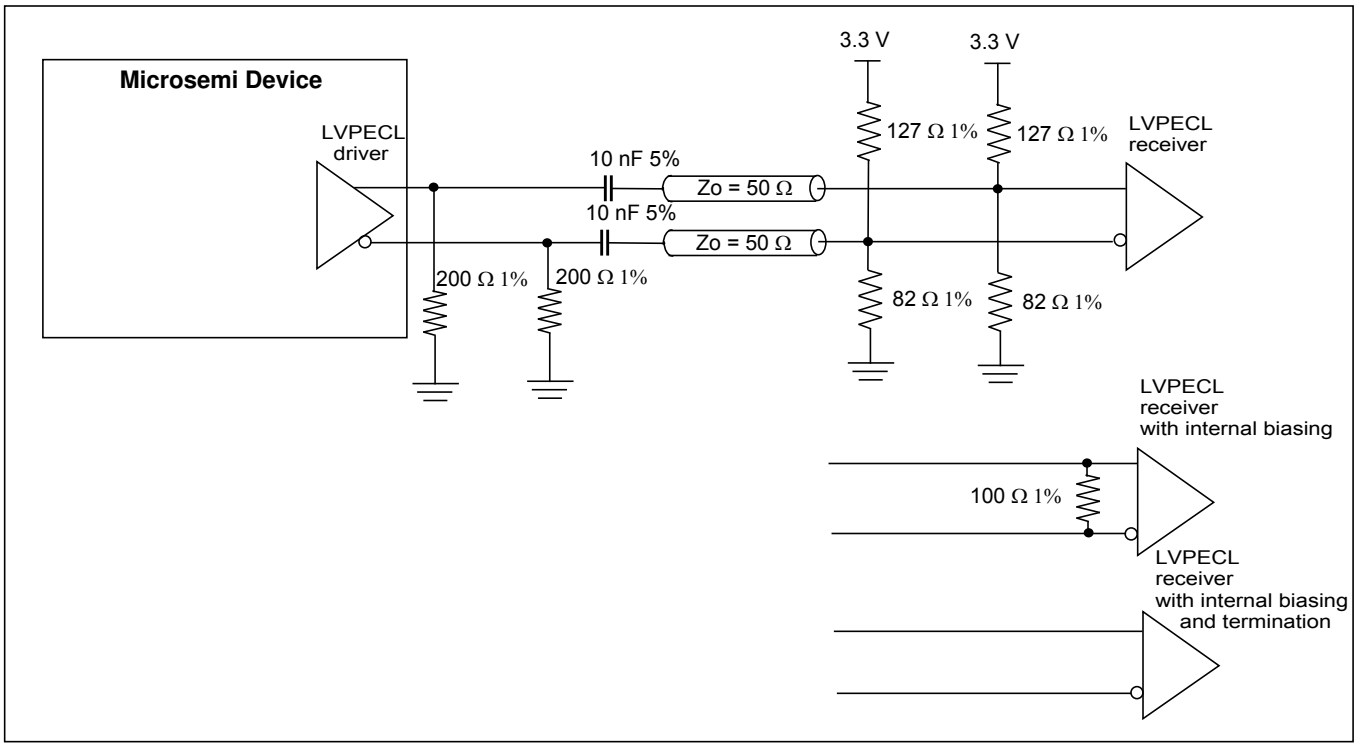

Figure 6 - Terminating AC coupled LVPECL Outputs

High performance LVCMOS outputs (hpoutclkx) should be terminated at the source with 22 Ω resistor as shown in Figure 7. The same type of termination should be used for configurable outputs when they are set to be LVCMOS.

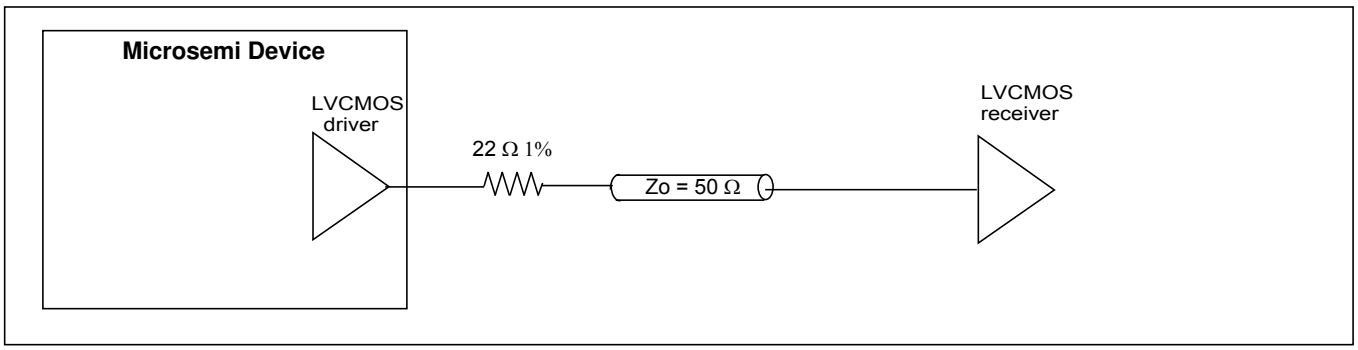

Figure 7 - Terminating LVCMOS Outputs

If the configurable output drivers are programmed to be LVDS, the termination in Figure 8 should be used.

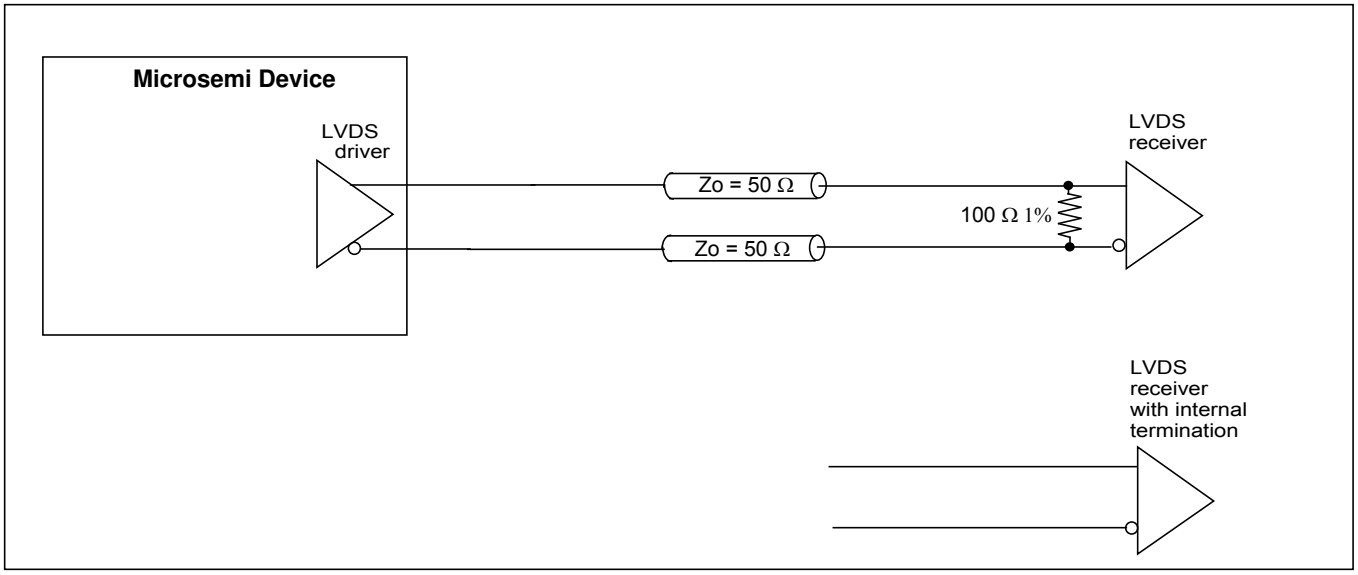

Figure 8 - Terminating LVDS Outputs

When configurable outputs are set to be HCSL, the termination shown in Figure 9 should be used.

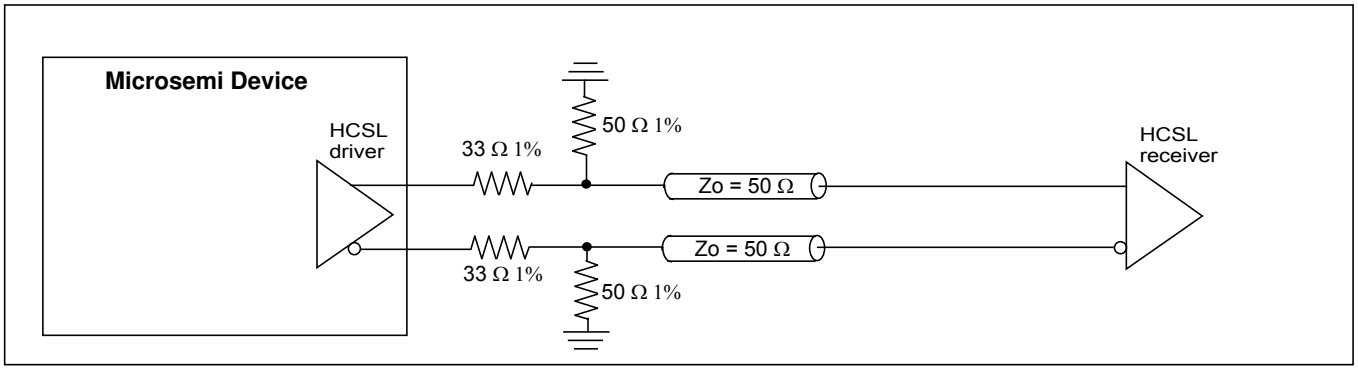

Figure 9 - Terminating HCSL Outputs

4.4.1 Programmable Single Ended Driver - Slew Rate Control

The following are the motivation for fast slew rate:

- Buffer high speed single ended (CMOS) output clock (up to 160 MHz) and/or
- Buffer single ended (CMOS) output clock on a large output load (up to 30 pf)
- Provide rail to rail single ended output clock for any selection of output drive supply voltage (1.5, 1.8, 2.5, 3.3 Volt)

Motivation for medium slew rate:

- Maintain limited output clock ringing and PCB output clocks cross modulation when driving low speed output clock or when small load is present at the output

Each of the available single ended output of the device has 2 available slew rate control limits.These limits are user selectable based on: output clock speed, expected output load or output supply voltage. Table 2 details the limits and the expected output clock slew rates.

	Slew Rate for Fast Slew		**Slew Rate for Medium Slew**	
Expected Load	10 pF	20 pF	10 pF	20 pF
Output Clock 80 MHz or less	1.62 V/ns	1.47 V/ns	0.93 V/ns	0.96 V/ns
Output Clock 160 MHz or less	1.58 V/ns	1.38 V/ns	1.09 V/ns	1.08 V/ns

Table 2 - Slew Rate Control Limits Versus Output Clock Rise/Fall Times

4.5 Master Clock Interface

The master oscillator determines the device free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL). Refer to Application Note ZLAN-68 for a list of recommended clock oscillators and crystals.

4.6 Clock Oscillator and Crystal Circuit

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **osci** pin as shown in Figure 10. The connection to osci should be direct and not AC coupled. The **osco** pin must be left unconnected.

When using crystal resonator as the master timing source, connect crystal between **osci** and **osco** pins as shown in Figure 10. Crystal should have bias resistor of 1MΩ and load capacitances C1 and C2. Value of load capacitances is dependent on crystal and should be as per crystal datasheet. Crystal should be a fundamental mode type -- not an overtone. See ZLAN-68 for crystal recommendation.

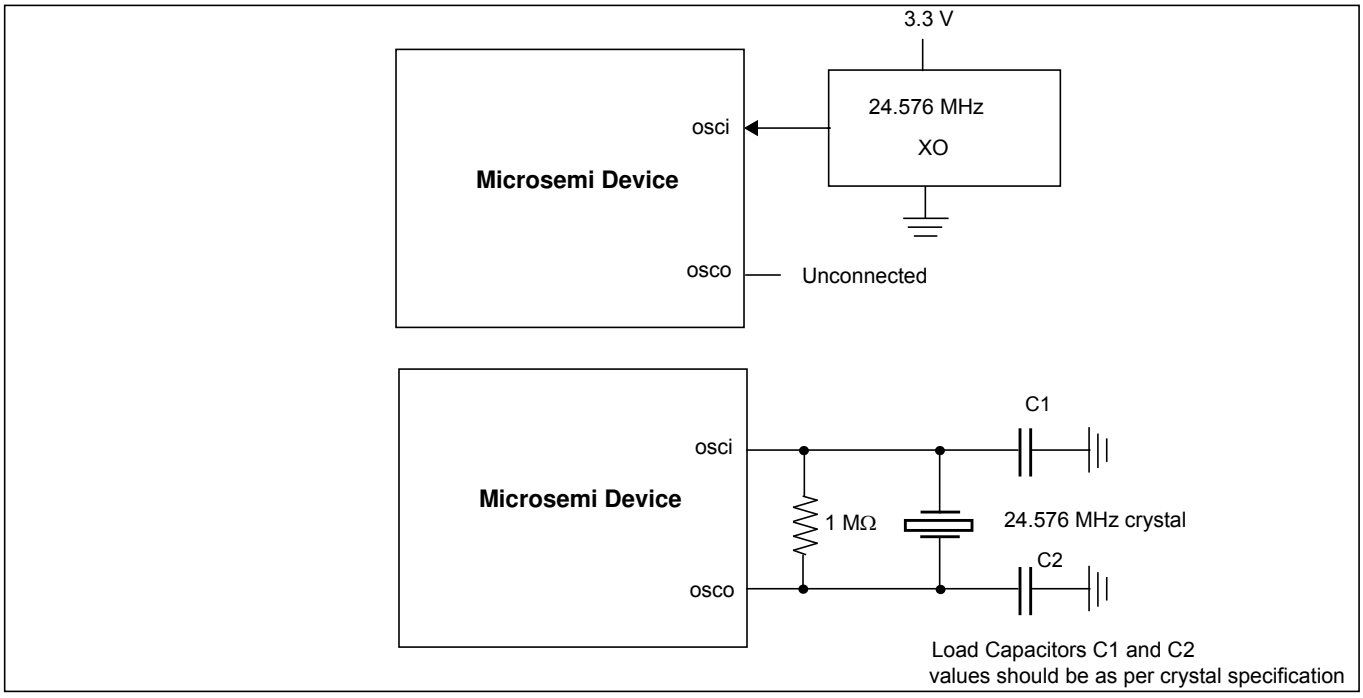

Figure 10 - Clock Oscillator Circuit

The device internal system clocks are generated off the device master clock input (Oscillator or a crystal employing an on-chip buffer/driver). The master clock selection is done at start-up using the available GPIO pins, right after pwr_b get de-asserted. To select 24.576 MHz oscillator, GPIO[1:0] pins need to be held high for 50 ms after the de-assertion of pwr_b, after which time they can be released and used as any other GPIO. Alternatively, these pins can be pulled high with 1 KΩ resistors.

GPIO [1:0]	Master Clock Frequency
0	reserved
1	reserved
2	reserved
3	24.576 MHz

Table 3 - Master Clock Frequency Selection

4.7 Power Up/Down Sequence

The 3.3 V supply should be powered before or simultaneously with the 1.8 V supply. The 1.8 V supply must never be greater than the 3.3 V supply by more than 0.3V. The 1.5V/1.8V/2.5V/3.3V configurable output supply must never be greater than the 3.3 V supply by more than 0.3 V.

The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

4.8 Power Supply Filtering

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Application Note ZLAN-269.

4.9 Power on Reset and Initialization Circuit

To ensure proper operation, the device must be reset by holding the pwr_b pin low for at least 2 ms after power-up when 3.3 V and 1.8 V supplies are stable. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 11. This circuit provides approximately 2 ms of reset low time. The pwr_b input has Schmidt trigger properties to prevent level bouncing.

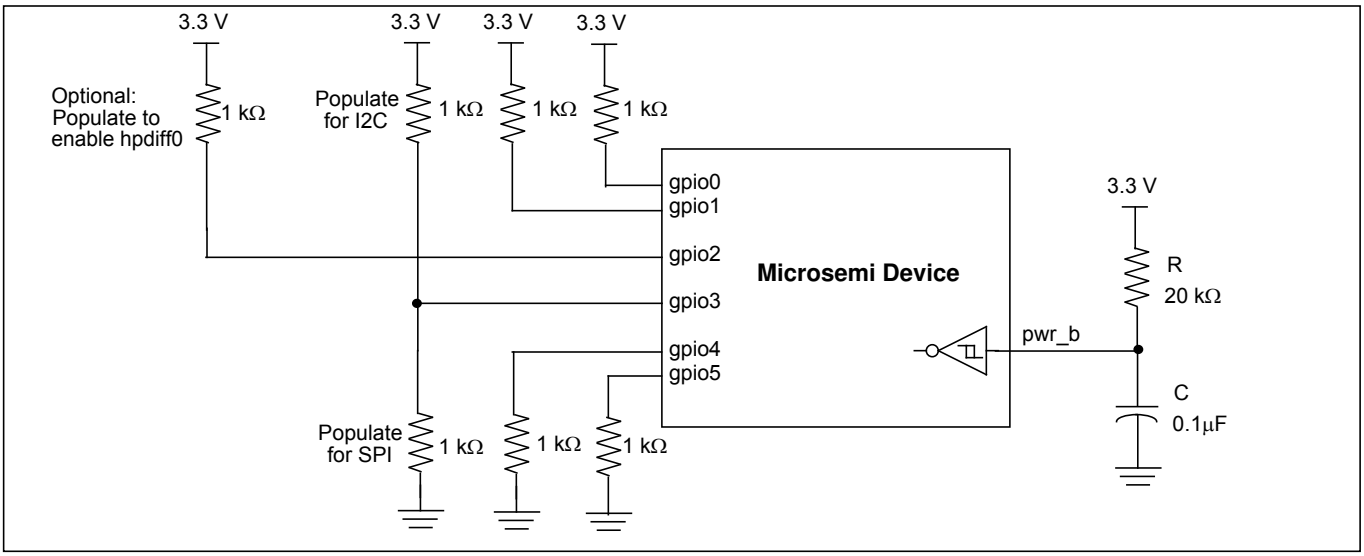

Figure 11 - Typical Power-Up Reset and Configuration Circuit

General purpose pins gpio[0,1,3,4,5] are used to configure device on the power up. They have to be pulled up/down with 1 KΩ resistors as shown in Figure 11 or they can be pulsed low/high during the pwr_b low pulse and kept at the same level for at least 50 ms after pwr_b goes high. After 50 ms they can be released and used as general purpose I/O as described in Section 5.0.

By default all outputs are disabled to allow user first to program required frequencies for different outputs and then to enable corresponding outputs. During the prototype phase, hardware designer can verity if the device is working properly even before software driver is implemented just by pulling up gpio2 pin which enables hpdiff0 output (generates 622.08 MHz by default).

4.10 Ultra Low Jitter Synthesizer Filter Components and Recommended Layout

The low jitter APLL has an on-chip loop filter, but for optimal APLL jitter performance external loop filter is recommended, the following component values are recommended:

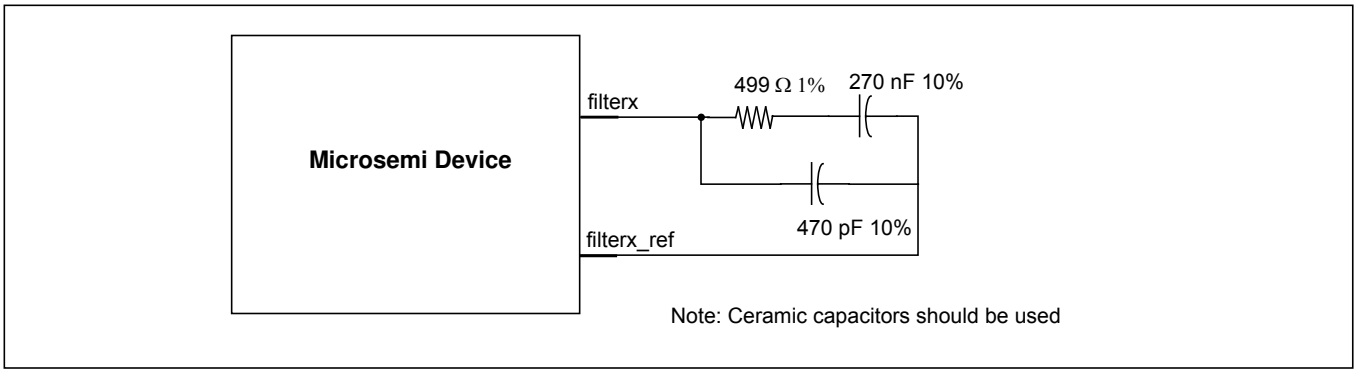

Figure 12 - APLL Filter Component Values

Recommended layout for loop filters is shown in Figure 13:

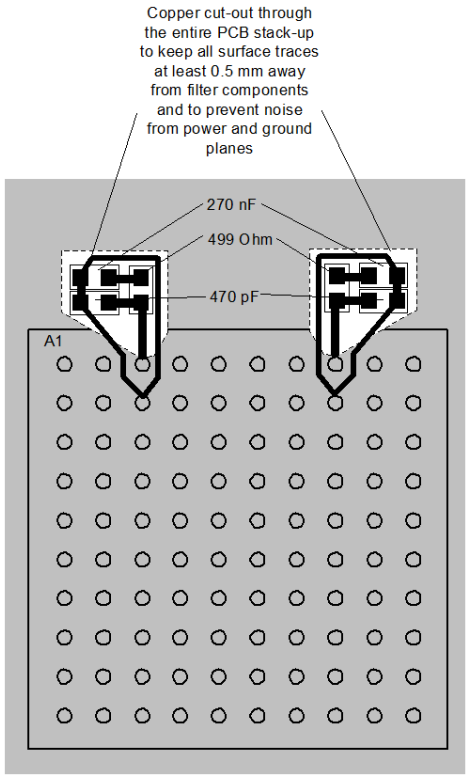

Figure 13 - Recommended Layout for Loop Filters

5.0 Configuration and Control

5.1 Configuration Registers

The ZL30230 configuration is composed of 253 x 8 bits. The configuration registers are assigned their values by any of the following three methods:

1) Default configuration
2) Custom OTP (One Time Programmable) configuration
3) SPI/I2C configuration

5.1.1 Default Configuration

At power-up the device sets its configuration registers to the default reset values.

5.1.2 Custom OTP Configuration

At power-up the device sets it configuration registers to the user defined custom configuration values stored in its one time programmable memory. Custom configurations can be generated using Microsemiès Clockcenter GUI (ZLS30CLKCTR). For custom configured devices contact your local Microsemi Field Applications Engineer or Sales Manager.

5.1.3 SPI/I2C Configuration

After power-up the values of R/W type configuration registers can be dynamically written via the SPI/I2C port. Configurations set via the SPI/I2C port are volatile and will need to rewritten if the device is reset or powered-down.

5.2 Output Multiplexer Configuration and Programmability

The following is the set of parameters that are configurable:

- Output multiplexer configuration
- Start or Stop clock.

5.3 Synthesizers Configuration and Programmability

The following is the set of parameters that are configurable:

- Synthesizer 0 and 1 output frequency between 1.0 GHz and 1.5 GHz
- Synthesizer 2 and 3 output frequency between 500 MHz and 750 MHz.
- Synthesizers 0, 1, 2, 3 high speed output clock, defined as a 1 kHz multiple and 1 kHz multiple with M/N ratio

5.4 Output Dividers and Skew Management Configuration and Programmability

The following is the set of parameters that are configurable:

- Post divider enable/disable
- Divider ratio (2 different setting, independent for each one of the divider outputs)
- Output phase shift value (skew)

5.5 Output Drivers configuration and Programmability

The following is the set of parameters that are configurable:

- Output driver Enable/Disable
- Output driver mode (single ended or differential)

- Single ended driver slew rate control (medium and fast)
- Differential driver mode (LVPECL)

5.6 GPIO Configuration and Programmability

The device GPIO is mapped by the SPI/I2C programmability. The following is an example of control signals that can be supported:

- Differential output clock enable (per output or as a bank of 2 or 4 outputs)
- Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR).
- Output clock stop/start
- Microport Interface Protocol I2C or SPI

The following table defines the function of the GPIO pin when configured as a control pin. Configuring the value in bit 6:0 in GPIO configuration registers enables the stated function.

Value	Name	Description
Default		
0x00	default	GPIO pin defined as an input and no function assigned to it.
Synthesizer Post Divider		
0x44	Stop output clock from Synthesizer0 Post Divider C bit1	This signal is OR-ed with the 'Syntheizer0 Post Divider C stop clock' bit1 in the 'Synthesizer0 and Synthesizer1 Post Dividers stop clock' register.
0x45	Stop output clock from Synthesizer0 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x46	Stop output clock from Synthesizer0 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x47	Stop output clock from Synthesizer0 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4C	Stop output clock from Synthesizer1 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4D	Stop output clock from Synthesizer1 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4E	Stop output clock from Synthesizer1 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4F	Stop output clock from Synthesizer1 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1

Value	Name	Description
0x50	Stop output clock from Synthesizer2 Post Divider A bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x51	Stop output clock from Synthesizer2 Post Divider A bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x52	Stop output clock from Synthesizer2 Post Divider B bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x53	Stop output clock from Synthesizer2 Post Divider B bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x54	Stop output clock from Synthesizer2 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x55	Stop output clock from Synthesizer2 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x56	Stop output clock from Synthesizer2 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x57	Stop output clock from Synthesizer2 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x58	Stop output clock from Synthesizer3 Post Divider A bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x59	Stop output clock from Synthesizer3 Post Divider A bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5A	Stop output clock from Synthesizer3 Post Divider B bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5B	Stop output clock from Synthesizer3 Post Divider B bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5C	Stop output clock from Synthesizer3 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5D	Stop output clock from Synthesizer3 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1