



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



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## Features

- Generates clock signals at power-up per user defined custom OTP (One Time Programmable) configuration
- Dynamically configurable via SPI/I2C interface and volatile configuration registers
- Two independently programmable clock generators output any clock rate from 1 kHz to 750 MHz
- Precision clock generators output clocks with jitter below 0.7 ps RMS for 10 G PHYs
- Operates from a single crystal resonator, clock oscillator or voltage controlled oscillator
- Supports programmable frequency offsets for clock margining; or for use as a digitally controlled oscillator
- Eight LVPECL outputs; max rate 750 MHz
- Four LVCMOS outputs; max rate 177.5 MHz

## Ordering Information

ZL30236GGG	100 Pin LPGA	11mmx11mm	Trays
ZL30236GGG2	100 Pin LPGA*	11mmx11mm	Trays

\*Pb Free Tin/Silver/Copper  
-40°C to +85°C

## Applications

- Timing for NPUs, FPGAs, Ethernet switches and PCIe switches
- Timing for 10 Gigabit CDRs, Rapid-IO, PCIe, Serial MII, Star Fabric, Fibre Channel, XAUI
- Processor clock, Processor bus clock, SDRAM clock, DDR clock

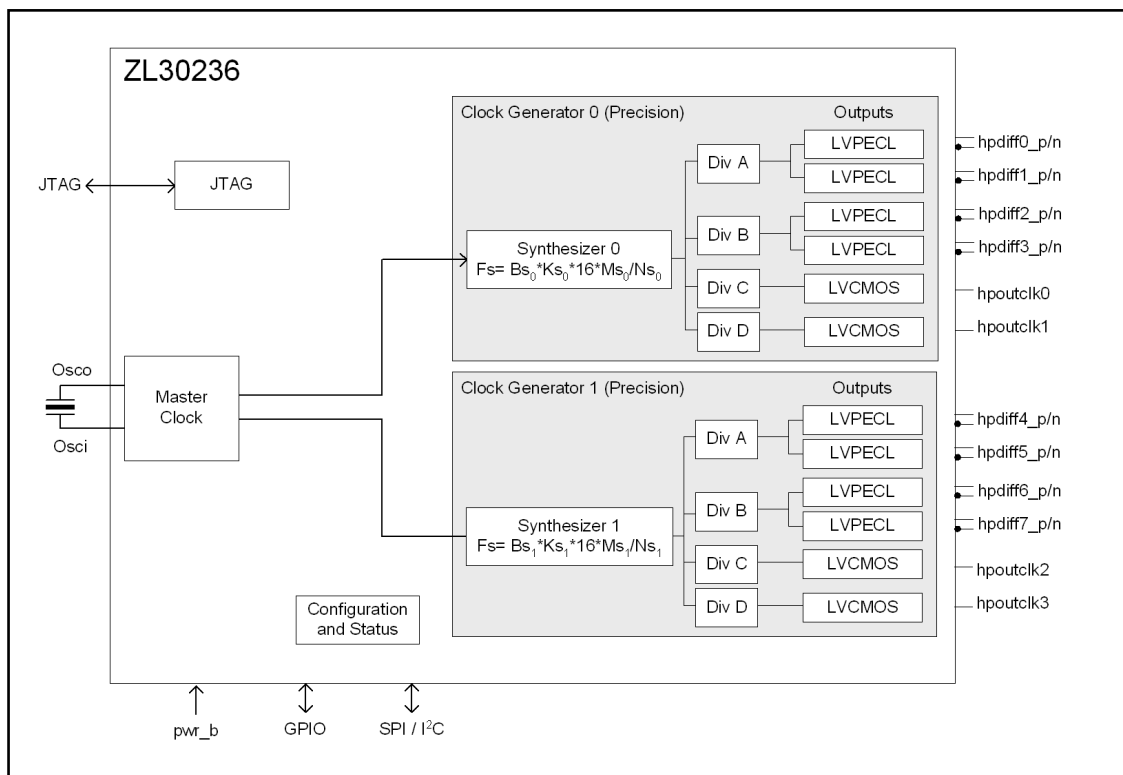
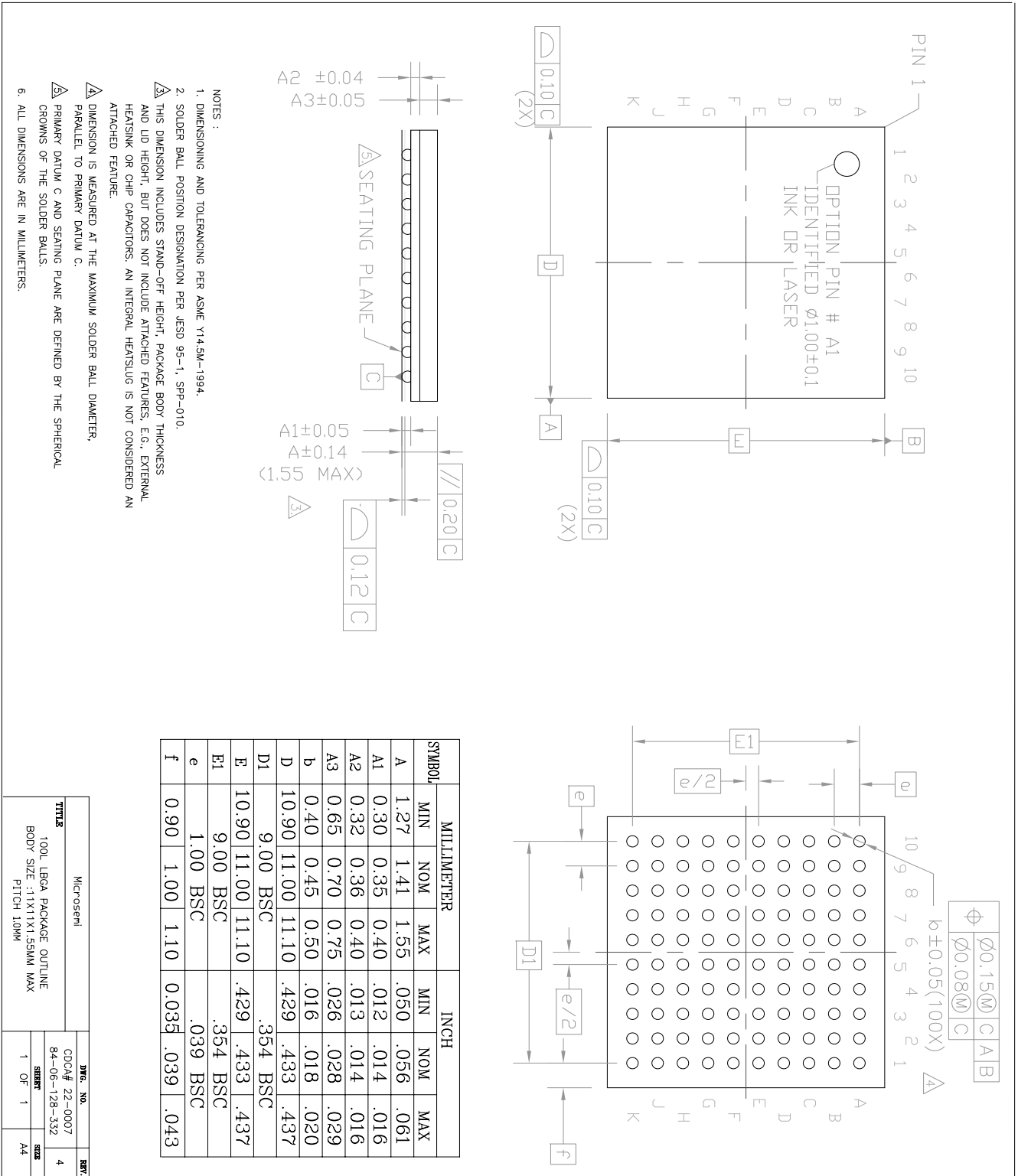


Figure 1 - Functional Block Diagram

# Mechanical Drawing





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