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## Features

- Four independent clock channels
- Frequency and Phase Sync over Packet Networks
  - Frequency accuracy performance for WCDMA-FDD, GSM, LTE-FDD and femtocell applications
  - Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT PEC and CES interfaces
  - Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA and CDMA2000 applications
- Client holdover and reference switching between multiple Servers
- Any input clock rate from 1 kHz to 750 MHz
- Automatic hitless reference switching and digital holdover on reference fail
- Digital PLLs filter jitter at 5.2 Hz, 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Operates from a single crystal resonator or clock oscillator

## Ordering Information:

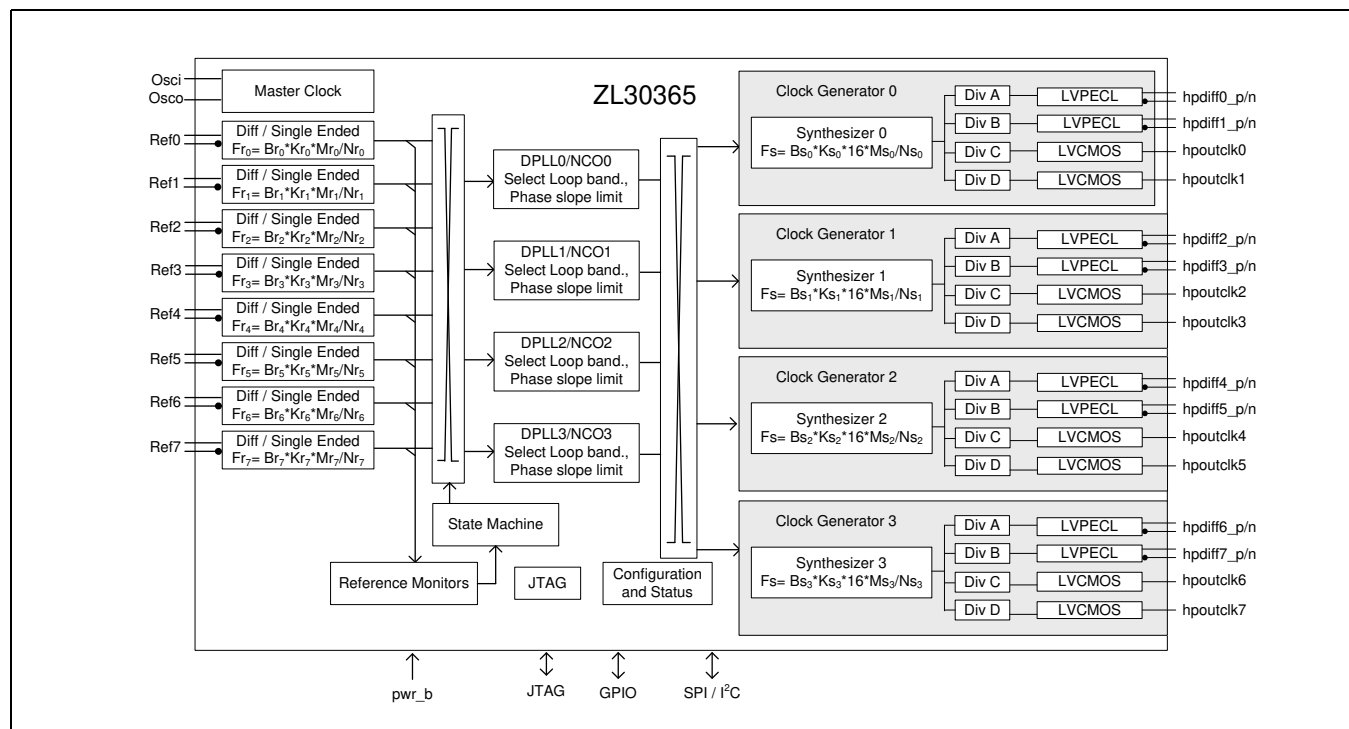
ZL30365GDG2    144 Pin LPGA    Trays

Pb Free Tin/Silver/Copper  
**-40°C to +85°C**  
Package size: 13 x 13 mm

- Electrical phase alignment to input 1 Hz frame pulse with associated reference clock (ref/sync pairing)
- Programmable synthesizers
  - Any output clock rate from 1 Hz to 750 MHz
  - Output jitter of 0.62 ps RMS
  - Eight LVPECL outputs and eight LVCMOS outputs
- Field configurable via SPI/I<sup>2</sup>C interface

## Applications

- OTN muxponders and transponders
- 10 Gigabit line cards
- Synchronous Ethernet, SONET/SDH, Fibre Channel, XAUI



**Figure 1 - Functional Block Diagram**

## Detailed Features

### General

- Four independent clock channels
- Operates from a single crystal resonator or clock oscillator
- Configurable via its SPI/I<sup>2</sup>C interface

### Time Synchronization Algorithm

- External algorithm controls software digital PLL to adjust frequency and phase alignment
- Frequency, Phase and Time Synchronization over IP, MPLS and Ethernet Packet Networks
- Frequency accuracy performance for WCDMA-FDD, GSM, LTE-FDD and femtocell applications, with target performance less than  $\pm 15$  ppb.
- Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications.
- Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA and CDMA2000 applications with target performance less than  $\pm 1$   $\mu$ s phase alignment.
- Time Synchronization for UTC-traceability and GPS replacement.
- Client reference switching between multiple Servers
- Client holdover when Server packet connectivity is lost

### Electrical Clock Inputs

- Eight input references configurable as single ended or differential
- Synchronize to any clock rate from 1 kHz to 750 MHz on differential inputs
- Synchronize to any clock rate from 1 kHz to 177.75 MHz on singled-ended inputs
- Synchronize to clock or sync pulse and clock pair
- Any input reference can be fed with sync (frame pulse) or clock.
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities
  - LOS
  - Single cycle monitor
  - Precise frequency monitor
  - Coarse frequency monitor
  - Guard soak timer
- Per input clock delay compensation

### Electrical Clock Engine

- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Internal state machine automatically controls mode of operation (free-run, locked, holdover)
- Automatic hitless reference switching and digital holdover on reference fail
  - Physical-to-physical reference switching
  - Physical-to-packet reference switching

- Packet-to-physical reference switching
- Packet-to-packet reference switching
- Selectable phase slope limiting
- Supports ITU-T G.823, G.824 and G.8261 for 2048 kbit/s and 1544 kbit/s interfaces

**Electrical Clock Generation**

- Four programmable synthesizers
- Eight LVPECL outputs
  - Two LVPECL outputs per synthesizer
  - Generate any clock rate from 1 Hz to 750 MHz
  - Low jitter of 0.62 ps RMS
  - Meets OC-192, STM-64, 1 GbE and 10 GbE interface jitter requirements
- Eight LVCMOS outputs
  - Two LVCMOS outputs per synthesizer
  - Generate any clock rate from 1 Hz to 177.75 MHz
  - Maximum jitter below 1 ps rms
- Programmable output advancement/delay to accommodate trace delays or compensate for system routing paths
- Outputs may be disabled to save power

**API Software**

- Interfaces to 1588-capable PHY and switches with integrated timestamping
- Abstraction layer for independence from OS and CPU, from embedded SoC to home-grown
- Fits into centralized, highly integrated pizza box architectures as well as distributed architectures with multiple line cards and timing cards

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