Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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One, Two and Four Channel Clock Transaltor

Features

- Up to four independent clock channels
- Excellent jitter performance of 180 fs rms in 12 kHz to 20 MHz band meets jitter requirements of 10G/40G and 100G PHYs
- Three programmable ultra-low jitter synthesizers generate any frequency from 0.5 Hz to 900 MHz.
- One programmable general purpose synthesizer generates any clock from 0.5 Hz to 180 MHz
- 6 differential (CML) or 12 single ended (CMOS) ultra-low jitter outputs plus two general purpose CMOS outputs
- Accepts up to 10 LVPECL/LVDS/HCSL/LVCMOS inputs
- Any input reference can be fed with clock, sync (frame pulse), clock /sync pair or clock modulated with sync pulse (embedded PPS ePPS and embedded PP2S ePP2S)

Ordering Information

ZL30611LDG6*	100 Pin aQFN	Trays
ZL30612LDG6*	100 Pin aQFN	Trays
ZL30614LDG6*	100 Pin aQFN	Trays

*Pb Free Tin/Silver/Copper

Package size: 10 x 10 mm

-40°C to +85°C

- Up to four programmable digital PLLs/NCOs with loop bandwidth from 14 Hz to 470 Hz synchronize to any clock rate from 1 kHz to 900 MHz and to clock plus sync pulse.
- Automatic hitless reference switching and digital holdover on reference fail with initial holdover accuracy better than 1 ppb with post holdover filter.

Applications

- Synchronous Ethernet/Sonet/SDH timing and line cards
- Wireless Backhaul
- Wireless Base stations
- Test Equipment

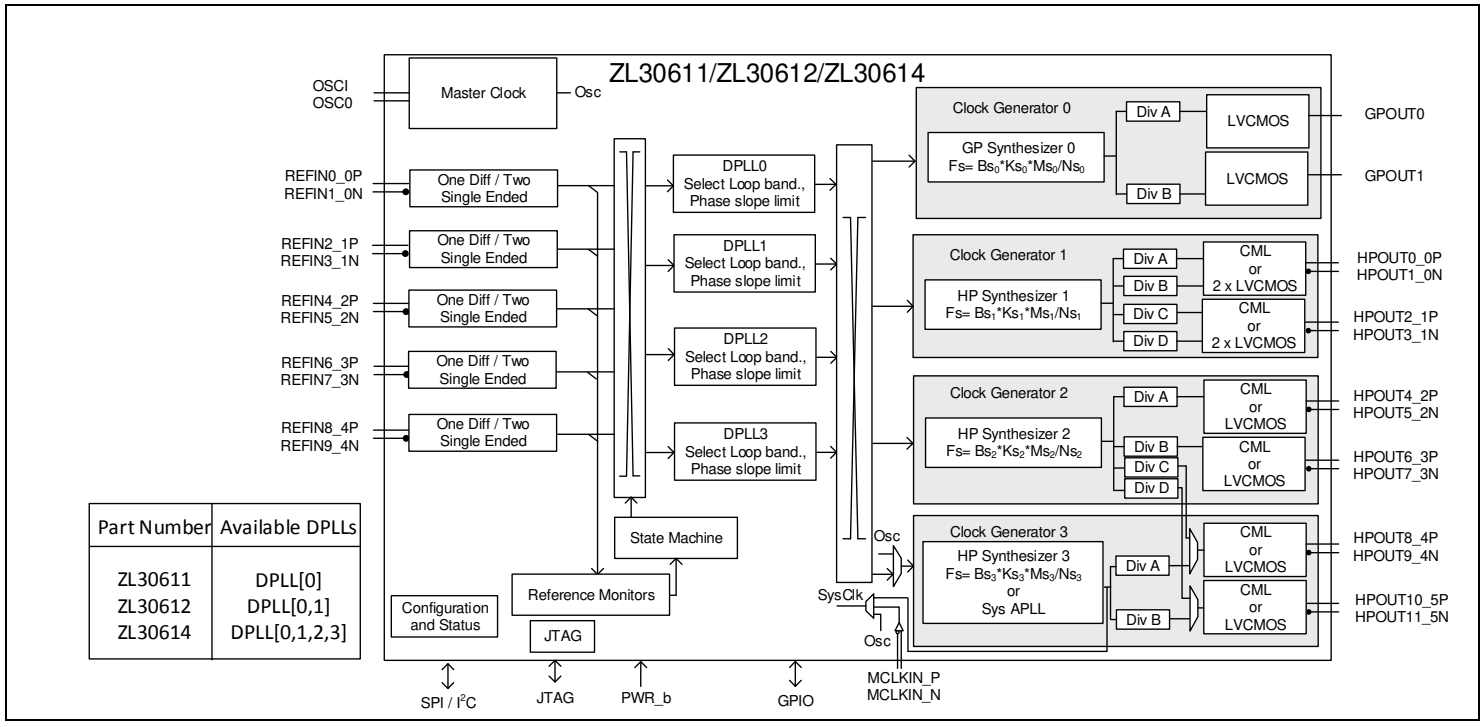

Figure 1. Functional Block Diagram

3 Feature List

3.1 General features

- Up to four independent clock channels
- Operates from a single crystal resonator or clock oscillator
- Configurable from SPI/I2C bus or from pre-configured flash memory

3.2 Electrical Clock Inputs

- Accepts up to 10 LVCMOS or 5 LVDS/HCSL/LVPECL/CML inputs
- Frequencies from 0.5 Hz to 180 MHz for LVCMOS
- Frequencies from 0.5 Hz to 900 MHz for LVDS/HCSL/LVPECL/CML
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities.
    - Each input reference has its own set of monitors which can be independently programmed.
    - Loss of signal (LOS)
    - Single Cycle Monitor (Triggers on glitches or variation in duty-cycle)
    - Coarse Frequency Monitor
    - Precise Frequency Monitor
- Locks to gapped clocks

3.3 Electrical Clock Input-Output Special Formats

- Supports 64 kHz composite clocks with external glue logic
- Supports embedded pulse per second (ePPS) single wire for carrying high-speed clock & 1PPS
- Supports REF-SYNC pair, a combination of a high speed clock reference and a frame pulse sync pair
- Each output can generate clock, sync pulse, embedded pulse per second (ePPS) or embedded pulse per 2 seconds (ePP2S)
    - Clock modulated sync feature helps in reducing number of clock lines on backplane and in addition provides equal delay for both clock and sync signals.

3.4 Electrical Clock Engine

- Digital PLLs filter jitter from 14 Hz up to 470 Hz
- Multiple modes of operation
    - Freerun
    - Forced holdover
    - Forced reference
    - Automatic
    - NCO
- Internal state machine automatically controls state
    - Locked
    - Acquiring
    - Holdover
- Support for fast lock with lock times in seconds
- Support for hitless reference switching
- Internal, per DPLL, time of day counters maintaining full 48-bit seconds and 32-bit nanoseconds aligned to 1PPS rollover
- Holdover better than 0.01 ppb
- Full rate conversion between input and output clock frequencies
- Supports ITU-T G.823, G.824 and G.8261 for 2048 Kbit/s and 1544 Kbit/s interfaces
- Supports G.781 SETS

3.5 Electrical Clock Generation

- Four programmable synthesizers
- Precision Synthesizers
  - Each ultra-low jitter output can be independently set to be differential (CML) or two CMOS
  - Six CML outputs
    - Generate clock rates from 0.5 Hz to 900 MHz
    - Jitter performance of 180 fs rms (12 KHz – 20 MHz)
    - Meets OC-192, STM-64, 1 GbE & 10 GbE interface jitter requirements
  - Twelve LVCMOS outputs
    - Generate clock rates from 0.5 Hz to 180 MHz
    - Jitter performance of 290 fs rms (12 kHz – 20 MHz)
- General Synthesizer
  - Two LVCMOS outputs
  - Generate clock rates from 1 Hz to 180 MHz
  - Jitter performance of 17 ps rms (12 kHz – 20 MHz)
- Programmable output advancement/delay to accommodate trace delays or compensate for system routing paths
- Each output has its own power supply pin which can be hooked to 3.3V, 2.5V or 1.8V supplies. Outputs may be disabled to save power

4 Application

The only difference between ZL30611/ZL30612/ZL30614 is the number of DPLLs. The least significant digit in the part number assigns the number of available DPLLs.

4.1 Applications Examples

- Integrated basestation reference synchronization for air interfaces for
- GSM, WCDMA, TD-SCDMA, LTE and LTE-A
- FDD or TDD mobile technology
- femtocells, small cells (residential, urban, rural, enterprise), picocells and macrocells
- Mobile Backhaul NID, cell-site router, edge switch/router, microwave or access aggregation node
- EPON/GPON OLT and ONU/OLT
- DSLAM and RT-DSLAM
- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fiber Channel, XAUI

4.2 Physical Layer – Chassis Architecture

ZL30611/ZL30612/ZL30614 provides up to four independent PLL channels which can synchronize to any input frequency from 0.5Hz up to 900MHz for clock/sync pair inputs and from 1 kHz to 900 MHz for clock only inputs. ZL30611/ZL30612/ZL30614 can generate any output frequency from 0.5Hz up to 180MHz for LVCMOS and up to 900MHz for CML outputs. Each channel is comprised of a DPLL and a Synthesizer.

Typical application of ZL30611/ZL30612/ZL30614 is Synchronous Ethernet/Sonet/SDH line card synchronizer device as shown in **Error! Reference source not found.**. Line card synchronizer is responsible for:

- Provide hitless reference switching between active and redundant timing cards.
- Translate frequency from backplane clock to frequencies required by PHY devices.
- Filter jitter down to levels required by PHY devices.
- Provide holdover in case both active and redundant timing card fail.

For 1588 applications synchronize to sync plus clock (typically 1pps plus 10MHz) and generate 1pps signal. If the XO frequency is higher than100MHz - 5%, Synthesizer 3 can be locked to any DPLL and used to generate any frequency. For fundamental mode oscillators (up to 50MHz) Synthesizer 3 needs to be used as an internal system clock generator.

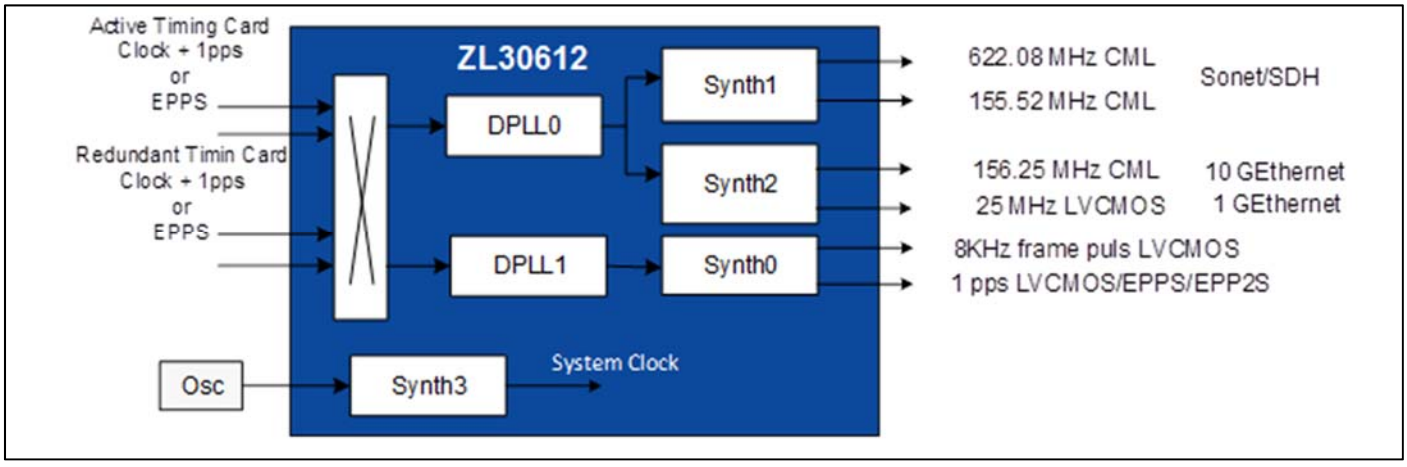

Figure 2. System with timing redundancy

5 Product Family

There are several devices within the ZL30611/612/614 family. They are differentiated by the number of DPLL, as shown in

Table 1 · ZL3061x Product Family

Product Number	Number of DPLL Channels	Number of Synthesizers
ZL30611	1	4
ZL30612	2	4
ZL30614	4	4

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