



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Features

- **Packet Network Frequency and Phase Sync**
 - Frequency accuracy for GSM, WCDMA-FDD, LTE-FDD basestations and small cells
 - Frequency performance for ITU-T G.823 and G.824 synchronization interface, G.8261 PNT PEC and CES interfaces and G.8263 PEC-S-F
 - Phase synchronization performance for WCDMA-TDD, TD-SCDMA, CDMA2000, LTE-TDD and LTE-A applications
 - Client holdover and reference switching between multiple servers
 - Support for new ITU-T packet clock drafts or recs: G.8263 PEC, G.8273.2 T-BC & T-TSC w/o SyncE, and G.8273.4 T-BC-P & T-TSC-P
 - Hybrid mode for mixing SyncE and IEEE1588
- **Physical Layer Clock Synchronization**
 - ITU-T G.8262 SyncE EEC options 1 and 2
- **Low-Bandwidth DPLL Per Channel**
 - Programmable bandwidth, 0.1Hz to 500Hz
 - Hitless reference switching
 - High-resolution holdover averaging
 - Numerically controlled oscillator mode
- **Three Input Clocks Per Channel**
 - Three inputs, two differential/CMOS, one CMOS
 - Any input frequency from 8kHz to 1250MHz (8kHz to 300MHz for CMOS)
- Per-input activity and frequency monitoring

Ordering Information

ZL30723LFG7	64 Pin LGA	Trays
ZL30723LFF7	64 Pin LGA	Tape and Reel
Ni Au		
Package size: 5 x 10 mm		
-40°C to +85°C		

- **Low-Jitter Frac-N APLL, 3 Outputs Per Channel**
 - Any output frequency from <1Hz to 1035MHz
 - High-resolution fractional frequency conversion with 0ppm error
 - Encapsulated design requires no external VCXO or loop filter components
 - Output jitter as low as 0.25ps RMS (12kHz-20MHz integration band)
 - Outputs are CML or 2xCMOS, can interface to LVDS, LVPECL, HSTL, SSTL and HCS
 - Per-output supply pin with CMOS output voltages from 1.5V to 3.3V
 - Precise output alignment circuitry and per-output phase adjustment
 - Per-output enable/disable and glitchless start/stop (stop high or low)
- **General Features**
 - Automatic self-configuration at power-up from internal EEPROM; up to four configurations
 - Input-to-output alignment with external feedback
 - SPI or I²C processor Interface
 - Easy-to-use evaluation software

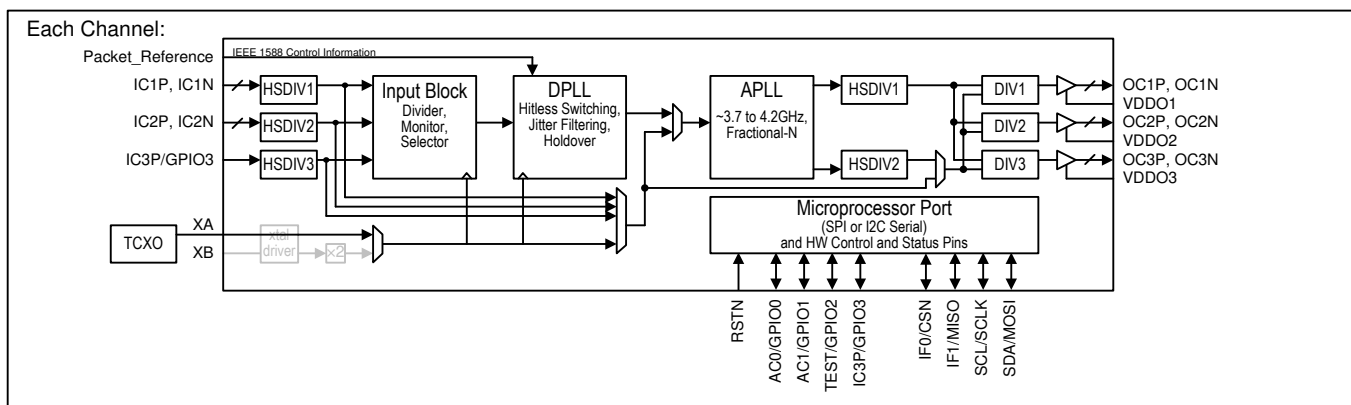


Figure 1 - Functional Block Diagram

1. Application Examples

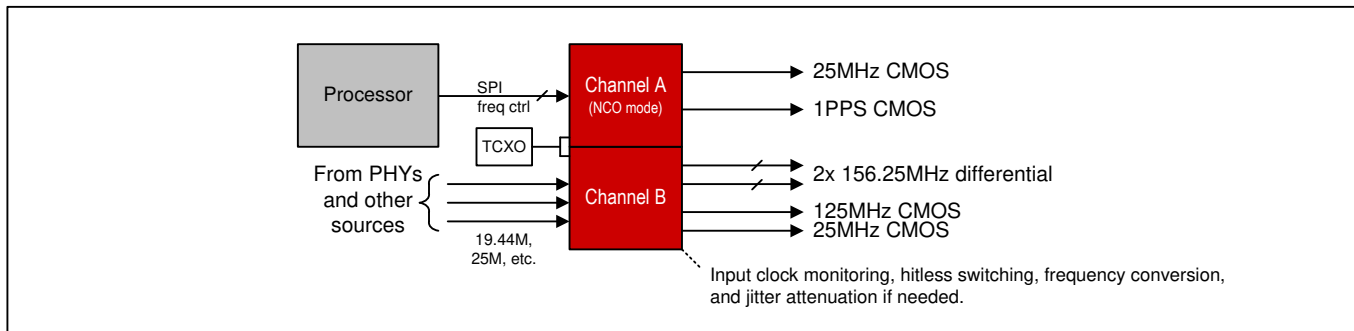


Figure 2 – Telecom Timing Card Application

2. Detailed Features

2.1 Time Synchronization Algorithm

- External algorithm controls software digital PLL to adjust frequency and phase alignment
- Frequency, phase and time synchronization over IP, MPLS and Ethernet packet networks
- Frequency accuracy performance for GSM, WCDMA-FDD, LTE-FDD femtocell, small cell (residential, urban, rural, enterprise), picocell and macrocell applications, with target performance less than ± 15 ppb
- Frequency performance for ITU-T G.8263 for PEC-S-F (Packet Equipment Clock - Slave - Frequency)
- Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications
- Phase synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA, CDMA2000, LTE-TDD and LTE-A femtocell, small cell (residential, urban, rural, enterprise), picocell and macrocell applications with target performance less than $\pm 1\mu\text{s}$ phase alignment.
- Phase performance for ITU-T packet clock drafts or recommendations in development
 - ITU-T G.8273.2 T-BC, T-TSC
 - ITU-T G.8273.4 T-BC-P, T-TSC-P
- Time Synchronization for TAI, UTC-traceability and GNSS/GPS replacement.
- Client reference switching between multiple servers
- Client holdover when server packet connectivity is lost
- Client synchronization to best server with monitoring of secondary server references

2.2 Input Clock Features

- Three input clocks per channel, two differential or single-ended, one single-ended
- Input clocks can be any frequency from 8kHz up to 1250MHz (differential) or 300MHz (single-ended)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the input after a few missing clock cycles
- Frequency measurement and monitoring with 1ppm resolution and accept/reject hysteresis
- Optional input clock invalidation on GPIO assertion to react to LOS signals from PHYs

2.3 Electrical Clock Engine Features

- Two internal DPLLs, one per channel
- Very high-resolution DPLL architecture
- State machine automatically transitions between tracking and freerun/holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.1Hz to 500Hz
- Less than 0.1dB gain peaking
- Programmable phase-slope limiting
- Programmable tracking range (i.e. hold-in range)

- Truly hitless reference switching with <200ps output clock phase transient
 - Physical-clock-to-physical-clock reference switching
 - Physical-clock-to-packet-timing reference switching
 - Packet-timing-to-physical-clock reference switching
 - Packet-timing-to-packet-timing reference switching
- Support for SyncE and SONET/SDH equipment clock specifications
 - ITU-T G.8262 option 1 EEC
 - ITU-T G.8262 option 2 EEC
 - ITU-T G.813 option 1 SEC
 - IUT-T G.813 option 2 SEC
- Output phase adjustment in 10ps steps
- High-resolution frequency and phase measurement
- Fast detection of input clock failure and transition to holdover mode
- Holdover frequency averaging with programmable averaging time and delay time

2.4 APLL Features

- APLL with very high-resolution fractional scaling (i.e. non-integer) per channel
- Any-to-any frequency conversion with 0ppm error
- Two high-speed dividers (integers 4 to 15, half divides 4.5 to 7.5)
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Bypass mode supports system testing

2.5 Output Clock Features

- Three low-jitter output clocks per channel
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1035MHz (250MHz max for CMOS and HSTL outputs)
- Output jitter as low as 0.25ps RMS (12kHz to 20MHz)
- In CMOS mode, an additional divider allows the OCxN pin to be an integer divisor of the OCxP pin (Example 1: OC3P 125MHz, OC3N 25MHz. Example 2: OC2P 25MHz, OC2N 1Hz)
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Sophisticated output-to-output phase alignment
- Per-output phase adjustment with high resolution and unlimited range
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

2.6 General Features

- SPI or I²C serial microprocessor interface per channel
- Automatic self-configuration at power-up from internal EEPROM memory; pin control to specify one of four stored configurations
- Numerically controlled oscillator (NCO) behavior allows system software to steer DPLL frequency with resolution better than 0.01ppb
- Input-to-output alignment with external feedback
- Four general-purpose I/O pins per channel each with many possible status and control options
- Output frame sync signals: 2kHz or 8kHz (SONET/SDH), 1Hz (IEEE 1588) or other frequency
- Internal compensation for local oscillator frequency error

2.7 API Software

- Interfaces to 1588-capable PHYs and switches with integrated timestamping
- Abstraction layer for independence from OS and CPU, from embedded SoC to home-grown
- Fits into centralized, highly integrated “pizza box” architectures as well as distributed architectures with multiple line cards and timing cards

3. Applications

- ITU-T G.8262 system timing cards for Synchronous Ethernet systems
- System timing cards which support ITU-T G.781 SETS (SDH Equipment Timing Source)
- Integrated basestation reference synchronization for air interfaces for
 - GSM, WCDMA, TD-SCDMA, LTE and LTE-A
 - FDD or TDD mobile technology
 - Femtocells, small cells (residential, urban, rural, enterprise), picocells and macrocells
- Mobile Backhaul NID, cell-site router, edge switch/router, microwave or access aggregation node
- EPON/GPON OLT and ONU/ONT
- DSLAM and RT-DSLAM
- 10G, 40G and 100G line cards
- SONET/SDH, Fibre Channel, XAU1

4. Pin Diagram

The device is packaged in a 5x10mm 64-pin LGA.

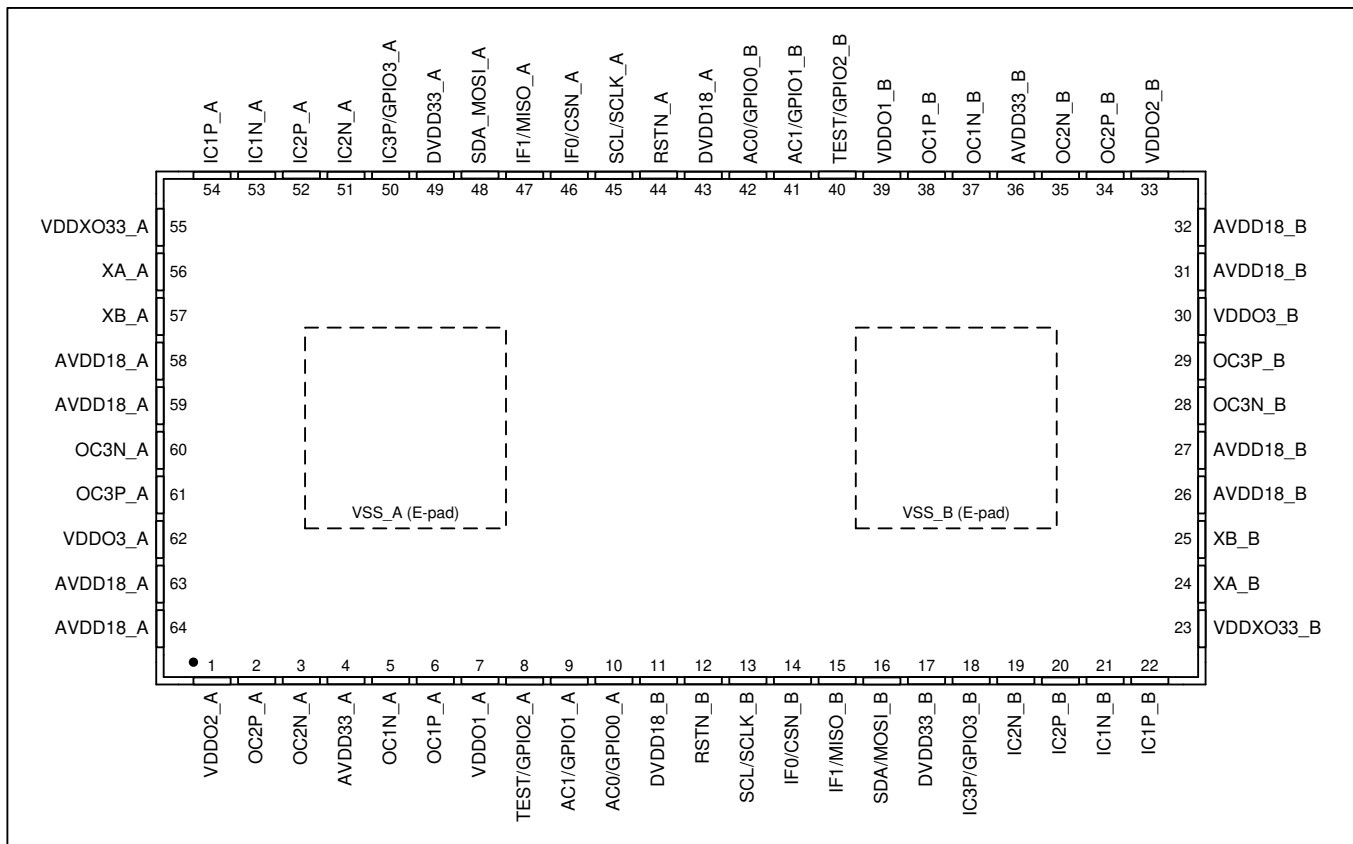
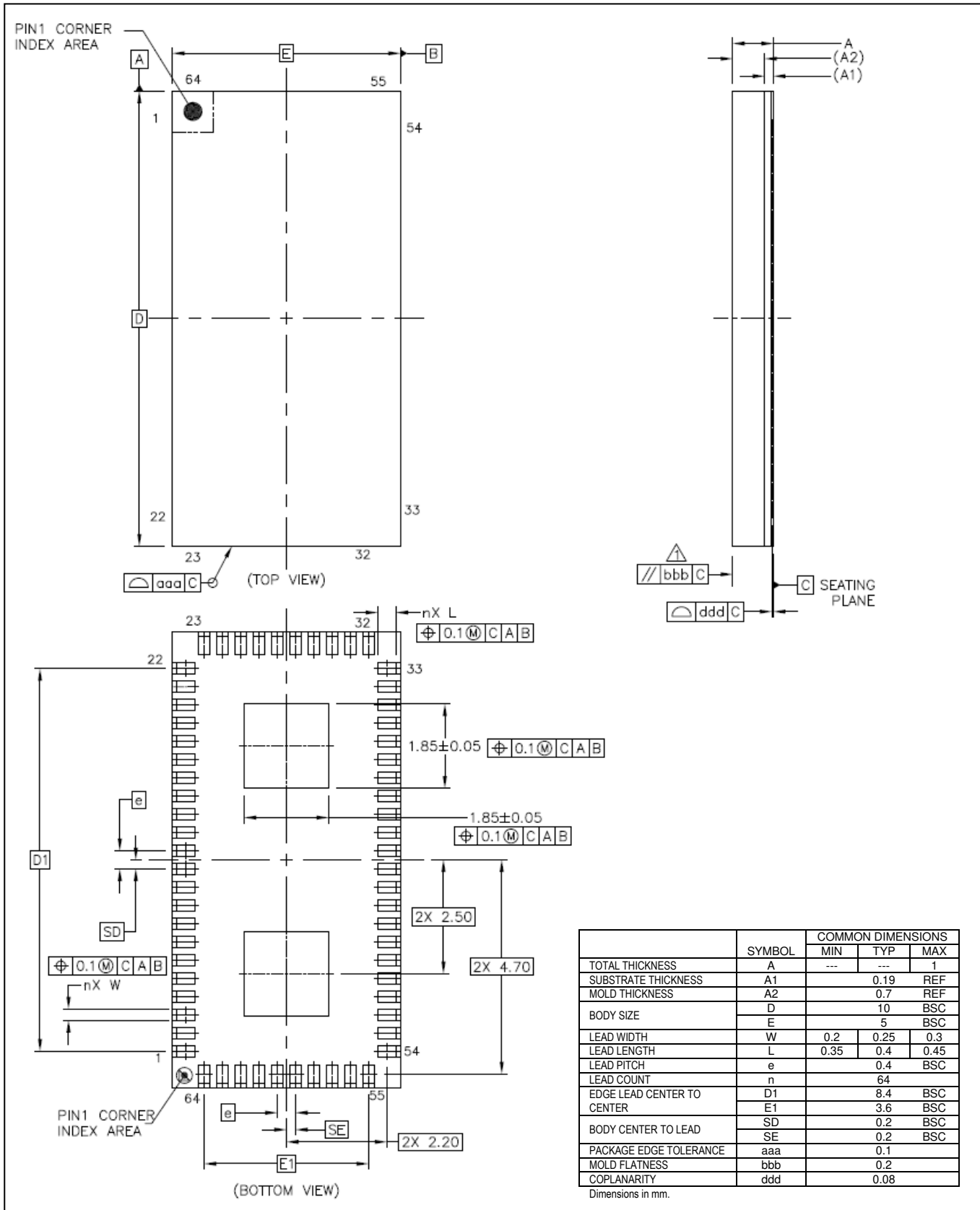


Figure 3 - Pin Diagram

5. Mechanical Drawing





Microsemi Corporate Headquarters
One Enterprise
Aliso Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

©2016 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,400 employees globally. Learn more at www.microsemi.com.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.