



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Zarlink has introduced a new generation family of AEC (ZL38002 and ZL38004). Zarlink recommends these products for new designs.

September 2010

Features

- Contains two echo cancellers: 112 ms acoustic echo canceller + 16 ms line echo canceller
- Works with low cost voice codec. ITU-T G.711 or signed mag μ /A-Law, or linear 2's comp
- Each port may operate in different format
- Advanced NLP design - full duplex speech with no switched loss on audio paths
- Fast re-convergence time: tracks changing echo environment quickly
- Adaptation algorithm converges even during Double-Talk
- Designed for exceptional performance in high background noise environments
- Provides protection against narrow-band signal divergence
- Howling prevention stops uncontrolled oscillation in high loop gain conditions
- Offset nulling of all PCM channels
- Serial micro-controller interface

Ordering Information

ZL38001QDG1	48 Pin TQFP*	Trays, Bake & Drypack
ZL38001DGF1	36 Pin SSOP*	Tape & Reel, Bake & Drypack
ZL38001DGE1	36 Pin SSOP*	Tubes, Bake & Drypack
*Pb Free Matte Tin		
-40°C to +85°C		

- ST-BUS, GCI, or variable-rate SSI PCM interfaces
- User gain control provided for speaker path (-24 dB to +48 dB in 3 dB steps)
- 18 dB gain at Sout to compensate for high ERL environments
- AGC on speaker path
- Handles up to 0 dB acoustic echo return loss
- Transparent data transfer and mute options
- 20 MHz master clock operation
- Low power mode during PCM Bypass
- Bootloadable for future factory software upgrades
- 2.7 V to 3.6 V supply voltage; 5 V tolerant inputs

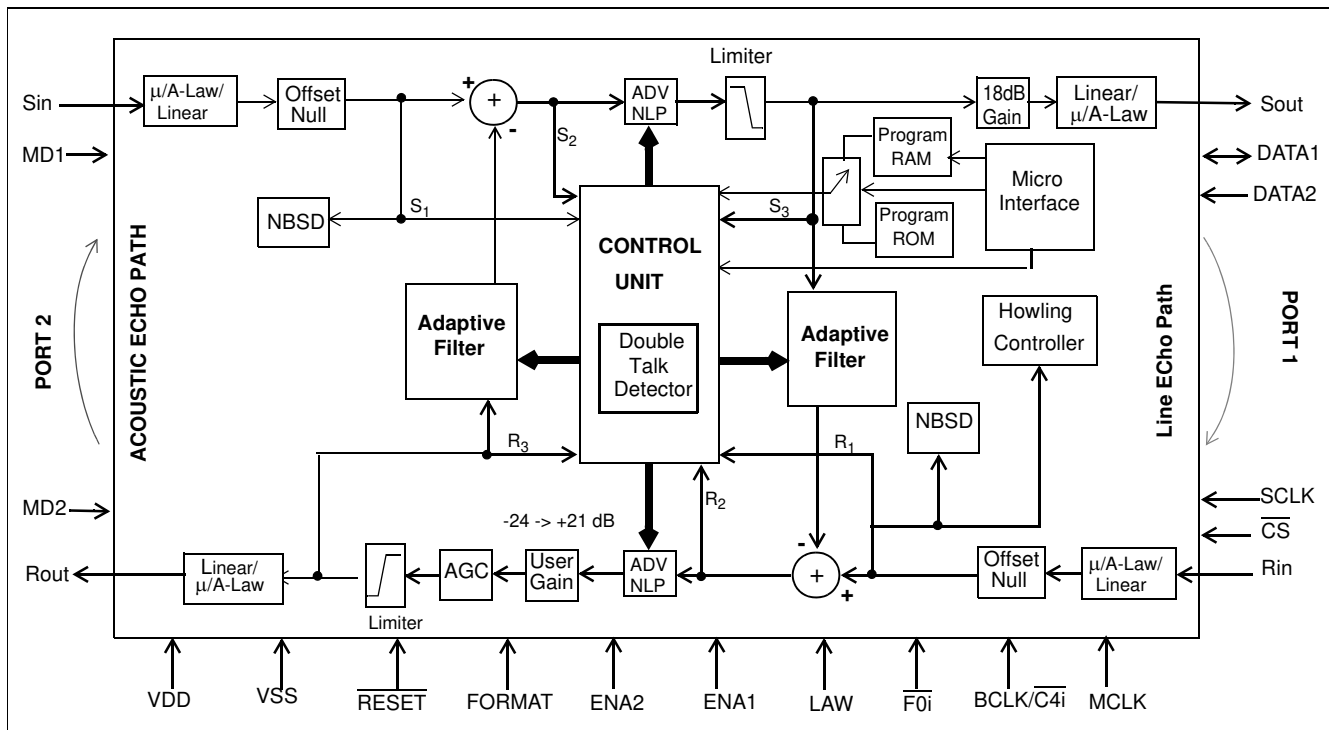


Figure 1 - Functional Block Diagram

Applications

- Hands-free in automobile applications

	MT93L16	ZL38001	ZL38002	ZL38003
Description	AEC for analog hands-free communication	AEC for analog hands-free communication	AEC with noise reduction for digital hands-free communication	AEC with noise reduction & codecs for digital hands-free communication
Application	Analog Desktop phone Analog Intercom	Analog Desktop phone Analog Intercom	Hands-free Car Kits Digital Desktop Phone Home Security Intercom & Pedestals	Hands-free Car Kits Digital Desktop Phone Home Security Intercom & Pedestals
Features				
AEC	1 channel	1 channel	1 channel	1 channel
LEC	1 channel	1 channel	Custom Load	Custom Load
Gains	User Gain	User Gain/18 dB Gain on Sout	User Gain + System tuning gains	User Gain + System tuning gains
Noise Reduction	N	N	Y	Y
Integrated Codecs	N	N	N	dual channel

Table 1 - Acoustic Echo Cancellation Family

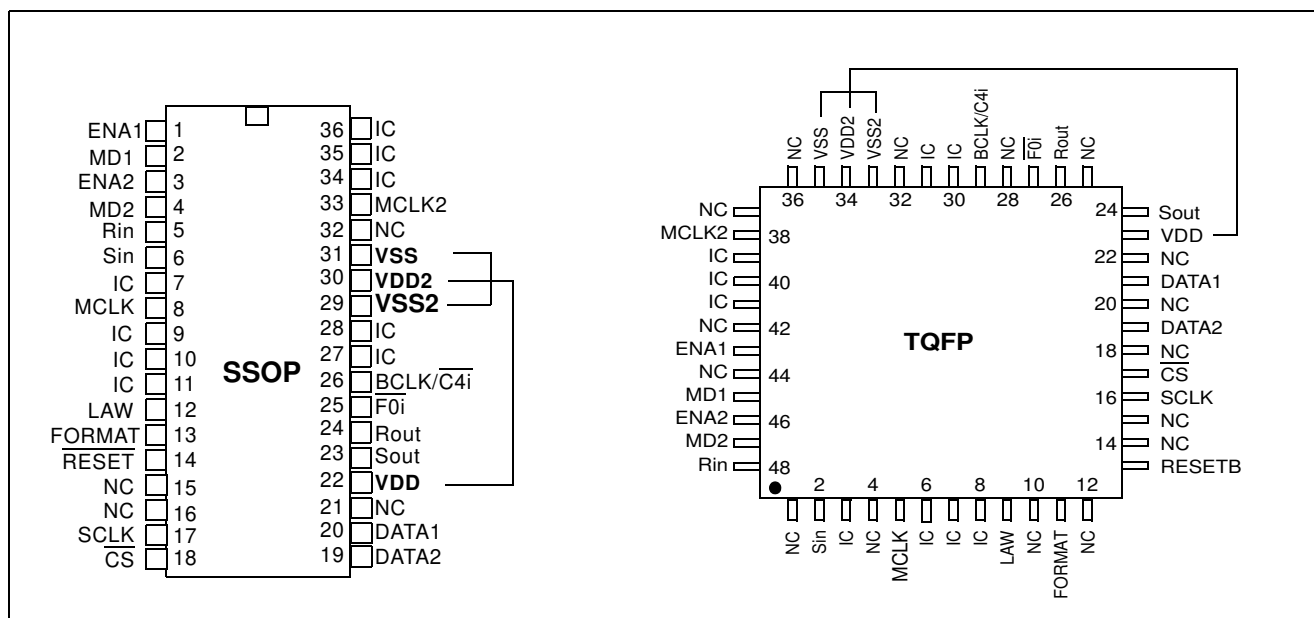


Figure 2 - Pin Connections

Pin Description

SSOP Pin #	TQFP Pin #	Name	Description
1	43	ENA1	SSI Enable Strobe/ST-BUS & GCI Mode for Rin/Sout (Input). This pin has dual functions depending on whether SSI or ST-BUS/GCI is selected. For SSI, this strobe must be present for frame synchronization. This is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer for on Rin/Sout pins. Strobe period is 125 microseconds. For ST-BUS or GCI, this pin, in conjunction with the MD1 pin, selects the proper mode for Rin/Sout pins (see ST-BUS and GCI Operation description).
2	45	MD1	ST-BUS & GCI Mode for Rin/Sout (Input). When in ST-BUS or GCI operation, this pin, in conjunction with the ENA1 pin, will select the proper mode for Rin/Sout pins (see ST-BUS and GCI Operation description). Connect this pin to Vss in SSI mode.
3	46	ENA2	SSI Enable Strobe /ST-BUS & GCI Mode for Sin/Rout (Input). This pin has dual functions depending on whether SSI or ST-BUS/GCI is selected. For SSI, this is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer on Sin/Rout pins. Strobe period is 125 microseconds. For ST-BUS/GCI, this pin, in conjunction with the MD2 pin, selects the proper mode for Sin/Rout pins (see ST-BUS and GCI Operation description).
4	47	MD2	ST-BUS & GCI Mode for Sin/Rout (Input). When in ST-BUS or GCI operation, this pin in conjunction with the ENA2 pin, selects the proper mode for Sin/Rout pins (see ST-BUS and GCI Operation description). Connect this pin to Vss in SSI mode.

Pin Description (continued)

SSOP Pin #	TQFP Pin #	Name	Description
5	48	Rin	Receive PCM Signal Input (Input). 128 kbps to 4096 kbps serial PCM input stream. Data may be in either companded or 2's complement linear format. This is the Receive Input channel from the line (or network) side. Data bits are clocked in following SSI, GCI or ST-BUS timing requirements.
6	2	Sin	Send PCM Signal Input (Input). 128 kbps to 4096 kbps serial PCM input stream. Data may be in either companded or 2's complement linear format. This is the Send Input channel (from the microphone). Data bits are clocked in following SSI, GCI or ST-BUS timing requirements.
7	3	IC	Internal Connection (Input). Must be tied to Vss.
8	5	MCLK	Master Clock (Input). Nominal 20 MHz Master Clock input (may be asynchronous relative to 8 KHz frame signal.) Tie together with MCLK2 (pin 33).
9,10,11	6, 7, 8	IC	Internal Connection (Input). Must be tied to Vss.
12	9	LAW	A/μ Law Select (Input). When low, selects μ -Law companded PCM. When high, selects A-Law companded PCM. This control is for both serial pcm ports.
13	11	FORMAT	ITU-T/Sign Mag (Input). When low, selects sign-magnitude PCM code. When high, selects ITU-T (G.711) PCM code. This control is for both serial pcm ports.
14	13	$\overline{\text{RESET}}$	Reset / Power-down (Input). An active low resets the device and puts the ZL38001 into a low-power stand-by mode.
17	16	SCLK	Serial Port Synchronous Clock (Input). Data clock for the serial microport interface.
18	17	$\overline{\text{CS}}$	Serial Port Chip Select (Input). Enables serial microport interface data transfers. Active low.
19	19	DATA2	Serial Data Receive (Input). In Motorola/National serial microport operation, the DATA2 pin is used for receiving data. In Intel serial microport operation, the DATA2 pin is not used and must be tied to Vss or Vdd.
20	21	DATA1	Serial Data Port (Bidirectional). In Motorola/National serial microport operation, the DATA1 pin is used for transmitting data. In Intel serial microport operation, the DATA1 pin is used for transmitting and receiving data.
22	23	VDD	Positive Power Supply (Input). Nominally 3.3 volts.
23	24	Sout	Send PCM Signal Output (Output). 128 kbps to 4096 kbps serial PCM output stream. Data may be in either companded or 2's complement linear PCM format. This is the Send Out signal after acoustic echo cancellation and non-linear processing. Data bits are clocked out following SSI, ST-BUS or GCI timing requirements.
24	26	Rout	Receive PCM Signal Output (Output). 128 kbps to 4096 kbps serial PCM output stream. Data may be in either companded or 2's complement linear PCM format. This is the Receive out signal after line echo cancellation non-linear processing, AGC and gain control. Data bits are clocked out following SSI, ST-BUS or GCI timing requirements.

Pin Description (continued)

SSOP Pin #	TQFP Pin #	Name	Description
25	27	$\overline{F0i}$	Frame Pulse (Input). In ST-BUS (or GCI) operation, this is an active-low (or active-high) frame alignment pulse, respectively. SSI operation is enabled by connecting this pin to Vss.
26	29	BCLK/ $\overline{C4i}$	Bit Clock/ST-BUS Clock (Input). In SSI operation, BCLK pin is a 128 kHz to 4.096 MHz bit clock. This clock must be synchronous with ENA1 and ENA2 enable strobes. In ST-BUS or GCI operation, $\overline{C4i}$ pin must be connected to the 4.096 MHz (C4) system clock.
27, 28	30, 31	IC	Internal Connection (Input). Tie to Vss.
29	33	VSS2	Digital Ground (Input). Nominally 0 volts.
30	34	VDD2	Positive Power Supply (Input). Nominally 3.3 volts (tie together with VDD, pin 22).
31	35	VSS	Digital Ground (Input). Nominally 0 volts (tie together with VSS2, pin 29).
33	38	MCLK2	Master Clock (Input). Nominal 20 MHz master clock (tie together with MCLK, pin 8).
34,35,36	39, 40, 41	IC	Internal Connection (Input). Tie to Vss.
15, 16, 21, 32	1, 4, 10, 12, 14, 15, 18, 20, 22, 25, 28, 32, 36, 37, 42, 44	NC	No Connect (Output). This pin should be left unconnected.

Table of Contents

1.0 Changes Summary	10
2.0 Functional Description	10
2.1 Adaptation Speed Control	10
2.2 Advanced Non-Linear Processor (ADV-NLP)1	11
2.3 Narrow Band Signal Detector (NBSD)	11
2.4 Howling Detector (HWLD)1	11
2.5 Offset Null Filter	11
2.6 Limiters	11
2.7 User Gain	11
2.8 AGC	12
2.9 18 dB Gain Pad at Sout	12
2.10 Mute Function	12
2.11 Bypass Control	13
2.12 Adaptation Enable/Disable	13
2.13 ZL38001 Throughput Delay	13
2.14 Power Down / Reset	13
3.0 PCM Data I/O	14
3.1 ST-BUS and GCI Operation	14
3.2 SSI Operation	17
3.3 PCM Law and Format Control (LAW, FORMAT)	18
3.4 Linear PCM	19
3.5 Bit Clock (BCLK/C4i)	19
3.6 Master Clock (MCLK)	19
4.0 Microport	19
4.1 Bootload Process and Execution from RAM	20
5.0 Register Summary	30

List of Figures

Figure 1 - Functional Block Diagram	1
Figure 2 - Pin Connections	3
Figure 3 - ST-BUS and GCI 8-Bit Companded PCM I/O on Timeslot 0 (Mode 1)	14
Figure 4 - ST-BUS and GCI 8-Bit Companded PCM I/O on Timeslot 2 (Mode 2)	15
Figure 5 - ST-BUS and GCI 8-Bit Companded PCM I/O with D and C channels (Mode 3)	16
Figure 6 - ST-BUS and GCI 16-Bit 2's Complement Linear PCM I/O (Mode 4)	17
Figure 7 - SSI Operations	18
Figure 8 - Serial Microport Timing for Intel Mode 0	22
Figure 9 - Serial Microport Timing for Motorola Mode 00 or National Microwire	23
Figure 10 - Master Clock - MCLK	26
Figure 11 - GCI Data Port Timing	27
Figure 12 - ST-BUS Data Port Timing	27
Figure 13 - SSI Data Port Timing	28
Figure 14 - INTEL Serial Microport Timing	28
Figure 15 - Motorola Serial Microport Timing	29

List of Tables

Table 1 - Acoustic Echo Cancellation Family	2
Table 2 - Quiet PCM Code Assignment	12
Table 3 - ST-BUS & GCI Mode Select	17
Table 4 - SSI Enable Strobe Pins	18
Table 5 - Companded PCM	19
Table 6 - Bootload RAM Control (BRC) Register States	21
Table 7 - Reference Level Definition for Timing Measurements	26

List of Register Tables

Register Table 1 - Main Control Register (MC)	30
Register Table 2 - Acoustic Echo Canceller Control Register (AEC)	30
Register Table 3 - Line Echo Canceller Control Register (LEC)	31
Register Table 4 - Acoustic Echo Canceller Status Register (ASR) (* Do not write to this register)	32
Register Table 5 - Line Echo Canceller Status Register (LSR) (* Do not write to this register)	33
Register Table 6 - Receive Gain Control Register	34
Register Table 7 - Double Talk Gain Control Register 1 (DTGCR1)	35
Register Table 8 - Double Talk Gain Control Register 2 (DTGCR2)	35
Register Table 9 - Double Talk detection Threshold Register (DTDT)	36
Register Table 10 - Receive (Rin) Peak Detect Register 1 (RIPD1)	36
Register Table 11 - Receive (Rin) Peak Detect Register 2 (RIPD2)	37
Register Table 12 - Receive (Rin) ERROR Peak Detect Register 1 (REPD1)	37
Register Table 13 - Receive (Rin) ERROR Peak Detect Register 2 (REPD2)	38
Register Table 14 - Receive (Rout) Peak Detect Register 1 (ROPD1)	38
Register Table 15 - Receive (Rout) Peak Detect Register 2 (ROPD2)	39
Register Table 16 - Send (Sin) Peak Detect Register 1 (SIPD1)	39
Register Table 17 - Send (Sin) Peak Detect Register 2 (SIPD2)	40
Register Table 18 - Send ERROR Peak Detect Register 1 (SEPD1)	40
Register Table 19 - Send ERROR Peak Detect Register 2 (SEPD2)	41
Register Table 20 - Send (Sout) Peak Detect Register 1 (SOPD1)	41
Register Table 21 - Send (Sout) Peak Detect Register 2 (SOPD2)	42
Register Table 22 - Rout Limiter Register 1 (RL1)	42
Register Table 23 - Rout Limiter Register 2 (RL2)	43
Register Table 24 - Sout Limiter Register (SL)	43
Register Table 25 - Firmware Revision Code Register (FRC)	44
Register Table 26 - Bootload RAM Control Register (BRC)	44
Register Table 27 - Bootload RAM Signature Register (SIG)	45

1.0 Changes Summary

The following table captures the changes from the October 2006 issue.

Page	Item	Change
1	Ordering Information Box	Removed the ZL38001QDC and ZL38001DGA packages.
3	“Pin Description“ Table	Removed QSOP Pin Descriptions.
3	“Pin Description“ Table	Added SSOP Pin Descriptions.
46	QSOP Package Outline	Removed mechanical drawing of the QSOP package.
46	SSOP Package Outline	Added mechanical drawing of the SSOP package.

2.0 Functional Description

The ZL38001 device contains an acoustic echo cancellers, as well as the many control functions necessary to operate the echo canceller. The ZL38001 provides clear signal transmission in both audio path directions to ensure reliable voice communication, even with low level signals. The ZL38001 does not use variable attenuators during double-talk or single-talk periods of speech, as do many other acoustic echo cancellers for speakerphones. Instead, the ZL38001 provides high performance full-duplex operation similar to network echo cancellers, so that users experience clear speech and uninterrupted background signals during the conversation. This prevents subjective sound quality problems associated with “noise gating” or “noise contrasting”.

The ZL38001 uses an advanced adaptive filter algorithm that is double-talk stable, which means that convergence takes place even while both parties are talking¹. This algorithm allows continual tracking of changes in the echo path, regardless of double-talk, as long as a reference signal is available for the echo canceller.

The echo tail cancellation capability of the acoustic echo canceller has been sized appropriately (112 ms) to cancel echo in an average sized office with a reverberation time of less than 112 ms.

In addition to the echo cancellers, the following functions are supported:

- Control of adaptive filter convergence speed during periods of double-talk, far end single-talk and near-end echo path changes
- Control of Non-Linear Processor thresholds for suppression of residual non-linear echo
- Howling detector to identify when instability is starting to occur and to take action to prevent oscillation
- Narrow-Band Detector for preventing adaptive filter divergence caused by narrow-band signals
- Offset Nulling filters for removal of DC components in PCM channels
- Limiters that introduce controlled saturation levels
- Serial controller interface compatible with Motorola, National and Intel microcontrollers
- PCM encoder/decoder compatible with μ /A-Law ITU-T G.711, μ /A-Law Sign-Mag or linear 2's complement coding
- Automatic gain control on the receive speaker path

2.1 Adaptation Speed Control

The adaptation speed of the acoustic echo canceller is designed to optimize the convergence speed versus divergence caused by interfering near-end signals. Adaptation speed algorithm takes into account many different

1. Patent pending.

factors such as relative double-talk condition, far end signal power, echo path change and noise levels to achieve fast convergence.

2.2 Advanced Non-Linear Processor (ADV-NLP)¹

After echo cancellation, there is likely to be residual echo which needs to be removed so that it will not be audible. The ZL38001 uses an NLP to remove low level residual echo signals which are not comprised of background noise. The operation of the NLP depends upon a dynamic activation threshold, as well as a double-talk detector which disables the NLP during double-talk periods.

The ZL38001 keeps the perceived noise level constant, without the need for any variable attenuators or gain switching that causes audible “noise gating”. The noise level is constant and identical to the original background noise even when the NLP is activated.

The NLP can be disabled by setting the NLP- bit to 1 in the AEC control registers.

2.3 Narrow Band Signal Detector (NBSD)¹

Single or multi-frequency tones (e.g., DTMF or signalling tones) present in the reference input of an echo canceller for a prolonged period of time may cause the adaptive filter to diverge. The Narrow Band Signal Detector (NBSD) is designed to prevent this divergence by detecting single or multi-tones of arbitrary frequency, phase, and amplitude. When narrow band signals are detected, the filter adaptation process is stopped but the echo canceller continues to cancel echo.

The NBSD can be disabled by setting the NB- bit to 1 in the MC control registers.

2.4 Howling Detector (HWLD)¹

The Howling detector is part of an Anti-Howling control, designed to prevent oscillation as a result of positive feedback in the audio paths.

The HWLD can be disabled by setting the AH- bit to 1 in the (MC) control register.

2.5 Offset Null Filter

To ensure robust performance of the adaptive filters at all times, any DC offset that may be present on either the Rin signal or the Sin signal, is removed by highpass filters. These filters have a corner frequency placed at 40 Hz.

The offset null filters can be disabled by setting the HPF- bit to 1 in the AEC control registers.

2.6 Limiters

To prevent clipping in the echo paths, two limiters with variable thresholds are provided at the outputs.

The Rout limiter threshold is in Rout Limiter Register 1 and 2. The Sout limiter threshold is in Sout Limiter Register. Both output limiters are always enabled.

2.7 User Gain

The user gain function provides the ability for users to adjust the audio gain in the receive path (speaker path). This gain is adjustable from -24 dB to +48 dB in 3 dB steps. It is important to use ONLY this user gain function to adjust the speaker volume. The user gain function in the ZL38001 is optimally placed between the two echo cancellers such that no reconvergence is necessary after gain changes.

The gain can be accessed through Receive Gain Control Register.

1. Patent Pending

2.8 AGC

The AGC function is provided to limit the volume in the speaker path. The gain of the speaker path is automatically reduced during the following conditions:

- When clipping of the receive signal occurs
- When initial convergence of the acoustic echo canceller detects unusually large echo return
- When howling is detected
- The AGC can be disabled by setting the AGC- bit to 1 in MC control register

2.9 18 dB Gain Pad at Sout

The purpose of the 18 dB gain pad is to improve the subjective quality in low ERL environments. The ZL38001 can cancel echo with a ERL as low as 0 dB (attenuation from Rout to Sin). In many hand free applications, the ERL can be low (or negative). This is due to both speaker and microphone gain setting. The speaker gain has to be set high enough for the speaker to be heard properly and the microphone gain needs to be set high enough to ensure sufficient signal is sent to the far end. If the ERL (Acoustic Attenuation - speaker gain - microphone gain) is greater than 0 dB, then the echo canceller cannot cancel echo. To overcome this limitation, the ZL38001 has a 18 dB gain pad at Sout. The microphone gain can be reduced by 18 dB to allow either the speaker gain and/or the acoustic coupling to be increased by a total of 18 dB allowing more flexibility in the design.

2.10 Mute Function

A pcm mute function is provided for independent control of the Receive and Send audio paths. Setting the MUTE_R or MUTE_S bit in the MC register, causes quiet code to be transmitted on the Rout or Sout paths respectively.

Quiet code is defined according to the following table.

	LINEAR 16 bits 2's complement	SIGN/ MAGNITUDE μ -Law A-Law	CCITT (G.711)	
			μ -Law	A-Law
+Zero (quiet code)	0000h	80h	FFh	D5h

Table 2 - Quiet PCM Code Assignment

2.11 Bypass Control

A PCM bypass function is provided to allow transparent transmission of pcm data through the ZL38001. When the bypass function is active, pcm data passes transparently from Rin to Rout and from Sin to Sout, with bit-wise integrity preserved.

When the Bypass function is selected, most internal functions are powered down to provide low power consumption.

The BYPASS control bit is located in the main control MC register.

2.12 Adaptation Enable/Disable

Adaptation control bits are located in the AEC and LEC control registers. When the ADAPT- bit is set to 1, the adaptive filter is frozen at the current state. In this state, the device continues to cancel echo with the current echo model.

When the ADAPT- bit is set to 0, the adaptive filter is continually updated. This allows the echo canceller to adapt and track changes in the echo path. This is the normal operating state.

2.13 ZL38001 Throughput Delay

In all modes, voice channels always have 2 frames of delay. In ST-BUS/GCI operation, the D and C channels have a delay of one frame.

2.14 Power Down / Reset

Holding the $\overline{\text{RESET}}$ pin at logic low will keep the ZL38001 device in a power-down state. In this state all internal clocks are halted, and the DATA1, Sout and Rout pins are tristated.

The user should hold the $\overline{\text{RESET}}$ pin low for at least 200 msec following power-up. This will insure that the device powers up in a proper state. Following any return of $\overline{\text{RESET}}$ to logic high, the user must wait for 8 complete 8 KHz frames prior to writing to the device registers. During this time, the initialization routines will execute and set the ZL38001 to default operation (program execution from ROM using default register values).

3.0 PCM Data I/O

The PCM data transfer for the ZL38001 is provided through two PCM ports. One port consists of Rin and Sout pins while the second port consists of Sin and Rout pins. The data are transferred through these ports according to either ST-BUS, GCI or SSI conventions and the device automatically detects the correct convention. The device determines the convention by monitoring the signal applied to the F0i pin. When a valid ST-BUS (active low) frame pulse is applied to the F0i pin, the ZL38001 will assume ST-BUS operation. When a valid GCI (active high) frame pulse is applied to the F0i pin, the device will assume GCI operation. If F0i is tied continuously to Vss, the device will assume SSI operation. Figures 11 to 13 show timing diagrams of these 3 PCM-interface operation conventions.

3.1 ST-BUS and GCI Operation

The ST-BUS PCM interface conforms to Zarlink's ST-BUS standard with an active-low frame pulse. Input data is clocked in by the rising edge of the bit clock (C4i) three-quarters of the way into the bitcell and output data bit boundaries (Rout, Sout) occur every second falling edge of the bit clock (see Figure 11.) The GCI PCM interface corresponds to the GCI standard commonly used in Europe with an active-high frame pulse. Input data is clocked in by the falling edge of the bit clock (C4i) three-quarters of the way into the bitcell and output data bit boundaries (Rout, Sout) occur every second rising edge of the bit clock (see Figure 12.)

Either of these interfaces (STBUS or GCI) can be used to transport 8 bit companded PCM data (using one timeslot) or 16 bit 2's complement linear PCM data (using two timeslots). The MD1/ENA1 pins select the timeslot on the Rin/Sout port while the MD2/ENA2 pin selects the timeslot on the Sin/Rout port, as in Table 3. Figures 3 to 6 illustrate the timeslot allocation for each of these four modes.

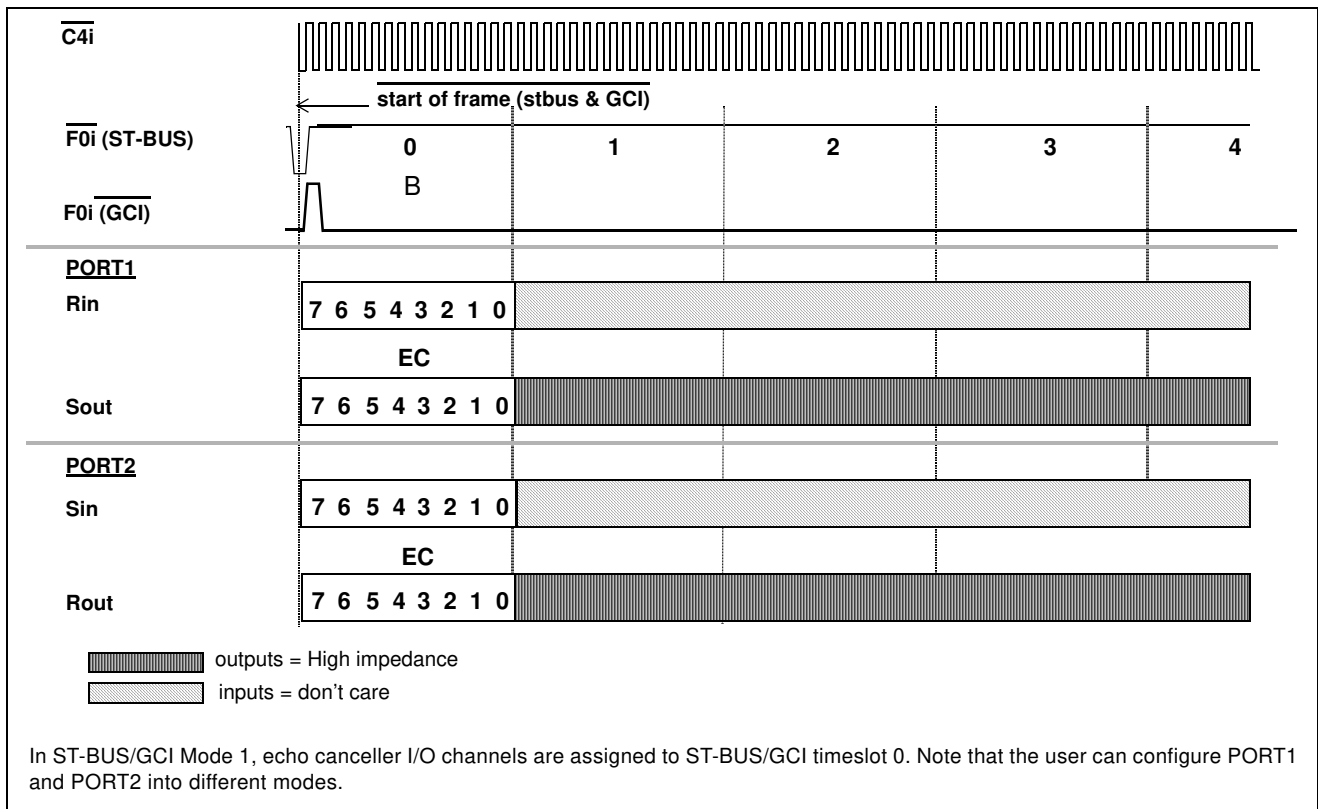


Figure 3 - ST-BUS and GCI 8-Bit Companded PCM I/O on Timeslot 0 (Mode 1)

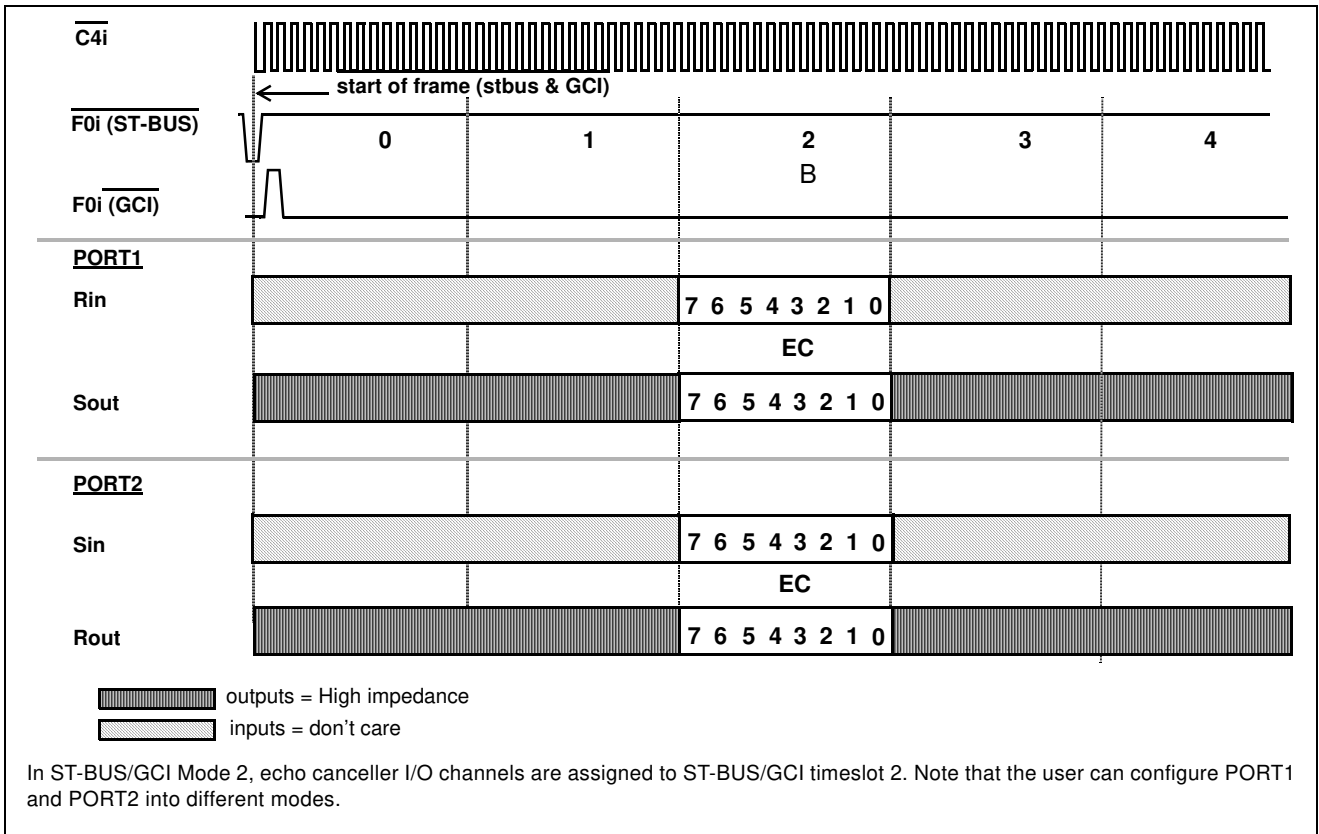


Figure 4 - ST-BUS and GCI 8-Bit Companded PCM I/O on Timeslot 2 (Mode 2)

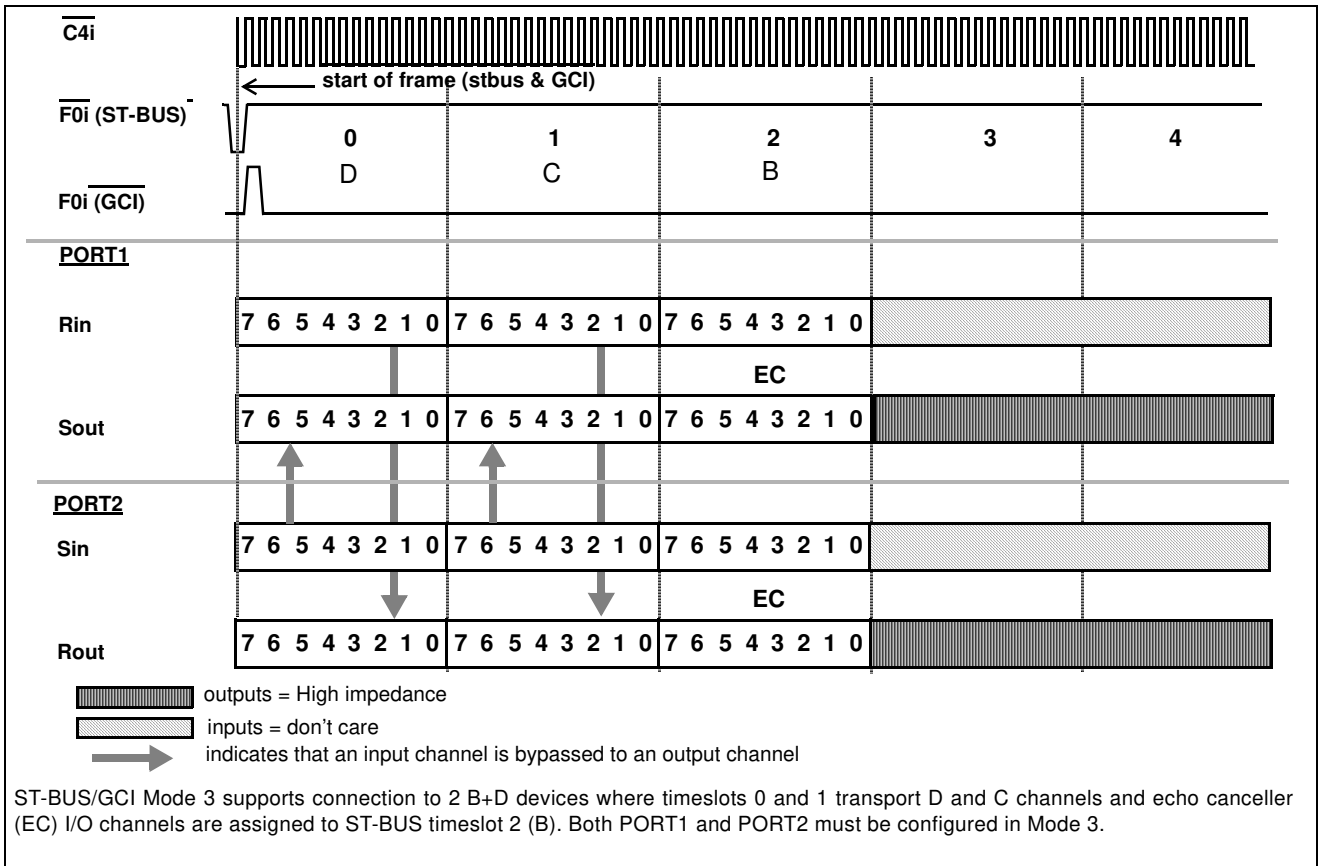


Figure 5 - ST-BUS and GCI 8-Bit Companded PCM I/O with D and C channels (Mode 3)

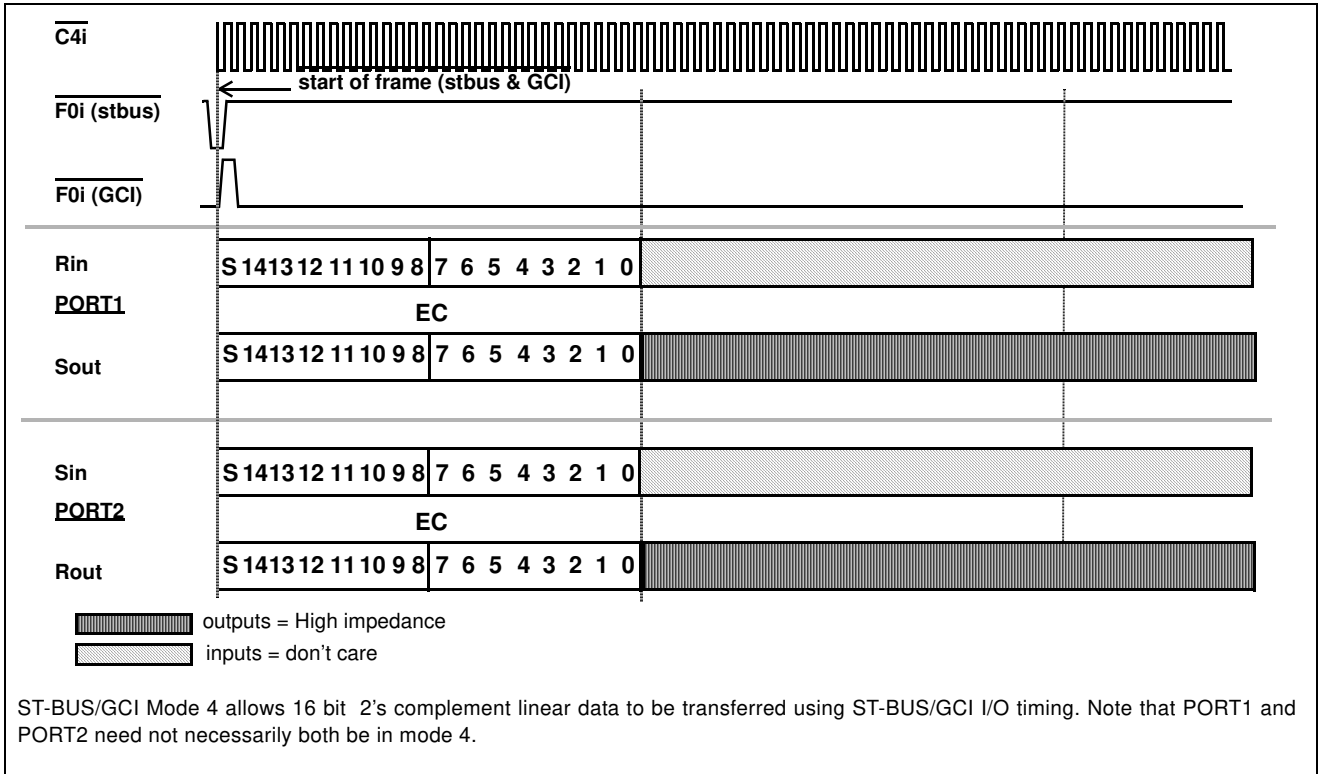


Figure 6 - ST-BUS and GCI 16-Bit 2's Complement Linear PCM I/O (Mode 4)

PORT1 Rin/Sout		ST-BUS/GCI Mode Selection	PORT2 Sin/Rout	
Enable Pins			Enable Pins	
MD1	ENA1		MD2	ENA2
0	0	Mode 1. 8 bit companded PCM I/O on timeslot 0	0	0
0	1	Mode 2. 8 bit companded PCM I/O on timeslot 2.	0	1
1	0	Mode 3. 8 bit companded PCM I/O on timeslot 2. Includes D & C channel bypass in timeslots 0 & 1.	1	0
1	1	Mode 4. 16-bit 2's complement linear PCM I/O on timeslots 0 & 1.	1	1

Table 3 - ST-BUS & GCI Mode Select

3.2 SSI Operation

The SSI PCM interface consists of data input pins (Rin, Sin), data output pins (Sout, Rout), a variable rate bit clock (BCLK), and two enable pins (ENA1, ENA2) to provide strobes for data transfers. The active high enable may be either 8 or 16 BCLK cycles in duration. Automatic detection of the data type (8 bit companded or 16-bit 2's complement linear) is accomplished internally. The data type cannot change dynamically from one frame to the next.

In SSI operation, the frame boundary is determined by the rising edge of the ENA1 enable strobe (see Figure 7). The other enable strobe (ENA2) is used for parsing input/output data and it must pulse within 125 microseconds of the rising edge of ENA1.

In SSI operation, the enable strobes may be a mixed combination of 8 or 16 BCLK cycles allowing the flexibility to mix 2's complement linear data on one port (e.g., Rin/Sout) with companded data on the other port (e.g., Sin/Rout).

Enable Strobe Pin	Designated PCM I/O Port
ENA1	Line Side Echo Path (PORT 1)
ENA2	Acoustic Side Echo Path (PORT 2)

Table 4 - SSI Enable Strobe Pins

3.3 PCM Law and Format Control (LAW, FORMAT)

The PCM companding/coding law used by the ZL38001 is controlled through the LAW and FORMAT pins. ITU-T G.711 companding curves for μ -Law and A-Law are selected by the LAW pin. PCM coding ITU-T G.711 and Sign-Magnitude are selected by the FORMAT pin. See Table 5.

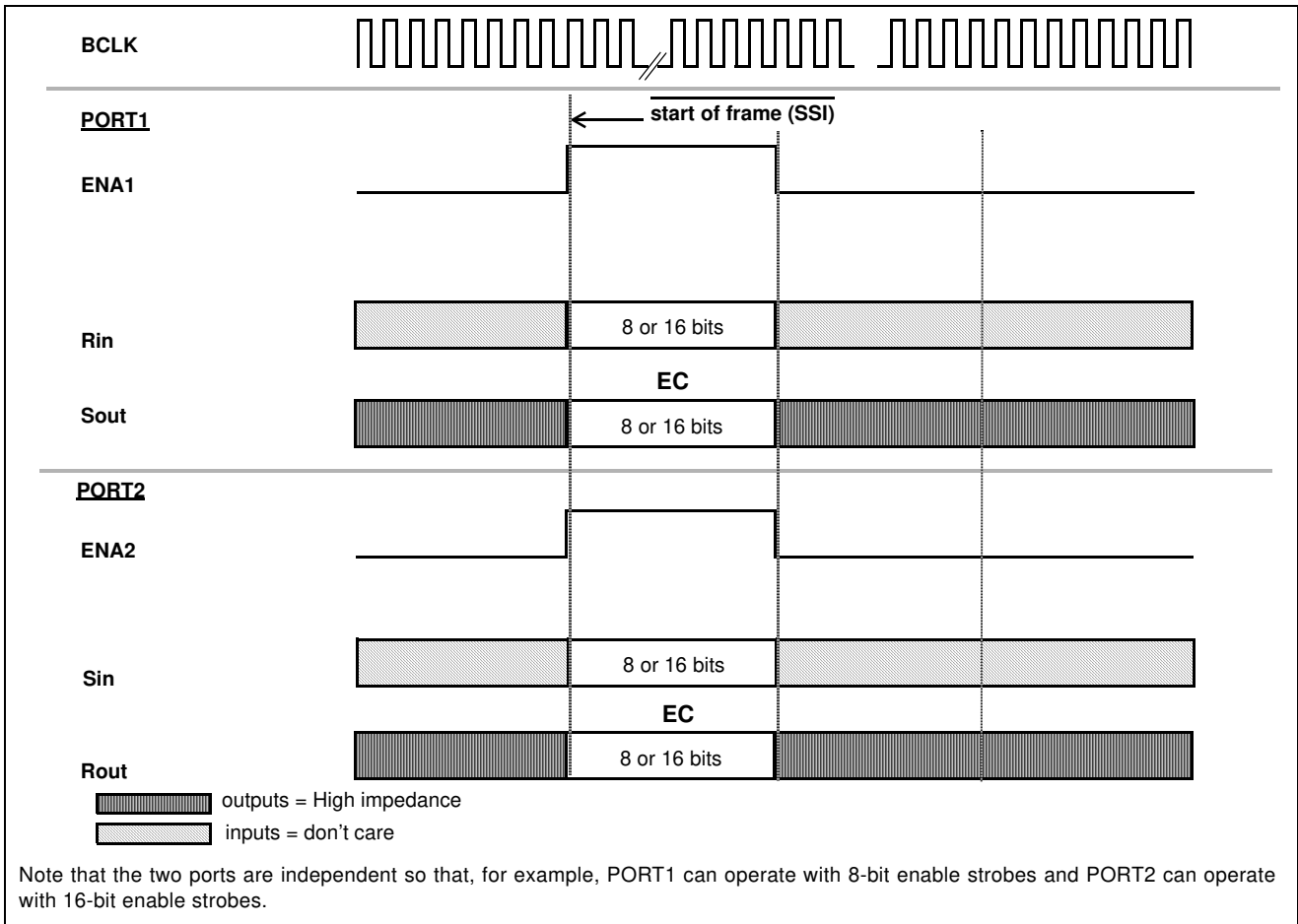


Figure 7 - SSI Operations

PCM Code	Sign-Magnitude	ITU-T (G.711)	
	FORMAT=0	FORMAT=1	
	μ /A-LAW LAW = 0 or 1	μ -LAW LAW = 0	A-LAW LAW = 1
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
- Zero	0000 0000	0111 1111	0101 0101
- Full Scale	0111 1111	0000 0000	0010 1010

Table 5 - Companded PCM

3.4 Linear PCM

The 16-bit 2's complement PCM linear coding permits a dynamic range beyond that which is specified in ITU-T G.711 for companded PCM. The echo-cancellation algorithm will accept 16-bits 2's complement linear code which gives a maximum signal level of +15 dBm0.

3.5 Bit Clock (BCLK/ $\overline{C4i}$)

The BCLK/ $\overline{C4i}$ pin is used to clock the PCM data for GCI and ST-BUS ($\overline{C4i}$) interfaces, as well as for the SSI (BCLK) interface.

In SSI operation, the bit rate is determined by the BCLK frequency. This input must contain either eight or sixteen clock cycles within the valid enable strobe window. BCLK may be any rate between 128 KHz to 4.096 MHz and can be discontinuous outside of the enable strobe windows defined by ENA1, ENA2 pins. Incoming PCM data (Rin, Sin) are sampled on the falling edge of BCLK while outgoing PCM data (Sout, Rout) are clocked out on the rising edge of BCLK. See Figure 13.

In ST-BUS and GCI operation, connect the system $\overline{C4}$ (4.096 MHz) clock to the $\overline{C4i}$ pin.

3.6 Master Clock (MCLK)

A nominal 20 MHz, continuously-running master clock (MCLK) is required. MCLK may be asynchronous with the 8 KHz frame.

4.0 Microport

The serial microport provides access to all ZL38001 internal read and write registers, plus write-only access to the bootloadable program RAM (see next section for bootload description.) This microport is compatible with Intel MCS-51 (mode 0), Motorola SPI (CPOL=0, CPHA=0) and National Semiconductor Microwire specifications. The microport consists of a transmit/receive data pin (DATA1), a receive data pin (DATA2), a chip select pin (\overline{CS}) and a synchronous data clock pin (SCLK).

The ZL38001 automatically adjusts its internal timing and pin configuration to conform to Intel or Motorola/National requirements. The microport dynamically senses the state of the SCLK pin each time \overline{CS} pin becomes active (i.e., high to low transition). If SCLK pin is high during \overline{CS} activation, then Intel mode 0 timing is assumed. In this case DATA1 pin is defined as a bi-directional (transmit/receive) serial port and DATA2 is internally disconnected. If SCLK is low during \overline{CS} activation, then Motorola/National timing is assumed and DATA1 is defined as the data transmit pin while DATA2 becomes the data receive pin. The ZL38001 supports Motorola half-duplex processor mode (CPOL=0

and CPHA=0). This means that during a write to the ZL38001, by the Motorola processor, output data from the DATA1 pin must be ignored. This also means that input data on the DATA2 pin is ignored by the ZL38001 during a valid read by the Motorola processor.

All data transfers through the microport are two bytes long. This requires the transmission of a Command/Address byte followed by the data byte to be written to or read from the addressed register. CS must remain low for the duration of this two-byte transfer. As shown in Figures 8 and 9, the falling edge of CS indicates to the ZL38001 that a microport transfer is about to begin. The first 8 clock cycles of SCLK after the falling edge of CS are always used to receive the Command/Address byte from the microcontroller. The Command/Address byte contains information detailing whether the second byte transfer will be a read or a write operation and at what address. The next 8 clock cycles are used to transfer the data byte between the ZL38001 and the microcontroller. At the end of the two-byte transfer, \overline{CS} is brought high again to terminate the session. The rising edge of \overline{CS} will tri-state the DATA1 pin. The DATA1 pin will remain tri-stated as long as \overline{CS} is high.

Intel processors utilize Least Significant Bit (LSB) first transmission while Motorola/National processors use Most Significant Bit (MSB) first transmission. The ZL38001 microport automatically accommodates these two schemes for normal data bytes. However, to ensure timely decoding of the R/W and address information, the Command/Address byte is defined differently for Intel and Motorola/National operations. Refer to the relative timing diagrams of Figure 8 and Figure 9. Receive data bits are sampled on the rising edge of SCLK while transmit data is clocked out on the falling edge of SCLK. Detailed microport timing is shown in Figure 14 and Figure 15.

4.1 Bootload Process and Execution from RAM

A bootloadable program RAM (BRAM) is available on the ZL38001 to support factory-issued software upgrades to the built-in algorithm. To make use of this bootload feature, users must include 4096 X 8 bits of memory in their microcontroller system (i.e., external to the ZL38001), from which the ZL38001 can be bootloaded. Registers and program data are loaded into the ZL38001 in the same fashion via the serial microport. Both employ the same command / address / data byte specification described in the previous section on serial microport. Either intel or motorola mode may be transparently used for bootloading. There are also two registers relevant to bootloading (BRC=control and SIG=signature, see Register Summary). The effect of these register values on device operation is summarized in Table 6.

Bootload mode is entered and exited by writing to the bootload bit in the Bootload RAM Control (BRC) register at address 3fh (see Register Summary). During bootload mode, any serial microport "write" (R/W command bit =0) to an address other than that of the BRC register will contribute to filling the program BRAM. Call these transactions "BRAM-fill" writes. Although a command/address byte must still precede each data byte (as described for the serial microport), the values of the address fields for these "BRAM-fill" writes are ignored (except for the value 3fh, which designates the BRC register.) Instead, addresses are internally generated by the ZL38001 for each "BRAM-fill" write. Address generation for "BRAM-fill" writes resumes where it left off following any read transaction while bootload mode is enabled. The first 4096 such "BRAM-fill" writes while bootload is enabled will load the memory, but further ones after that are ignored. Following the write of the first 4096 bytes, the program BRAM will be filled. Before bootload *mode is disabled*, it is recommended that users then read back the value from the signature register (SIG) and compare it to the one supplied by the factory along with the code. Equality verifies that the correct data has been loaded. The signature calculation uses an 8-bit MISR which only incorporates input from "BRAM-fill" writes. Resetting the bootload bit (C_2) in the BRC register to 0 (see Register Summary) exits bootload mode, resetting the signature (SIG) register and internal address generator for the next bootload. A hardware reset (RESET=0) similarly returns the ZL38001 to the ready state for the start of a bootload.

FUNCTIONAL DESCRIPTION FOR USING THE BOOTABLE RAM			
BOOTLOAD MODE - Microport Access is to bootload RAM (BRAM)			
BRC Register Bits C ₃ C ₂ C ₁ C ₀ X 1 0 0	R/W	Address	Data
	W	3fh (= 1 1 1 1 1 b)	Writes "data" to BRC reg. - Bootload frozen; BRAM contents are NOT affected.
	W	other than 3fh	Writes "data" to next byte in BRAM (bootloading.)
	R	1 x x x x b	Reads back "data" = BRC reg value. - Bootload frozen; BRAM contents are NOT affected.
	R	0 x x x x b	Reads back "data" = SIG reg value. - Bootload frozen; BRAM contents are NOT affected.
NON-BOOTLOAD MODE - Microport Access is to device registers (DREGs)			
BRC Register Bits C ₃ C ₂ C ₁ C ₀ X 0 0 0	R/W	Address	Data
	W	any (= a ₅ a ₄ a ₃ a ₂ a ₁ a ₀ b)	Writes "data" to corresponding DREG.
	R	any (= a ₅ a ₄ a ₃ a ₂ a ₁ a ₀ b)	Reads back "data" = corresponding DREG value.
PROGRAM EXECUTION MODES			
C ₃ C ₂ C ₁ C ₀ 0 0 0 0	Execute program in ROM, bootload mode disabled. - BRAM address counter reset to initial (ready) state. - SIG reg reseeded to initial (ready) state		
C ₃ C ₂ C ₁ C ₀ 0 1 0 0	Execute program in ROM, while bootloading the RAM. - BRAM address counter increments on microport writes (except to 3fh) - SIG reg recalculates signature on microport writes (except to 3fh)		
C ₃ C ₂ C ₁ C ₀ 1 0 0 0	Execute program in RAM, bootload mode disabled. - BRAM address counter reset to initial (ready) state. - SIG reg reseeded to initial (ready) state		
C ₃ C ₂ C ₁ C ₀ 1 1 0 0	- NOT RECOMMENDED - (Execute program in RAM, while bootloading the RAM)		

Table 6 - Bootload RAM Control (BRC) Register States

Note: bits C₁ C₀ are reserved, and must be set to zero.

Once the program has been loaded, to begin execution from RAM, bootload mode must be disabled (BOOT bit, $C_2=0$) and execution from RAM enabled (RAM_ROMb bit, $C_3=1$) by setting the appropriate bits in the BRC register. During the bootload process, however, ROM program execution (RAM_ROMb bit, $C_3=0$) should be selected. See Table 6 for the effect of the BRC register settings on Microport accesses and on program execution.

Following program loading and enabling of execution from RAM, it is recommended that users set the software reset bit in the Main Control (MC) register, to ensure that the device updates the default register values to those of the new program in RAM. Note: it is important to use a software reset rather than a hardware ($\overline{RESET}=0$) reset, as the latter will return the device to its default settings (which includes execution from program ROM instead of RAM.)

To verify which code revision is currently running, users can access the Firmware Revision Code (FRC) register (see Register Summary). This register reflects the identity code (revision number) of the last program to run register initialization (which follows a software or hardware reset.)

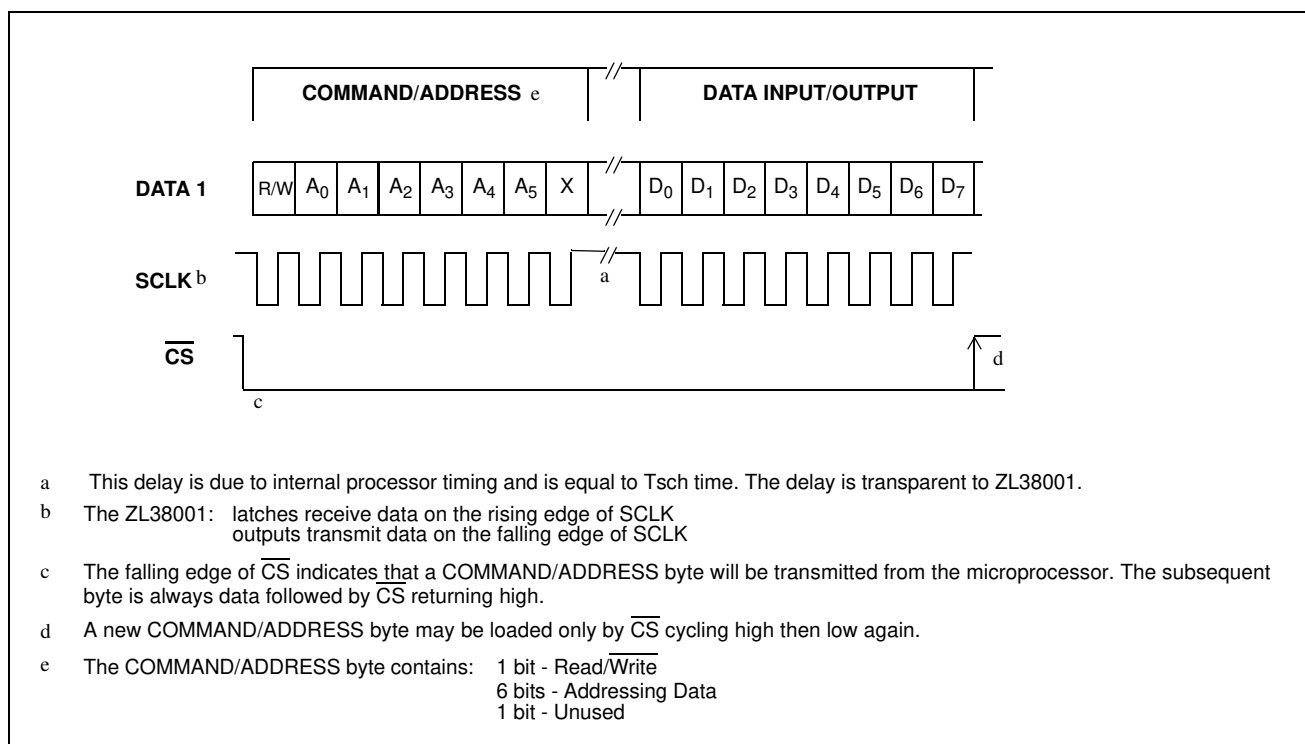


Figure 8 - Serial Microport Timing for Intel Mode 0

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	$V_{DD}-V_{SS}$	-0.5	5.0	V
2	Input Voltage	V_i	$V_{SS}-0.3$	5.5	V
3	Output Voltage Swing	V_o	$V_{SS}-0.3$	5.5	V
4	Continuous Current on any digital pin	$I_{i/o}$		± 20	mA
5	Storage Temperature	T_{ST}	-65	150	°C
6	Package Power Dissipation	P_D		90 (typ)	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Supply Voltage	V_{DD}	2.7	3.3	3.6	V	
2	Input High Voltage		1.4		V_{DD}	V	
3	Input Low Voltage		V_{SS}		0.4	V	
4	Operating Temperature	T_A	-40		+85	°C	

Echo Return Limits

	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
1	Acoustic Echo Return			0	dB	Measured from Rout -> Sin
2	Line Echo Return			0	dB	Measured from Sout -> Rin

DC Electrical Characteristics* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Conditions/Notes
1	Standby Supply Current:	I_{CC}		3	70	μA	$\overline{RESET} = 0$
	Operating Supply Current:	I_{DD}		20		mA	$\overline{RESET} = 1$, clocks active
2	Input HIGH voltage	V_{IH}	$0.7V_{DD}$			V	
3	Input LOW voltage	V_{IL}			$0.3V_{DD}$	V	
4	Input leakage current	I_{IH}/I_{IL}		0.1	10	μA	$V_{IN}=V_{SS}$ to V_{DD}
5	High level output voltage	V_{OH}	$0.8V_{DD}$			V	$I_{OH}=2.5$ mA
6	Low level output voltage	V_{OL}			$0.4V_{DD}$	V	$I_{OL}=5.0$ mA
7	High impedance leakage	I_{OZ}		1	10	μA	$V_{IN}=V_{SS}$ to V_{DD}
8	Output capacitance	C_o		10		pF	
9	Input capacitance	C_i		8		pF	

[‡] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

*DC Electrical Characteristics are over recommended temperature and supply voltage.

AC Electrical Characteristics[†] - Serial Data Interfaces - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Notes
1	MCLK Frequency	f_{CLK}	19.15		20.5	MHz	
2	BCLK/ $\overline{C4i}$ Clock High	t_{BCH} , t_{C4H}	90			ns	
3	BCLK/ $\overline{C4i}$ Clock Low	t_{BLL} , t_{C4L}	90			ns	
4	BCLK/ $\overline{C4i}$ Period	t_{BCP}	240		7900	ns	
5	SSI Enable Strobe to Data Delay (first bit)	t_{SD}	80			ns	$C_L = 150$ pF
6	SSI Data Output Delay (excluding first bit)	t_{DD}	80			ns	$C_L = 150$ pF
7	SSI Output Active to High Impedance	t_{AHZ}	80			ns	$C_L = 150$ pF
8	SSI Enable Strobe Signal Setup	t_{SSS}	10		t_{BCP} -15	ns	
9	SSI Enable Strobe Signal Hold	t_{SSH}	15		t_{BCP} -10	ns	
10	SSI Data Input Setup	t_{DIS}	10			ns	
11	SSI Data Input Hold	t_{DIH}	15			ns	
12	ST-BUS/GCI $\overline{F0i}$ Setup	t_{F0iS}	20		150	ns	
13	ST-BUS/GCI $\overline{F0i}$ Hold	t_{F0iH}	20		150	ns	
14	ST-BUS/GCI Data Output delay	t_{DSD}	80			ns	$C_L = 150$ pF
15	ST-BUS/GCI Output Active to High Impedance	t_{ASHZ}	80			ns	$C_L = 150$ pF
16	ST-BUS/GCI Data Input Hold time	t_{DSH}	20			ns	
17	ST-BUS/GCI Data Input Setup time	t_{DSS}	20			ns	

[†] Timing is over recommended temperature and power supply voltages.