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ZL38002
Digital Echo Canceller for Hands Free Communication
Data Sheet

Features

January 2007

Ordering Information		
ZL38002QDG	48 Pin TQFP	Trays
ZL38002QDG1	48 Pin TQFP*	Trays
ZL38002DGE1	36 Pin QSOP*	Tubes, Bake & Drypack
ZL38002DGF1	36 Pin QSOP*	Tape & Reel, Bake & Drypack

*Pb Free Matte Tin

-40°C to 85°C

- 112 ms acoustic echo canceller
- Up to 12 dB of noise reduction
- Works with low cost voice codec. ITU-T G.711 or signed mag μ/A-Law, or linear 2's compliment
- Each port may operate independently in companded format or linear format
- Advanced NLP design - full duplex speech with no switched loss on audio paths
- Fast re-convergence time: tracks changing echo environment quickly
- Adaptation algorithm converges even during Double-Talk
- Designed for exceptional performance in high background noise environments
- Provides protection against narrow-band signal divergence
- Howling prevention stops uncontrolled oscillation in high loop gain conditions
- Programmable offset nulling of all PCM channels
- Serial micro-controller interface
- Idle channel noise suppression
- ST-BUS, GCI, or variable-rate SSI PCM interfaces
- User gain control provided for speaker path (-24 dB to +21 dB in 3 dB steps)
- Adjustable gain pads from -24 dB to +21 dB at Xin, Sin and Sout to compensate for different system requirements
- AGC on speaker path
- Handles up to -6 dB acoustic echo return loss (with the appropriate gain pad settings)
- Transparent data transfer and mute options
- 20 MHz master clock operation
- Low power mode during PCM Bypass
- Bootloadable for future factory software upgrades
- 2.7 V to 3.6 V supply voltage; 5 V-tolerant inputs

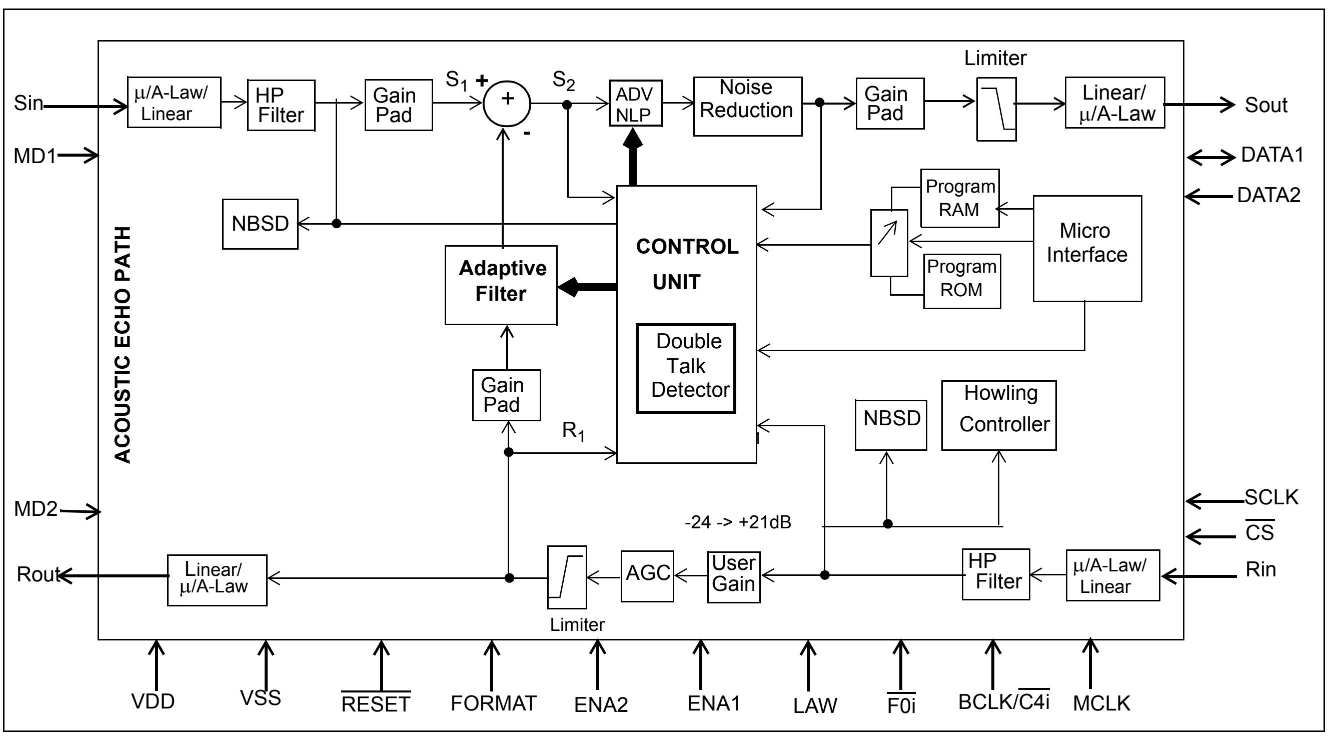

Figure 1 - Functional Block Diagram

Applications

- Hands free car kits
- Full duplex speaker-phone for digital telephone
- Echo cancellation for video conferencing
- Security systems
- Intercom systems (door entry, elevator, and restaurant drive-through)

	MT93L16	**ZL38001**	**ZL38002**	**ZL38003**
Description	AEC for analog hands-free communication	AEC for analog hands-free communication	AEC with noise reduction for digital hands-free communication	AEC with noise reduction & codecs for digital hands-free communication
Application	Analog Desktop phone Analog Intercom	Analog Desktop phone Analog Intercom	Hands-free Car Kits Digital Desktop Phone Home Security Intercom & Pedestals	Hands-free Car Kits Digital Desktop Phone Home Security Intercom & Pedestals
Features				
AEC	1 channel	1 channel	1 channel	1 channel
LEC	1 channel	1 channel	Custom Load	Custom Load
Gains	User Gain	User Gain/18 dB Gain on Sout	User Gain + System tuning gains	User Gain + System tuning gains
Noise Reduction	N	N	Y	Y
Integrated Codecs	N	N	N	dual channel

Table 1 - Acoustic Echo Cancellation Family

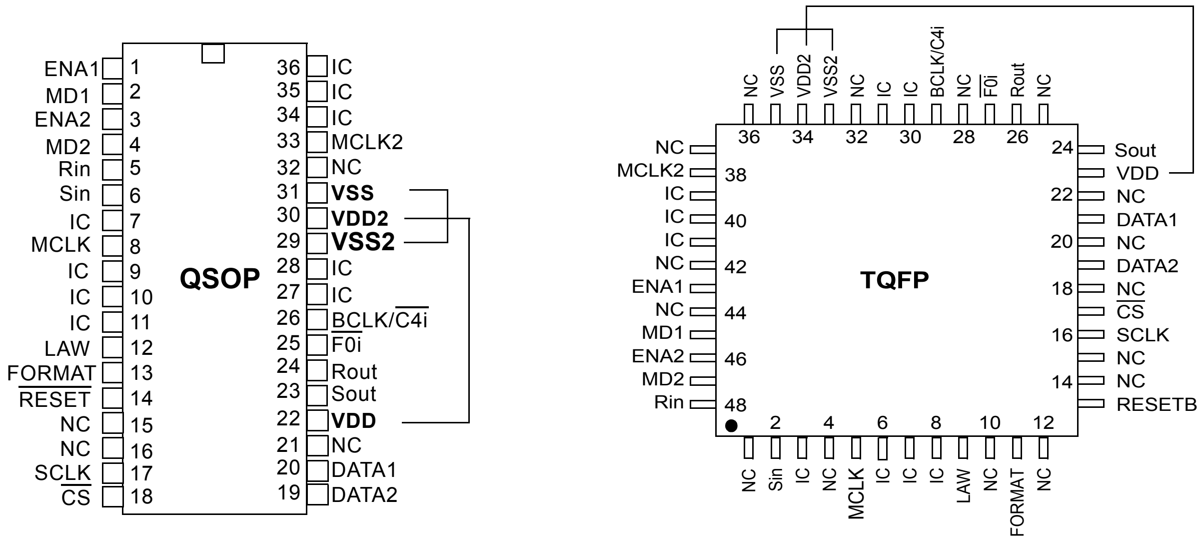

Figure 2 - Pin Connections

Pin Description

QSOP Pin #	TQFP Pin #	Name	Description
1	43	ENA1	**SSI Enable Strobe/ST-BUS & GCI Mode for Rin/Sout (Input).** This pin has dual functions depending on whether SSI or ST-BUS/GCI is selected. For SSI, this strobe must be present for frame synchronization. This is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer for on Rin/Sout pins. Strobe period is 125 ms. For ST-BUS or GCI, this pin, in conjunction with the MD1 pin, selects the proper mode for Rin/Sout pins (see ST-BUS and GCI Operation description).
2	45	MD1	**ST-BUS & GCI Mode for Rin/Sout (Input).** When in ST-BUS or GCI operation, this pin, in conjunction with the ENA1 pin, will select the proper mode for Rin/Sout pins (see ST-BUS and GCI Operation description). Connect this pin to Vss in SSI mode.
3	46	ENA2	**SSI Enable Strobe /ST-BUS & GCI Mode for Sin/Rout (Input).** This pin has dual functions depending on whether SSI or ST-BUS/GCI is selected. For SSI, this is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer on Sin/Rout pins. Strobe period is 125 ms. For ST-BUS/GCI, this pin, in conjunction with the MD2 pin, selects the proper mode for Sin/Rout pins (see ST-BUS and GCI Operation description).
4	47	MD2	**ST-BUS & GCI Mode for Sin/Rout (Input).** When in ST-BUS or GCI operation, this pin in conjunction with the ENA2 pin, selects the proper mode for Sin/Rout pins (see ST-BUS and GCI Operation description). Connect this pin to Vss in SSI mode.

Pin Description (continued)

QSOP Pin #	TQFP Pin #	Name	Description
5	48	Rin	**Receive PCM Signal Input (Input).** 128 kbps to 4096 kbps serial PCM input stream. Data may be in either companded or 2’s complement linear format. This is the Receive Input channel from the line (or network) side. Data bits are clocked in following SSI, GCI or ST-BUS timing requirements.
6	2	Sin	**Send PCM Signal Input (Input).** 128 kbps to 4096 kbps serial PCM input stream. Data may be in either companded or 2’s complement linear format. This is the Send Input channel (from the microphone). Data bits are clocked in following SSI, GCI or ST-BUS timing requirements.
7	3	IC	**Internal Connection (Input).** Must be tied to Vss.
8	5	MCLK	**Master Clock (Input).** Nominal 20 MHz Master Clock input (can be asynchronous relative to 8 KHz frame signal.) Tie together with MCLK2.
9,10,11	6, 7, 8	IC	**Internal Connection (Input).** Must be tied to Vss.
12	9	LAW	**A/$\overline{\mu}$ Law Select (Input).** When low, selects μ–Law companded PCM. When high, selects A-Law companded PCM. This control is for both serial pcm ports.
13	11	FORMAT	**ITU-T/$\overline{\text{Sign Mag}}$ (Input).** When low, selects sign-magnitude PCM code. When high, selects ITU-T (G.711) PCM code. This control is for both serial pcm ports.
14	13	$\overline{\text{RESET}}$	**Reset / Power-down (Input).** An active low resets the device and puts the ZL38002 into a low-power stand-by mode.
17	16	SCLK	**Serial Port Synchronous Clock (Input).** Data clock for the serial microport interface.
18	17	$\overline{\text{CS}}$	**Serial Port Chip Select (Input).** Enables serial microport interface data transfers. Active low.
19	19	DATA2	**Serial Data Receive (Input).** In Motorola/National serial microport operation, the DATA2 pin is used for receiving data. In Intel serial microport operation, the DATA2 pin is not used and must be tied to Vss or Vdd.
20	21	DATA1	**Serial Data Port (Bidirectional).** In Motorola/National serial microport operation, the DATA1 pin is used for transmitting data. In Intel serial microport operation, the DATA1 pin is used for transmitting and receiving data.
22	23	VDD	**Positive Power Supply (Input**). Nominally 3.3 volts.
23	24	Sout	**Send PCM Signal Output (Output).** 128 kbps to 4096 kbps serial PCM output stream. Data may be in either companded or 2’s complement linear PCM format. This is the Send Out signal after acoustic echo cancellation and non-linear processing. Data bits are clocked out following SSI, ST-BUS or GCI timing requirements.
24	26	Rout	**Receive PCM Signal Output (Output).** 128 kbps to 4096 kbps serial PCM output stream. Data may be in either companded or 2’s complement linear PCM format. This is the Receive out signal after the AGC and gain control. Data bits are clocked out following SSI, ST-BUS or GCI timing requirements.

Pin Description (continued)

QSOP Pin #	TQFP Pin #	Name	Description
25	27	$\overline{F0i}$	**Frame Pulse (Input).** In ST-BUS (or GCI) operation, this is an active-low (or active-high) frame alignment pulse, respectively. SSI operation is enabled by connecting this pin to Vss.
26	29	BCLK/$\overline{C4i}$	**Bit Clock/ST-BUS Clock (Input).** In SSI operation, BCLK pin is a 128 kHz to 4.096 MHz bit clock. This clock must be synchronous with ENA1 and ENA2 enable strobes. In ST-BUS or GCI operation, $\overline{C4i}$ pin must be connected to the 4.096 MHz ($\overline{C4}$) system clock.
27, 28	30, 31	IC	**Internal Connection (Input).** Tie to Vss.
29	33	VSS2	**Digital Ground (Input).** Nominally 0 volts.
30	34	VDD2	**Positive Power Supply (Input).** Nominally 3.3 volts (tie together with VDD).
31	35	VSS	**Digital Ground (Input).** Nominally 0 volts (tie together with VSS2).
33	38	MCLK2	**Master Clock (Input).** Nominal 20 MHz master clock (tie together with MCLK).
34,35,36	39, 40, 41	IC	**Internal Connection (Input).** Tie to Vss.
15, 16, 21, 32	1, 4, 10, 12, 14, 15, 18, 20, 22, 25, 28, 32, 36, 37, 42, 44	NC	**No Connect (Output).** This pin should be left unconnected.

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1.0 Changes Summary

The following table captures the changes from the November 2005 issue.

Page	Item	Change
1		Updated Ordering Information

2.0 Functional Description

The ZL38002 device is comprised of an acoustic echo canceller and the necessary control functions for operation. The ZL38002 guarantees clear signal transmission in both transmit and receive audio path directions to ensure reliable voice communication, even when low level signals are provided. The ZL38002 does not use variable attenuators during double-talk or single-talk periods of speech, as do many other acoustic echo cancellers for speakerphones. Instead, the ZL38002 provides high performance full-duplex operation similar to network echo cancellers. This results in users experiencing clear speech and uninterrupted background signals during the conversation and prevents subjective sound quality problems associated with “noise gating” or “noise contrasting”.

The ZL38002 uses an advanced adaptive filter algorithm that is double-talk stable, which means that convergence takes place even while both parties are talking. This algorithm allows continual tracking of changes in the echo path, regardless of double-talk, as long as a reference signal is available for the echo canceller.

The echo tail cancellation capability of the acoustic echo canceller has been sized appropriately (112 ms) to cancel echo in an average sized office with a reverberation time of less than 112 ms.

In addition to the echo cancellers, the following functions are supported:

- 12 dB of noise reduction
- User gain pads at the Sin and Sout ports plus one at the input of adaptive filter (XRAM)
- Control of adaptive filter convergence speed during periods of double-talk, far end single-talk and near-end echo path changes
- Control of Non-Linear Processor thresholds for suppression of residual non-linear echo
- Howling detector to identify when instability is starting to occur and to take action to prevent oscillation
- Narrow-Band Detector for preventing adaptive filter divergence caused by narrow-band signals
- Programmable high pass filters at Rin and Sin for removal of DC components in PCM channels
- Limiters that introduce controlled saturation levels
- Serial controller interface compatible with Motorola, National and Intel microcontrollers
- PCM encoder/decoder compatible with m/A-Law ITU-T G.711, m/A-Law Sign-Mag or linear 2’s complement coding
- Automatic gain control on the receive speaker path
- Idle channel noise suppression

2.1 Noise Reduction

The ZL38002 incorporates a noise reduction circuit that reduces background noise up to 12 dB. The level of noise reduction is programmed allowing the user to adjust the level of noise cancellation according to system requirements. This is controlled through the NR register on page 3 address 16_H. A larger value in this register will increase the amount of noise reduction. As the amount of noise reduction is increased the amount of distortion in the audio path also increases. The noise reduction can be bypassed by setting bit 4 in Control Register 1 (Address 01_H)

2.2 Noise Suppression

The ZL38002 also utilizes noise suppression which can be used to reduce idle channel noise from emanating from the acoustic end. By setting a threshold value in the lower nibble (bits 0-3) of the MCR2 register on page 0 address 01_H, idle channel noise below the threshold is zero-forced. The threshold limits ranges from 0 to 16 (based on a 16 bit 2's complement) with a value of 0 disabling suppression.

2.3 Adaptation Speed Control

The adaptation speed of the acoustic echo canceller is designed to optimize the convergence speed versus divergence caused by interfering near-end signals. Adaptation speed algorithm takes into account many different factors such as relative double-talk condition, far end signal power, echo path change and noise levels to achieve fast convergence.

2.4 Advanced Non-Linear Processor (ADV-NLP)

After echo cancellation, there is likely to be residual echo which needs to be removed so that it will not be audible. The ZL38002 uses an NLP to remove low level residual echo signals which are not comprised of background noise. The operation of the NLP depends upon a dynamic activation threshold, as well as a double-talk detector which disables the NLP during double-talk periods.

The ZL38002 keeps the perceived noise level constant, without the need for any variable attenuators or gain switching that causes audible “noise gating”. The noise level is constant and identical to the original background noise even when the NLP is activated.

The NLP can be disabled by setting the NLP- bit to 1 in the AEC control registers.

2.5 Narrow Band Signal Detector (NBSD)[1]

Single or multi-frequency tones (e.g,. DTMF, or signalling tones) present in the reference input of an echo canceller for a prolonged period of time may cause the adaptive filter to diverge. The Narrow Band Signal Detector (NBSD) is designed to prevent this divergence by detecting single or multi-tones of arbitrary frequency, phase, and amplitude. When narrow band signals are detected, the filter adaptation process is stopped but the echo canceller continues to cancel echo.

The NBSD can be disabled by setting the NB- bit to 1 in the MC control registers.

2.6 Howling Detector (HWLD)1

The Howling detector is part of an Anti-Howling control, designed to prevent oscillation as a result of positive feedback in the audio paths.

The HWLD can be disabled by setting the AH- bit to 1 in the (MC) control register.

2.7 Programmable High Pass Filter

Programmable high pass filters are place at the Sin and Rin ports. These filters have two functions, one to remove any DC offset that may be present on either the Rin or the Sin port and two, to filter low frequency noise such as road noise (below 300 Hz).

The offset null filters can be disabled by setting the HPF- bit to 1 in the AEC control registers.

1. Patented

2.8 Limiters

To prevent clipping in the echo paths, two limiters with variable thresholds are provided at the outputs.

2.9 User Gain

The user gain function provides the ability for users to adjust the audio gain on all paths. This gain is adjustable from -24 dB to +21 dB in 3 dB steps for the Sout and Rout paths. It is important to use ONLY this user gain function to adjust the speaker volume. The user gain function in the ZL38002 is optimally placed outside the echo path such that no reconvergence is necessary after gain changes, avoiding a burst of each overtime the speaker gain is changed.

2.10 AGC

The AGC function is provided to limit the volume in the speaker path. The gain of the speaker path is automatically reduced during the following conditions:

- When clipping of the receive signal occurs
- When initial convergence of the acoustic echo canceller detects unusually large echo return
- When howling is detected

The AGC can be disabled by setting the AGC- bit to 1 in MC control register

2.11 Programmable Gain Pad

The ZL38002 has three gain pads located at Sin, Sout and at the adaptive filter (Xin). These gain pads are intended to be set once during initialization and not be used as dynamic gain adjustments. The purpose of theses gainpads are to help fine tune the performance of the acoustic echo canceller for a particular system.

For example, the gain pad can be used to improve the subjective quality in low ERL environments. The ZL38002 can cancel echo with a ERL as low as 0 dB (attenuation from Rout to Sin). In many hand free applications, the ERL can be low (or negative). This is due to both speaker and microphone gain setting. The speaker gain has to be set high enough for the speaker to be heard properly and the microphone gain needs to be set high enough to ensure sufficient signal is sent to the far end. If the ERL (Acoustic Attenuation - speaker gain - microphone gain) is greater than 0 dB, then the echo canceller cannot cancel echo. To overcome this limitation, the gain pad at Sin and Sout can be used to lower the Sin level (and therefore the ERL) by 6 dB, perform the echo cancellation then amplify it at Sout by 6 dB. This will have the effect having 0dB gain between Sin and Sout for double talk signals while injecting a additional 6 dB attenuation for the echo return. It is important to reduce the DTDT threshold (Page 0 address 30) to match the Sin/Sout gain settings.

The gain can be accessed through Customer Gain Control Registers 1 - 2 (Page 0, Address $1C_H$ - $1D_H$).

2.12 Mute Function

A pcm mute function is provided for independent control of the Receive and Send audio paths. Setting the MUTE_R or MUTE_S bit in the MC register, causes quiet code to be transmitted on the Rout or Sout paths respectively. The ZL38002 has an optional DC offset control. The user can add a positive offset to the mute value. This is controlled through the DC offset register (Page 0, Address 03h)

Quiet code is defined according to the following table.

	LINEAR 16 bits 2's complement	SIGN/ MAGNITUDE μ-Law A-Law	CCITT (G.711)	
			μ-Law	A-Law
+Zero (quiet code)	0000h	80h	FFh	D5h

Table 2 - Quiet PCM Code Assignment

2.13 Master Bypass

A PCM bypass function is provided to allow transparent transmission of pcm data through the ZL38002. When the bypass function is active, PCM data passes transparently from Rin to Rout and from Sin to Sout, with bit-wise integrity preserved.

When the Bypass function is selected, most internal functions are powered down to provide low power consumption.

The BYPASS control bit is located in the main control MC register.

2.14 AEC Bypass

An AEC bypass function is provided to allow the user to bypass only the AEC (i.e the echo estimate from the adaptive filter is not subtracted from the Send path). This bypass does not effect any other function in the ZL38002.

The AEC BYPASS control bit is located in the Acoustic Echo Canceller Control Register (AECCR).

2.15 Adaptation Control

Adaptation control bit is located in the Acoustic Echo Canceller Control Register (Page 0, Address 21h). When the ADAPT- bit is set to 1, the adaptive filter is frozen at the current state. In this state, the device continues to cancel echo with the current echo model.

When the ADAPT- bit is set to 0, the adaptive filter is continually updated allowing the echo cancellor to adapt and track changes in the echo path. This is the normal operating state ZL38002

2.16 Throughput Delay

In all modes, except ST-BUS/GCI operation, voice channels have 2 frames of constant delay. In ST-BUS/$\overline{\text{GCI}}$ operation, the D and C channels have a delay of one frame.

2.17 Power Down / Reset

Holding the $\overline{\text{RESET}}$ pin at logic low will keep the ZL38002 device in a power-down state. In this state all internal clocks are halted, and the DATA1, Sout and Rout pins are tristated.

The user should hold the $\overline{\text{RESET}}$ pin low for at least 200 msec following power-up. This will insure that the device powers up in a proper state. Following any return of $\overline{\text{RESET}}$ to logic high, the user must wait for 8 complete 8 KHz frames prior to writing to the device registers. During this time, the initialization routines will execute and set the ZL38002 to default operation based on the installed algorithm.

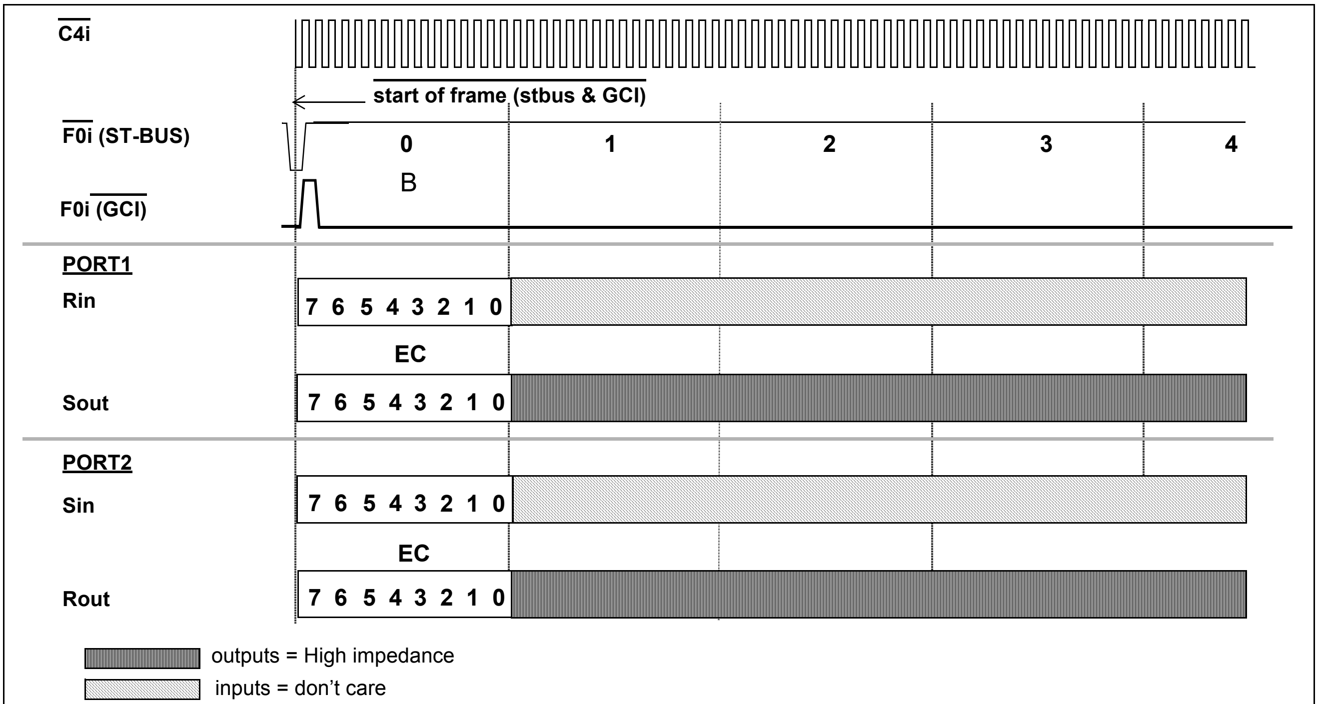
3.0 PCM Data I/O

The PCM data transfer for the ZL38002 is provided through two PCM ports. One port consists of Rin and Sout pins while the second port consists of Sin and Rout pins. The data are transferred through these ports according to either ST-BUS, GCI or SSI conventions detected automatically by the device. The ZL38002 determines the convention by monitoring the signal applied to the F0i pin. When a valid ST-BUS (active low) frame pulse is applied to the F0i pin, the ZL38002 will assume ST-BUS operation. When a valid GCI (active high) frame pulse is applied to the F0i pin, the device will assume GCI operation. If F0i is tied continuously to Vss, the device is set to SSI operation. Figures 3 to 6 show timing diagrams of these 3 PCM-interface operation conventions.

3.1 ST-BUS and GCI Operation

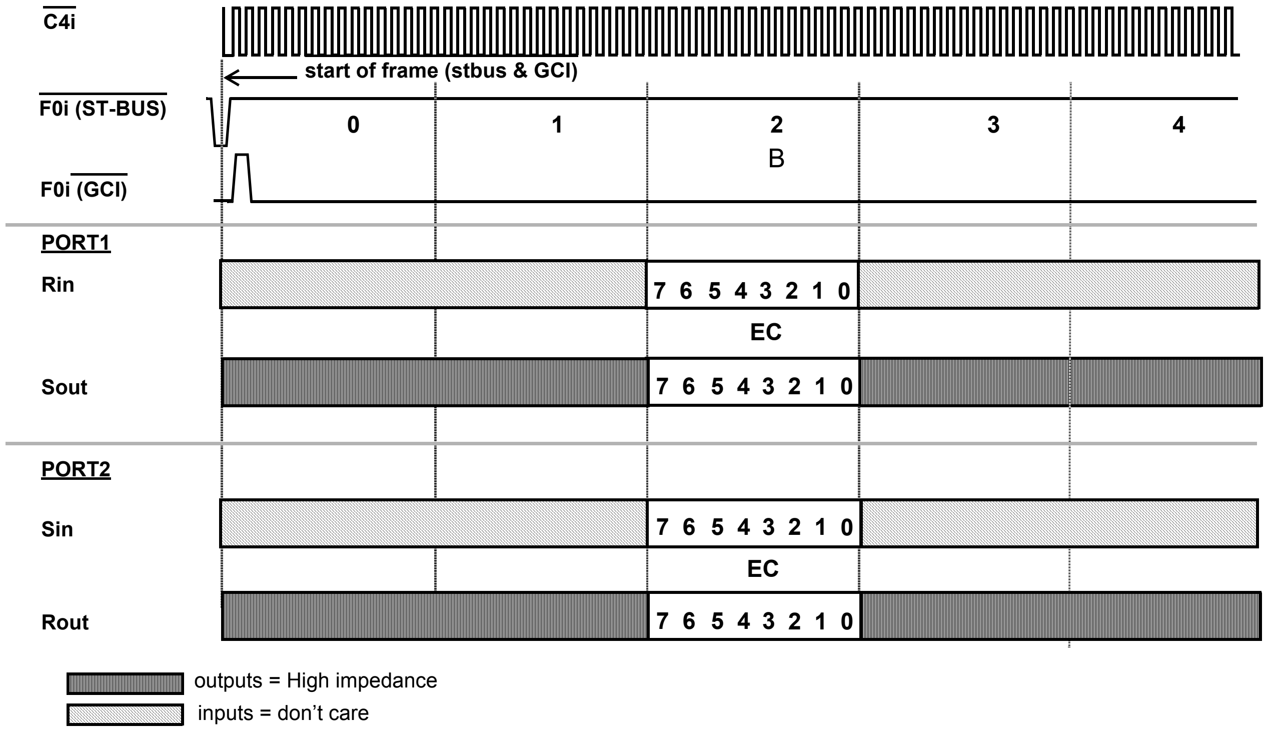
The ST-BUS PCM interface conforms to Zarlink's ST-BUS standard with an active-low frame pulse. Input data is clocked in by the rising edge of the bit clock (C4i) three-quarters of the way into the bit cell and output data bit boundaries (Rout, Sout) occur every second falling edge of the bit clock (see Figure 11.) The GCI PCM interface corresponds to the GCI standard commonly used in Europe with an active-high frame pulse. Input data is clocked in by the falling edge of the bit clock (C4i) three-quarters of the way into the bit cell and output data bit boundaries (Rout, Sout) occur every second rising edge of the bit clock (see Figure 12.)

Either of these interfaces (ST-BUS or GCI) can be used to transport 8 bit companded PCM data (using one timeslot) or 16 bit 2's complement linear PCM data (using two timeslots). The MD1/ENA1 pins select the timeslot on the Rin/Sout port while the MD2/ENA2 pin selects the timeslot on the Sin/Rout port, as in Table 2. Figures 3 to 6 illustrate the timeslot allocation for each of these four modes.



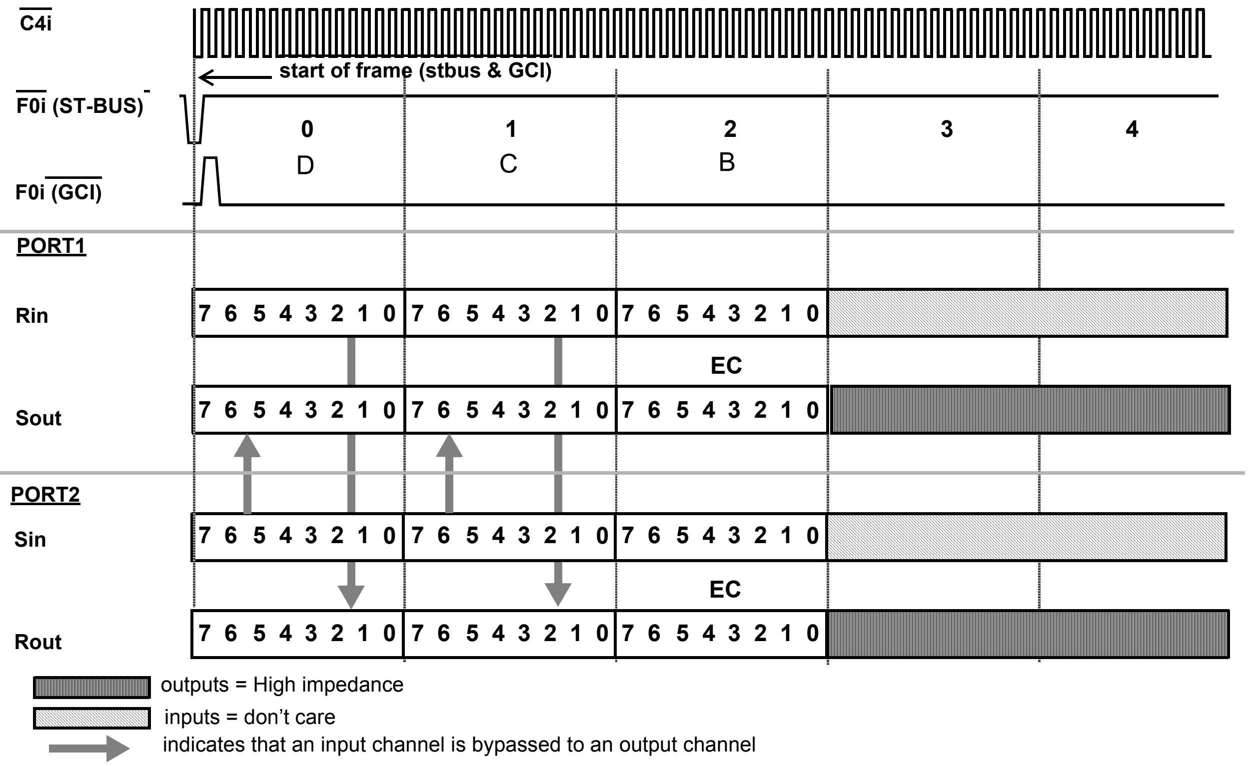
In ST-BUS/GCI Mode 1, echo canceller I/O channels are assigned to ST-BUS/GCI timeslot 0. Note that the user can configure PORT1 and PORT2 into different modes.

Figure 3 - ST-BUS and GCI 8-Bit Companded PCM I/O on Timeslot 0 (Mode 1)



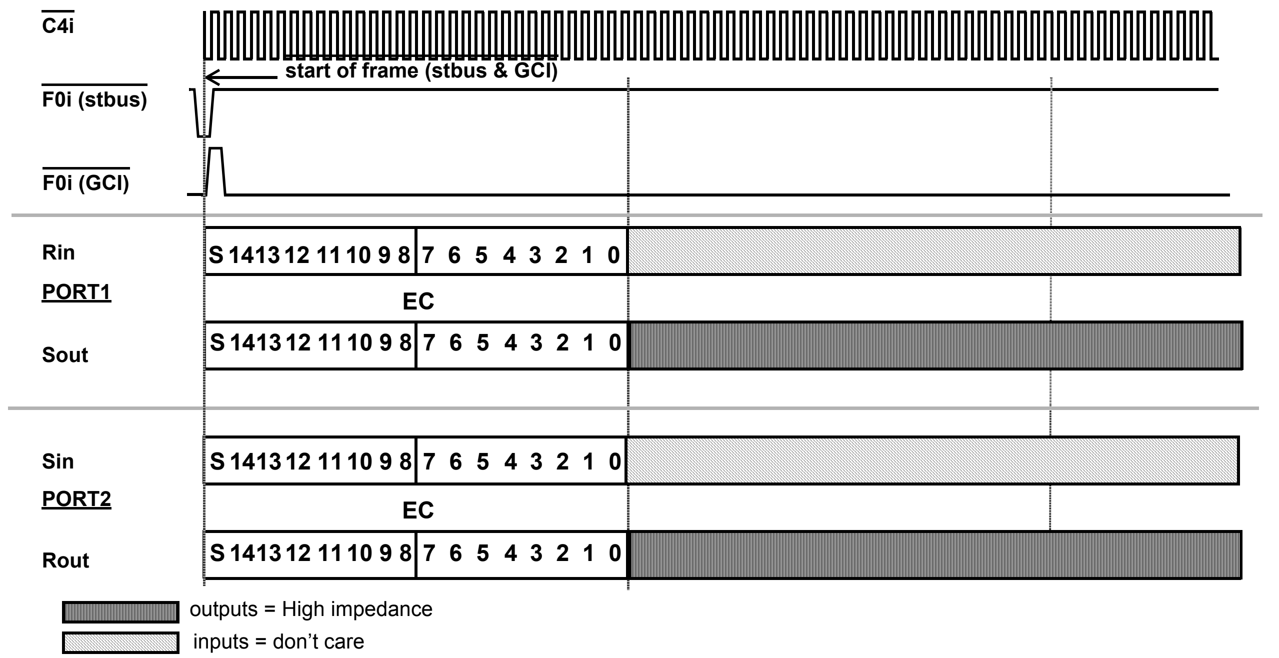
In ST-BUS/GCI Mode 2, echo canceller I/O channels are assigned to ST-BUS/GCI timeslot 2. Note that the user can configure PORT1 and PORT2 into different modes.

Figure 4 - ST-BUS and GCI 8-Bit Companded PCM I/O on Timeslot 2 (Mode 2)



ST-BUS/GCI Mode 3 supports connection to 2 B+D devices where timeslots 0 and 1 transport D and C channels and echo canceller (EC) I/O channels are assigned to ST-BUS timeslot 2 (B). Both PORT1 and PORT2 must be configured in Mode 3.

Figure 5 - ST-BUS and GCI 8-Bit Companded PCM I/O with D and C channels (Mode 3)



ST-BUS/GCI Mode 4 allows 16 bit 2's complement linear data to be transferred using ST-BUS/GCI I/O timing. Note that PORT1 and PORT2 need not necessarily both be in mode 4.

Figure 6 - ST-BUS and GCI 16-Bit 2's Complement Linear PCM I/O (Mode 4)

PORT1 Rin/Sout		**ST-BUS/GCI Mode Selection**	**PORT2 Sin/Rout**	
Enable Pins			Enable Pins	
MD1	ENA1		MD2	ENA2
0	0	Mode 1. 8 bit companded PCM I/O on timeslot 0	0	0
0	1	Mode 2. 8 bit companded PCM I/O on timeslot 2.	0	1
1	0	Mode 3. 8 bit companded PCM I/O on timeslot 2. Includes D & C channel bypass in timeslots 0 & 1.	1	0
1	1	Mode 4. 16-bit 2's complement linear PCM I/O on timeslots 0 & 1.	1	1

Table 3 - ST-BUS & GCI Mode Select

3.2 SSI Operation

The SSI PCM interface consists of data input pins (Rin, Sin), data output pins (Sout, Rout), a variable rate bit clock (BCLK), and two enable pins (ENA1, ENA2) to provide strobes for data transfers. The active high enable may be either 8 or 16 BCLK cycles in duration. Automatic detection of the data type (8 bit companded or 16-bit 2's complement linear) is accomplished internally. The data type cannot change dynamically from one frame to the next.

In SSI operation, the frame boundary is determined by the rising edge of the ENA1 enable strobe (see Figure 7). The other enable strobe (ENA2) is used for parsing input/output data and it must pulse within 125 microseconds of the rising edge of ENA1.

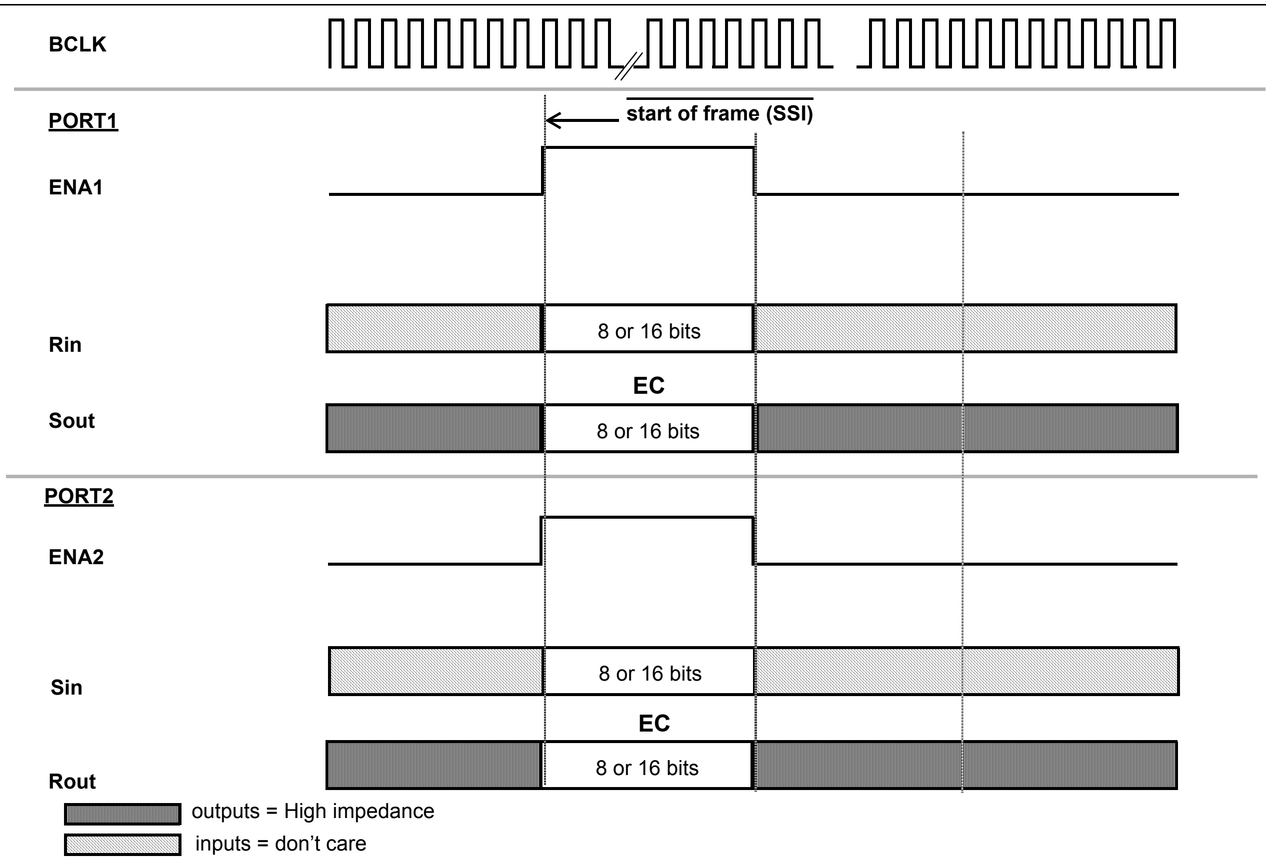
In SSI operation, the enable strobes may be a mixed combination of 8 or 16 BCLK cycles allowing the flexibility to mix 2's complement linear data on one port (e.g., Rin/Sout) with companded data on the other port (e.g., Sin/Rout).

Enable Strobe Pin	Designated PCM I/O Port
ENA1	Line Side Echo Path (PORT 1)
ENA2	Acoustic Side Echo Path (PORT 2)

Table 4 - SSI Enable Strobe Pins

3.3 PCM Law and Format Control (LAW, FORMAT)

The PCM companding/coding law used by the ZL38002 is controlled through the LAW and FORMAT pins. ITU-T G.711 companding curves for m-Law and A-Law are selected by the LAW pin. PCM coding ITU-T G.711 and Sign-Magnitude are selected by the FORMAT pin. See Table 4.



Note that the two ports are independent so that, for example, PORT1 can operate with 8-bit enable strobes and PORT2 can operate with 16-bit enable strobes.

Figure 7 - SSI Operations

PCM Code	Sign-Magnitude FORMAT=0	ITU-T (G.711) FORMAT=1	
	μ/A-LAW LAW = 0 or 1	μ-LAW LAW = 0	A-LAW LAW =1
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
- Zero	0000 0000	0111 1111	0101 0101
- Full Scale	0111 1111	0000 0000	0010 1010

Table 5 - Companded PCM

3.4 Linear PCM

The 16-bit 2's complement PCM linear coding permits a dynamic range beyond that which is specified in ITU-T G.711 for companded PCM. The echo-cancellation algorithm will accept 16-bits 2's complement linear code which gives a maximum signal level of +15 dBm0.

3.5 Bit Clock (BCLK/$\overline{\text{C4i}}$)

The BCLK/$\overline{\text{C4i}}$ pin is used to clock the PCM data for GCI and ST-BUS ($\overline{\text{C4i}}$) interfaces, as well as for the SSI (BCLK) interface.

In SSI operation, the bit rate is determined by the BCLK frequency. This input must contain either eight or sixteen clock cycles within the valid enable strobe window. BCLK may be any rate between 128 KHz to 4.096 MHz and can be discontinuous outside of the enable strobe windows defined by ENA1, ENA2 pins. Incoming PCM data (Rin, Sin) are sampled on the falling edge of BCLK while outgoing PCM data (Sout, Rout) are clocked out on the rising edge of BCLK. See Figure 13.

In ST-BUS and GCI operation, connect the system $\overline{\text{C4}}$ (4.096 MHz) clock to the $\overline{\text{C4i}}$ pin.

3.6 Master Clock (MCLK)

A nominal 20 MHz, continuously-running master clock (MCLK) is required. MCLK may be asynchronous with the 8 KHz frame.

4.0 Microport

The serial microport provides access to all ZL38002 internal read and write registers, plus write-only access to the bootloadable program RAM (see next section for bootload description). This microport is compatible with Intel MCS-51 (mode 0), Motorola SPI (CPOL=0, CPHA=0) and National Semiconductor Microwire specifications. The microport consists of a transmit/receive data pin (DATA1), a receive data pin (DATA2), a chip select pin ($\overline{\text{CS}}$) and a synchronous data clock pin (SCLK).

The ZL38002 automatically adjusts its internal timing and pin configuration to conform to Intel or Motorola/National specifications. The microport dynamically senses the state of the SCLK pin each time the $\overline{\text{CS}}$ pin becomes active (i.e., high to low transition). If the SCLK pin is high during a $\overline{\text{CS}}$ activation, then the Intel mode 0 timing is assumed. In this case the DATA1 pin is defined as a bi-directional (transmit/receive) serial port and DATA2 is internally disconnected. If SCLK is low during a $\overline{\text{CS}}$ activation, then Motorola/National timing is assumed and DATA1 is defined as the data transmit pin while DATA2 becomes the data receive pin. The ZL38002 supports Motorola halfduplex processor mode (CPOL=0 and CPHA=0). This means that during a write to the ZL38002, via a Motorola processor, output data from the DATA1 pin is disregarded. This also means that input data on the DATA2 pin is ignored by the ZL38002 during a valid read by the Motorola processor.

All data transfers through the microport are two bytes long. This requires the transmission of a Command/Address byte followed by the data byte to be written to or read from the addressed register. $\overline{CS}$ must remain low for the duration of this two-byte transfer. As shown in Figures 8 and 9, the falling edge of $\overline{CS}$ indicates to the ZL38002 that a microport transfer is about to begin. The first 8 clock cycles of SCLK after the falling edge of $\overline{CS}$ are always used to receive the Command/Address byte from the microcontroller. The Command/Address byte contains information detailing whether the second byte transfer will be a read or a write operation and at what address. The next 8 clock cycles are used to transfer the data byte between the ZL38002 and the microcontroller. At the end of the two-byte transfer, $\overline{CS}$ is brought high again to terminate the session. The rising edge of $\overline{CS}$ will tri-state the DATA1 pin. The DATA1 pin will remain tri-stated as long as $\overline{CS}$ is high.

Intel processors utilize Least Significant Bit (LSB) first transmission while Motorola/National processors use Most Significant Bit (MSB) first transmission. The ZL38002 microport automatically accommodates both schemes for normal data bytes. However, to ensure timely decoding of the R/$\overline{W}$ and address information, the Command/Address byte is defined differently for Intel and Motorola/National operations. Refer to the relative timing diagrams of Figure 6 and Figure 7. Receive data bits are sampled on the rising edge of SCLK while transmit data is clocked out on the falling edge of SCLK. Detailed microport timing is shown in Figure 13 and Figure 14.

5.0 Bootload Process and Execution from RAM

A bootloadable program RAM (BRAM) is available on the ZL38002 to support factory-issued software upgrades to the built-in algorithm. To make use of this bootload feature, users must include 4096 X 8 bits of memory in their microcontroller system (i.e., external to the ZL38002), from which the ZL38002 can be bootloaded. Registers and program data are loaded into the ZL38002 in the same fashion via the serial microport. Both employ the same command / address / data byte specification described in the previous section on serial microport. Either intel or motorola mode may be transparently used for bootloading. There are also two registers relevant to bootloading (BRC=control and SIG=signature, see Register Summary). The effect of these register values on device operation is summarized in Table 5.

Bootload mode is entered and exited by writing to the bootload bit in the Bootload RAM Control (BRC) register at address 3fh (see Register Summary). During bootload mode, any serial microport “write” (R/$\overline{W}$ command bit =0) to an address other than that of the BRC register will contribute to filling the program BRAM. Call these transactions "BRAM-fill" writes. Although a command/address byte must still precede each data byte (as described for the serial microport), the values of the address fields for these “BRAM-fill” writes are ignored (except for the value 3fh, which designates the BRC register.) Instead, addresses are internally generated by the ZL38002 for each “BRAM-fill” write. Address generation for “BRAM-fill” writes resumes where it left off following any read transaction while bootload mode is enabled. The first 4096 "BRAM-fill" writes while bootload is enabled will load the memory, filling the BRAM and ignoring further writes. Before bootload *mode is disabled*, it is recommended that users then read back the value from the signature register (SIG) and compare with the one supplied by the factory along with the code. Equality verifies that the correct data has been loaded. The signature calculation uses an 8-bit MISR which only incorporates input from “BRAM-fill” writes. Resetting the bootload bit ($\mathbf{C_2}$) in the BRC register to 0 (see Register Summary) exits bootload mode, resetting the signature (SIG) register and internal address generator for the next bootload. A hardware reset ($\overline{RESET}$=0) similarly returns the ZL38002 to the ready state for the start of a bootload.

<table>
<tr><th colspan="4">FUNCTIONAL DESCRIPTION FOR USING THE BOOTABLE RAM</th></tr>
<tr><td></td><th colspan="3">BOOTLOAD MODE - Microport Access is to bootload RAM (BRAM)</th></tr>
<tr><td rowspan="5">BRC Register Bits
$C_3C_2C_1C_0$
X 1 0 0</td><td>$R/\overline{W}$</td><td>Address</td><td>Data</td></tr>
<tr><td>$\overline{W}$</td><td>3fh
(= 1 1 1 1 1 1 b)</td><td>Writes "data" to BRC reg.
- Bootload frozen; BRAM contents are NOT affected.</td></tr>
<tr><td>$\overline{W}$</td><td>other than 3fh</td><td>Writes "data" to next byte in BRAM (bootloading.)</td></tr>
<tr><td>R</td><td>1 x x x x x b</td><td>Reads back "data" = BRC reg value.
- Bootload frozen; BRAM contents are NOT affected.</td></tr>
<tr><td>R</td><td>0 x x x x x b</td><td>Reads back "data" = SIG reg value.
- Bootload frozen; BRAM contents are NOT affected.</td></tr>
<tr><td></td><th colspan="3">NON-BOOTLOAD MODE - Microport Access is to device registers (DREGs)</th></tr>
<tr><td rowspan="3">BRC Register Bits
$C_3C_2C_1C_0$
X 0 0 0</td><td>$R/\overline{W}$</td><td>Address</td><td>Data</td></tr>
<tr><td>$\overline{W}$</td><td>any
(= $a_5\ a_4\ a_3\ a_2\ a_1\ a_0$ b)</td><td>Writes "data" to corresponding DREG.</td></tr>
<tr><td>R</td><td>any
(= $a_5\ a_4\ a_3\ a_2\ a_1\ a_0$ b)</td><td>Reads back "data" = corresponding DREG value.</td></tr>
<tr><th colspan="4">PROGRAM EXECUTION MODES</th></tr>
<tr><td>$C_3C_2C_1C_0$
0 0 0 0</td><td colspan="3">Execute program in ROM, bootload mode disabled.
- BRAM address counter reset to initial (ready) state.
- SIG register reseeded to initial (ready) state</td></tr>
<tr><td>$C_3C_2C_1C_0$
0 1 0 0</td><td colspan="3">Execute program in ROM, while bootloading the RAM.
- BRAM address counter increments on microport writes (except to 3fh)
- SIG register recalculates signature on microport writes (except to 3fh)</td></tr>
<tr><td>$C_3C_2C_1C_0$
1 0 0 0</td><td colspan="3">Execute program in RAM, bootload mode disabled.
- BRAM address counter reset to initial (ready) state.
- SIG register reseeded to initial (ready) state</td></tr>
<tr><td>$C_3C_2C_1C_0$
1 1 0 0</td><td colspan="3">- INVALID -</td></tr>
</table>

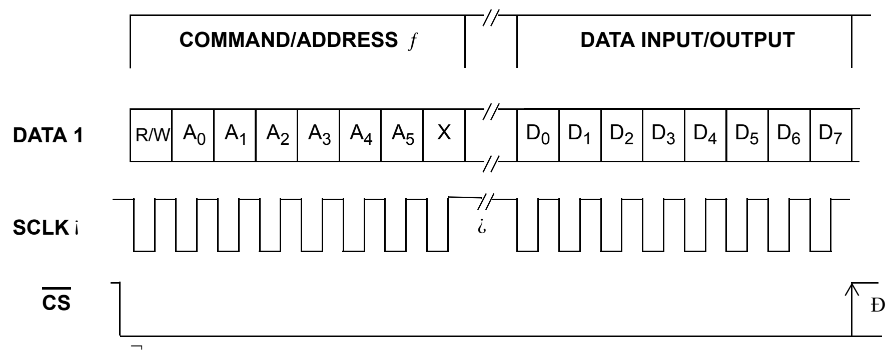
Table 6 - Bootload RAM Control (BRC) Register States

Note: bits $C_1\ C_0$ are reserved, and must be set to zero.

To begin execution from the RAM once the program has been loaded, the bootload mode must be disabled (BOOT bit, $\mathbf{C_2}$=0) and execution from RAM enabled (RAM_ROMb bit, $\mathbf{C_3}$=1) by setting the appropriate bits in the BRC register. During the bootload process, however, ROM program execution (RAM_ROMb bit, $\mathbf{C_3}$=0) should be selected. See Table 5 for the effect of the BRC register settings on Microport accesses and on program execution.

Following program loading and enabling of execution from RAM, it is recommended that the user set the software reset bit in the Main Control (MC) register, to ensure that the device updates the default register values to those of the new program in RAM. Note: it is important to use a software reset rather than a hardware (RESET=0) reset, as the latter will return the device to its default settings (which includes execution from program ROM instead of RAM.)

To verify which code revision is currently running, users can access the Firmware Revision Code (FRC) register (see Register Summary). This register reflects the identity code (revision number) of the last program to run register initialization (which follows a software or hardware reset.)



¿ This delay is due to internal processor timing and is equal to Tsch time. The delay is transparent to ZL38002.

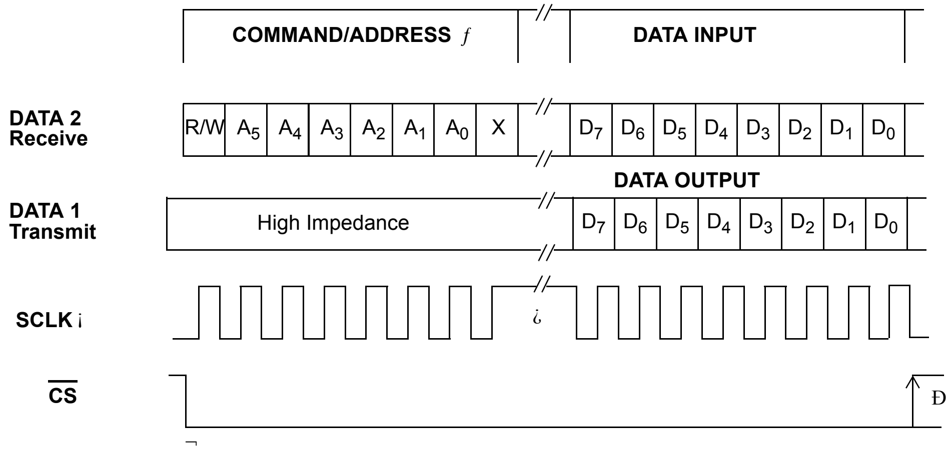
¡ The ZL38002: latches receive data on the rising edge of SCLK
outputs transmit data on the falling edge of SCLK

¬ The falling edge of $\overline{CS}$ indicates that a COMMAND/ADDRESS byte will be transmitted from the microprocessor. The subsequent byte is always data followed by $\overline{CS}$ returning high.

Ð A new COMMAND/ADDRESS byte may be loaded only by $\overline{CS}$ cycling high then low again.

ƒ The COMMAND/ADDRESS byte contains: 1 bit - Read/$\overline{\text{Write}}$
6 bits - Addressing Data
1 bit - Unused

Figure 8 - Serial Microport Timing for Intel Mode 0



¿ This delay is due to internal processor timing and is equal to Tsch time. The delay is transparent to ZL38002.

¡ The ZL38002: latches receive data on the rising edge of SCLK
outputs transmit data on the falling edge of SCLK

¬ The falling edge of $\overline{CS}$ indicates that a COMMAND/ADDRESS byte will be transmitted from the microprocessor. The subsequent byte is always data followed by $\overline{CS}$ returning high.

Ð A new COMMAND/ADDRESS byte may be loaded only by $\overline{CS}$ cycling high then low again.

ƒ The COMMAND/ADDRESS byte contains: 1 bit - Read/$\overline{\text{Write}}$
6 bits - Addressing Data
1 bit - Unused

Figure 9 - Serial Microport Timing for Motorola Mode 00 or National Microwire

6.0 Register Summary

Any register not described in the following section should be labels reserved for internal use.

Address	CPU Access	Page	Reset Value	Description
00_H	R/$\overline{W}$	0	00_H	Main Control Register 1 (MCR1)
01_H	R/$\overline{W}$	0	00_H	Main Control Register 2 (MCR2)
02_H	Read	0		Status Register (SR)
03_H	R/$\overline{W}$	0	00_H	DC Offset Register
04_H	R/$\overline{W}$	0	$A1_H$	High Pass Filter Constant Register (FLTSH)
05_H	R/$\overline{W}$	0	08_H	Mu Constant
07_H	Read	0	$A6_H$	Bootload RAM Signature Register (SIG)
08_H	R/$\overline{W}$	0	80_H	Slow Adaptation Threshold Register 1 (SATR1)
09_H	R/$\overline{W}$	0	04_H	Slow Adaptation Threshold Register 2 (SATR2)
12_H	R/W	0	00_H	Automatic Sout Gain Reduction (SoutGR)
$1C_H$	R/$\overline{W}$	0	88_H	Customer Gain Control Register 1 (CGCR1)
$1D_H$	R/$\overline{W}$	0	08_H	Customer Gain Control Register 2 (CGCR2)
20_H	R/$\overline{W}$	0	$6D_H$	Receive Gain Control Register (RGCR)
21_H	R/$\overline{W}$	0	00_H	Acoustic Echo Canceller Control Register (AECCR)
22_H	Read	0	00_H	Acoustic Echo Canceller Status Register 1 (ARCSR1)
23_H	Read	0	00_H	Acoustic Echo Canceller Status Register 2 (AECSR2)
24_H	R/$\overline{W}$	0	80_H	Acoustic LMS Filter Length Register 1 (ALMSFR1)
25_H	R/$\overline{W}$	0	$3E_H$	Acoustic LMS Filter Length Register 2 (ALMSFR2)
26_H	R/$\overline{W}$	0	$3D_H$	Decay Step Size Control Register (DSSCR)
27_H	R/$\overline{W}$	0	06_H	Decay Step Number Register (DSNR)
28_H	R/$\overline{W}$	0	96_H	Near-End Speech Detection Threshold 1 (NESDT1)
29_H	R/$\overline{W}$	0	04_H	Near-End Speech Detection Threshold 2 (NESDT2)
30_H	R/$\overline{W}$	0	80_H	Double-Talk Hand-Over Time 1 (DTHOT1)
31_H	R/$\overline{W}$	0	21_H	Double-Talk Hand-Over Time 2 (DTHOT2)
32_H	R/$\overline{W}$	0	$2A_H$	Automatic Rout Gain Reduction Register (RoutGR)
34_H	R/$\overline{W}$	0	AA_H	NLP Threshold Register
35_H	R/$\overline{W}$	0	01_H	
36_H	Read	0	00_H	Send (Sin) Peak Detect Register 1 (SPDR1)
37_H	Read	0	00_H	Send (Sin) Peak Detect Register 2 (SPDR2)
38_H	Read	0	00_H	Send Error Peak Detect Register 1 (SEPDR1)
39_H	Read	0	00_H	Send Error Peak Detect Register 2 (SEPDR2)

Table 7 - Address Map

Address	CPU Access	Page	Reset Value	Description
$3A_H$	Read	0	00_H	Receive (Rout) Peak Detect Register 1 (RPDR1) Receive (Rout) Peak Detect Register 2 (RPDR2)
$3B_H$	Read	0	00_H	
$3C_H$	Read	0	00_H	Adaptation Speed Register 1 (ASR1) Adaptation Speed Register 2 (ASR2)
$3D_H$	Read	0	10_H	
$3F_H$	$R/\overline{W}$	0/1/2/3	08_H	BRC Bootload RAM Control Register (BRCR)
$1A_H$	Read	1	00_H	Noise Level R Path Register 1 (NLRPR1) Noise Level R Path Register 2 (NLRPR2)
$1B_H$	Read	1	00_H	
$3A_H$	Read	1	00_H	Noise Level S Path Register 1 (NLSPR1) Noise Level S Path Register 2 (NLSPR2)
$3B_H$	Read	1	00_H	
$1C_H$	$R/\overline{W}$	2	00_H	AGC Gain Register 1 (AGCGR1) AGC Gain Register 2 (AGCGR2)
$1D_H$	$R/\overline{W}$	2	08_H	
15_H	$R/\overline{W}$	3	20_H	Noise Threshold for Noise Reduction Register (NRTH)
17_H	$R/\overline{W}$	3	20_H	Minimum Noise Reduction Level Register(Beta)

Table 7 - Address Map (continued)

7.0 Register Definitions

Read/$\overline{\text{Write}}$ Page 0, Address: 00_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
LIMIT	MUTE_R	MUTE_S	BYPASS	NB-	AGC-	AH-	RESET

Bit	Name	Description
7	LIMIT	When high, Rin and Sin signals are limited to 0.25 in amplitude. When low, no limit is imposed on the inputs.
6	MUTE_R	When high, the Rin path is muted to quiet code (after the NLP) and when low the Rin path is not muted.
5	MUTE_S	When high, the Sin path is muted to quiet code (after the NLP) and when low the Sin path is not muted.
4	BYPASS	When high, the Send and Receive paths are transparently by-passed from input to output and when low the Send and Receive paths are not bypassed.
3	NB-	When high, Narrowband signal detectors in Rin and Sin paths are disabled and when low the signal detectors are enabled.
2	AGC-	When high, AGC is disabled and when low AGC is enabled.
1	AH-	When high, the Howling detector is disabled and when low the Howling detector is enabled.
0	RESET	When high, the power initialization routine is executed presetting all registers to default values. This bit automatically clears itself to'0' when reset is complete.

Register Table 1 - Main Control Register 1 (MC1)

Read/$\overline{\text{Write}}$ Address: 01_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
SHFT	Reserved	Reserved	NRdis	NSUP3	NSUP2	NSUP1	NSUP0

Bit	Name	Description
7	SHFT	When high and in 16-bit linear mode, this bit enables shift right by 2 on inputs Sin, Rin, and shift left by 2 on outputs Sout, Rout, for codec. If not in 16-bit linear mode for **both I/O port**s, this bit is ignored. When low, =default, no shift.
6	Reserved	Reserved: Must be set to low
5	Reserved	Reserved: Must be set to low

Register Table 2 - Main Control Register 2 (MC2)