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Timberwolf Digital Signal Processor family, powered by *AcuEdge*™ Technology

Designed for IP Cameras with Sound Classification

ZL38052

Preliminary Data Sheet

Document ID# 154531 Version 1 March 2016

Description

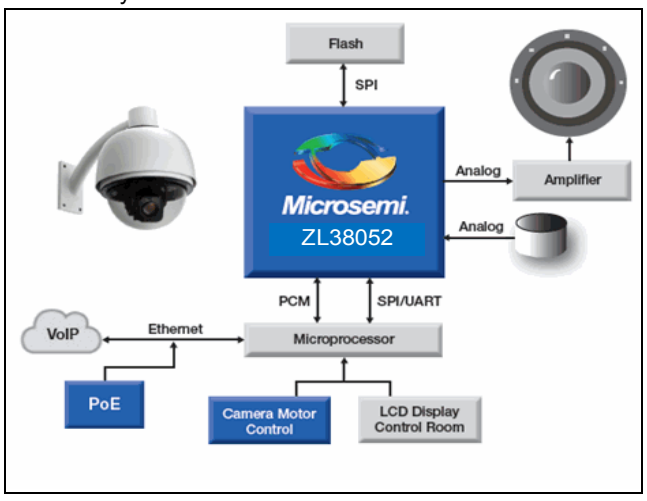
The ZL38052 is part of Microsemi's Timberwolf audio processor family of products. These devices feature Microsemi's innovative *AcuEdge* acoustic technology, which is a set of highly-complex and integrated algorithms. The Microsemi *AcuEdge* Technology ZL38052 is designed to provide leading edge far field microphone processing with advanced features targeted for IP and security cameras with high definition (HD) 2-way hands-free voice.

The Microsemi *AcuEdge* Technology license-free, royalty-free intelligent audio Firmware provides Beamforming, Sound Location Estimation, Acoustic Echo Cancellation (AEC), Noise Reduction and a variety of other voice enhancements to improve both the intelligibility and subjective quality of voice in harsh environments. The ZL38052 also incorporates a sound classification feature allowing the system to recognize smoke detector alarms (T3), carbon monoxide detector alarms (T4) and glass break detection.

Microsemi offers additional tools to speed up the product development cycle. The *MiTuner*™ ZLS38508 or ZLS38508LITE GUI software packages allow a user to interactively configure the ZL38052 device. The optional *MiTuner* ZLE38470BADA Automatic Tuning Kit provides automatic tuning and easy control for manual fine tuning adjustments.

Applications

- IP Cameras
- Security Cameras



Typical IP Security Camera Application

Ordering Information

Device OPN	Package	Packing
ZL38052LDF1	64-pin QFN (9x9)	Tape & Reel
ZL38052LDG1	64-pin QFN (9x9)	Tray
ZL38052UGB2	56-ball WLCSP (3.1x3.1)	Tape & Reel

These packages meet RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

Microsemi *AcuEdge* Technology ZLS38052 Firmware

There are two Firmware images that may be selected to provide the desired operating mode. Firmware images can be swapped during normal operation to switch modes dynamically. Firmware image size varies with firmware load.

ZLS38052.0 (Full Duplex Communication)

- Far Field Microphone Processing
- Microphone Beamforming
- Sound Location Estimation
- Full Narrowband and Wideband Acoustic Echo cancellation operation
  - Supports long tail AEC (up to 256 ms)
  - Non-Linear AEC provides higher tolerance for speaker distortions
- Howling detection/cancellation
  - Prevents oscillation in AEC audio path
- Advanced noise reduction reduces background noise from the near-end speech signal using Psychoacoustic techniques
- Various encoding/decoding options:16-bit linear, G.722, G.711 A/µlaw
- Send and receive path equalizers

ZLS38052.2 (Glass Break and Energy Detectors)

- Detects T3 (Temporal smoke alarm) signals
- Detects T4 (Temporal carbon monoxide alarm) signals
- Detects the sound of breaking glass
- Programmable Energy Detector

ZL38052 Hardware Features

- DSP with Voice Hardware Accelerators

- 2 digital microphone interfaces allowing sampling of up to 4 digital Microphones
- 2 independent headphone drivers
  - Dual 16-bit digital-to-analog converters (DACs)
  - 16 ohms single-ended or differential drive capability
  - 32 mW output drive power into 16 ohms
- 2 Time-Division Multiplexing (TDM) buses
  - The ports can be configured for Inter-IC Sound (I^2S) or Pulse-Code Modulation (PCM) operation
  - PCM operation supports PCM and GCI timing, I^2S operation supports I^2S and left justified timing
  - Each port can be a clock master or a slave
  - Each port supports up to four bi-directional streams when configured in PCM mode or two bi-directional streams when configured for I^2S mode at data rates from 128 kb/s to 8 Mb/s
- 2 Serial Peripheral Interface (SPI) ports
  - The SPI Slave port is recommended as the main communication port with a host processor. The port provides the fastest means to Host Boot and configures the device's firmware and configuration record.
  - The Master SPI port is used to load the device's firmware and configuration record from external Flash memory (Auto Boot).
- Inter-Integrated Circuit (I^2C) Port (pins shared with SPI Slave Port)
  - The I^2C port can be used as the main communication port with a host processor, and can be used to Host Boot and configure the device's firmware and configuration record
- General purpose Universal Asynchronous Receiver/Transmitter (UART) port for debug
  - The UART port can be used as a debug tool and is used for tuning purposes
- 14 General Purpose Input/Output (GPIO) pins (full operation with Full Duplex Communication Firmware, limited operation with Alarm, Glass Break And Energy Detector Firmware)
  - GPIO ports can be used for interrupt and event reporting, fixed function control, bootstrap options, as well as being used for general purpose I/O for communication and controlling external devices

The *MiTuner*™ Automatic Tuning Kit and ZLS38508 MiTuner GUI

Microsemi's Automatic Tuning Kit option includes:

- Audio Interface Box hardware
- Microphone and Speaker
- ZLS38508 *MiTuner* GUI software
  - Allows tuning of Microsemi's *AcuEdge* Technology Audio Processor

The ZLS38508 software features:

- Auto Tuning and Subjective Tuning support
- Allows tuning of key parameters of the system design
- Provides visual representations of the audio paths with drop-down menus to program parameters, allowing:
  - Control of the audio routing configuration
  - Programming of key building blocks in the transmit (Tx) and receive (Rx) audio paths
  - Setting analog and digital gains
- Configuration parameters allow users to "fine tune" the overall performance

Tools

- ZLK38000 Evaluation Kit
- *MiTuner*™ ZLS38508 and ZLS38508LITE GUI
- *MiTuner*™ ZLE38470BADA Automatic Tuning Kit

1.0 ZL38052 Device Overview

The Microsemi ZL38052 Audio Processor powered by ZLS38052 *AcuEdge*™ Technology Firmware is ideal for providing high definition audio to IP cameras. The ZL38052 has two primary modes of operation 1) Full Duplex Communication mode and 2) Sound Classifier mode.

In general, the two modes of operation provide the following functionality:

Full Duplex Communication Mode

This mode offers a high performance two way audio solution offering the following features:

- Wide band (16 kHz sampling) operation
- Configurable Acoustic Echo Canceler (AEC)
  - Programmable echo cancellation tail length up to 256 ms
  - Non-linear Acoustic Echo Controller
  - Non-Linear Processor (NLP)
- Beamforming with two or three microphone array
- Sound Locator identifies the direction of the loudest audio source, providing alerts of potential interest
- Patented Psycho-Acoustic Noise Reduction – up to 20 dB for white noise
- Integrated Compressor / Limiter / Expander enhances intelligible speech from significant distances
- Patented Anti-Howling – reduces oscillation in echo canceller audio path, including co-located devices
- Parametric Equalizers in the Send and Receive paths
- Programmable Tone Generators to generate DTMF, tone ringer, and test tones
- Cross Point Switch provides signal mixing
- Programmable coding (μ/A-law ITU-T G.711, G.722, or 16- bit linear) at line interface

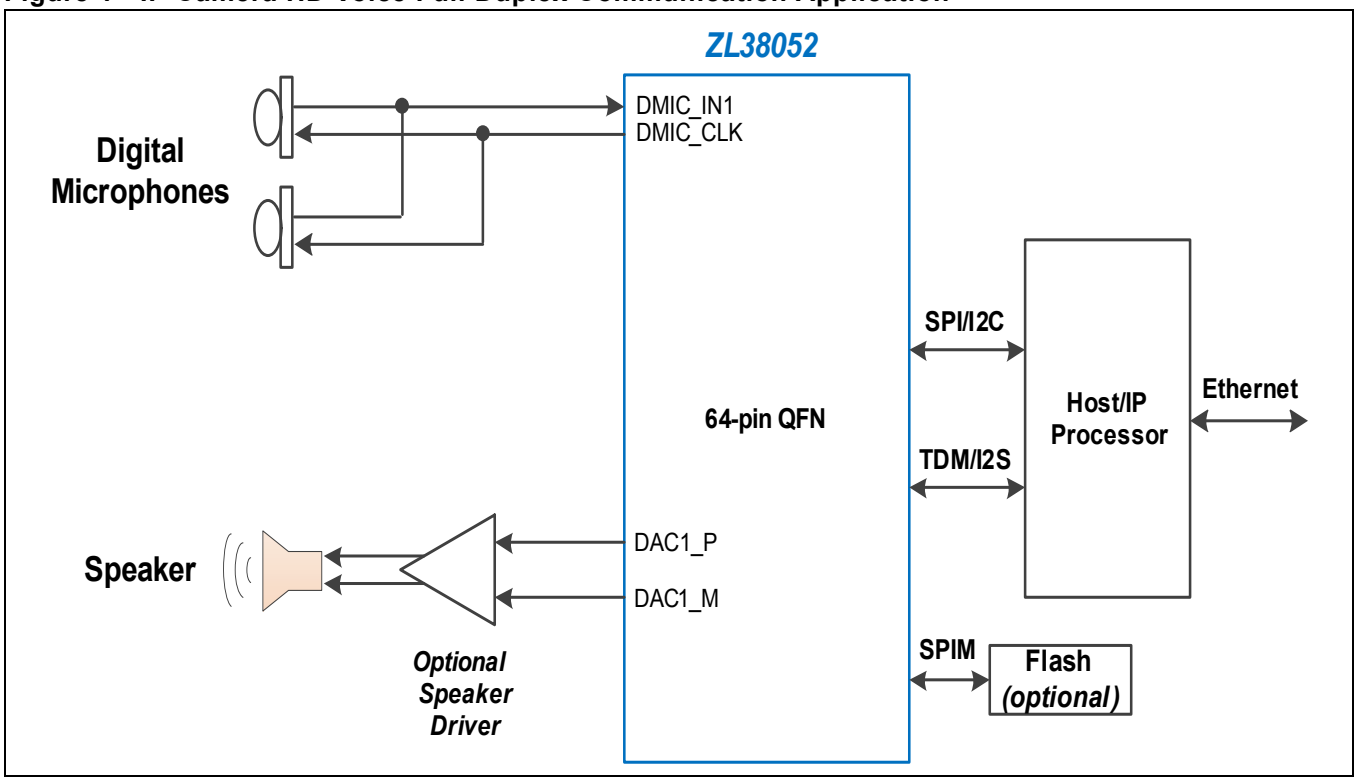
Sound Classifier Mode

The mode offers a sound classification feature with the following features:

- Smoke detector alarm (T3)
- Carbon monoxide alarms (T4)
- Glass break detector
- Programmable Energy Detector

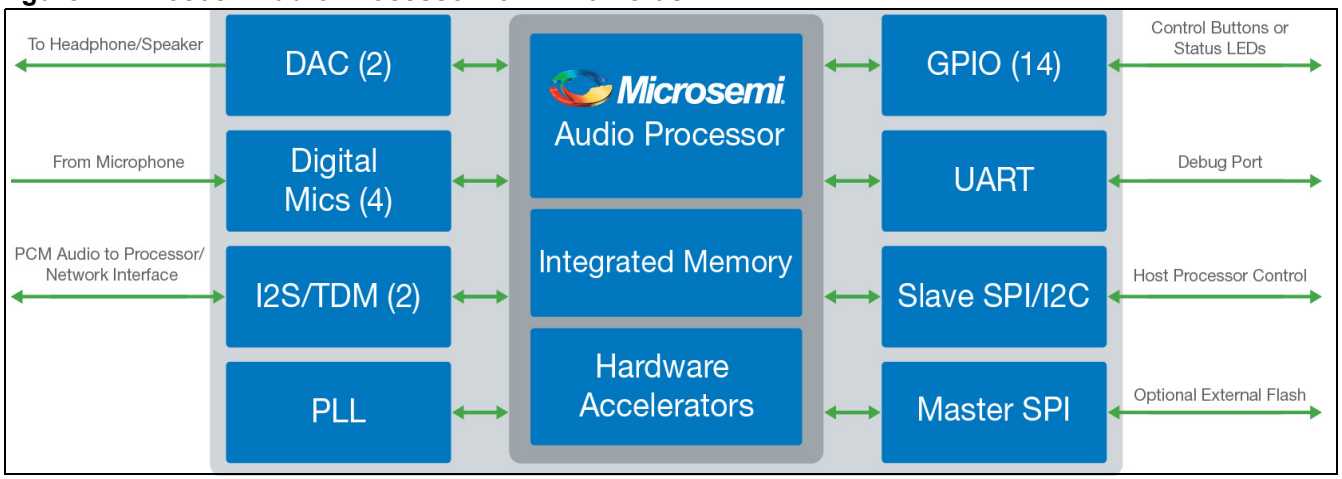
A typical IP Camera application is presented in Figure 1.

Figure 1 - IP Camera HD Voice Full Duplex Communication Application



The main functional blocks of the ZL38052 device are shown in Figure 2.

Figure 2 - ZL38052 Audio Processor for IP Cameras



2.0 Firmware

The two modes of operation in the ZL38052 (Full Duplex Communication and Sound Classification) are selected depending on which Firmware is loaded into the device. The Firmware is initially loaded at power up, either from external serial Flash or from a host controller (see 7.0, “Device Booting and Firmware Swapping“ on page 31). Real time switching between the two Firmware modes can be done during normal operation, however this requires a host controller to support. There are timing constraints that should be noted for Firmware Swapping (see 11.2, “Host Bus Interface Timing Parameters“ on page 55 for more information).

The ZL38052 Firmware Manual provides detailed information on the use of the two firmware modes of operation for the ZL38052 and should be consulted.

The majority of the signal processing (AEC, Equalization, Noise Reduction, Beamforming, CLE, etc.) runs in the Audio Processor Block at 16 kHz. Each of the audio inputs (Digital Mics, I^2S/TDM) and outputs (DACs, I^2S/TDM) can be routed amongst themselves or to the Audio Processor via a highly configurable Cross Point Switch.

The ZL38052 device provides the following peripheral interfaces:

- 2 digital microphone interfaces allowing sampling of up to 4 digital microphones
- 2 Time-Division Multiplexing (TDM) buses
  - The ports can be configured for Inter-IC Sound (I^2S) or Pulse-Code Modulation (PCM) operation
  - PCM operation supports PCM and GCI timing, I^2S operation supports I^2S and left justified timing
  - Each port can be a clock master or a slave
  - Each port supports up to four bi-directional streams when configured in PCM mode or two bi-directional streams when configured for I^2S mode at data rates from 128 kb/s to 8 Mb/s
  - Sample rate conversions are automatically done when data is sent/received at different rates than is processed internally
- SPI – The device provides two Serial Peripheral Interface (SPI) ports
  - The SPI Slave port is recommended as the main communication port with a host processor. The port provides the fastest means to Host Boot and configure the device's firmware and configuration record*.
  - The Master SPI port is used to loads the device's firmware and configuration record from external Flash memory (Auto Boot).
- I^2C - The device provides one Inter-Integrated Circuit (I^2C) port. (pins are shared with the SPI Slave port)
  - The I^2C port can be used as the main communication port with a host processor, and can be used to Host Boot and configure the device's firmware and configuration record.
- UART – The device provides one Universal Asynchronous Receiver/Transmitter (UART) port
  - The UART port can be used as a debug tool and is used for tuning purposes.
- GPIO – The device provides 14 General Purpose Input/Output (GPIO) ports (full operation with Full Duplex Communication Firmware, limited operation with Alarm, Glass Break And Energy Detector Firmware).
  - GPIO ports can be used for interrupt and event reporting, fixed function control, bootstrap options, as well as being used for general purpose I/O for communication and controlling external devices.
  - The 56 pin WLCSP package is limited to 11 GPIOs.

* Note: The configuration record is a set of register values that are customizable by the application developer to configure and tune the ZL38052 for a particular design. Refer to the Microsemi AcuEdge™ Technology ZLS38052 Firmware Manual for firmware and configuration record information.

2.1 Full Duplex Communication Mode (Firmware ZLS38052.0)

The ZLS38052.0 Firmware offers a sophisticated audio compressor/limiter/expander (CLE) with adjustable attack and decay time. This feature along with Beamforming and advanced Noise Reduction allows for Far Field Microphone pick-up.

The full duplex communication firmware (ZLS38052.0) supports the following additional ports:

- 2 independent headphone drivers
  - Dual 16-bit digital-to-analog converters (DACs)
  - 16 ohms single-ended or differential drive capability

- 32 mW output drive power into 16 ohms

2.2 Sound Classifier Mode (Firmware ZLS38052.2)

This mode of operation uses a single microphone input to be able to provide enhanced Sound Classification. This mode of operation supports:

- Detects T3 (temporal smoke alarm) signals
- Detects T4 (temporal carbon monoxide alarm) signals
- Detects the sound of breaking glass
- Programmable Energy Detector

Refer to the *Microsemi AcuEdge™ Technology ZLS38052 Firmware Manual* for more information on the Firmware options and usage for the ZL38052.

3.0 Audio Interfaces

3.1 Digital Microphone Interface

The ZL38052 supports up to four digital microphones using the DMIC_CLK, DMIC_IN1, and DMIC_IN2 interface pins.

The ZL38052 digital microphone clock output (DMIC_CLK) is either 1.024 MHz or 3.072 MHz depending on the selected TDM-A sample rate. Selecting 16 kHz TDM-A sample rate corresponds to a 1.024 MHz digital microphone clock and selecting a 48 kHz sample rate corresponds to a 3.072 MHz digital microphone clock. Microphone data is decimated and filtered to operate at 16 kHz sampling rate of the Audio Processing block. When there is no TDM-A bus to set the sample rate, the ZL38052 will operate from the crystal (or clock oscillator) and will pass digital audio from the microphones operating at a 48 kHz sampling rate.

When in full duplex communication mode, AEC can be performed on up to three microphones selected to go to the ZL38052 voice processing section, the other paths may be routed to the TDM bus for use by the host or an external Codec. Alternatively the host processor can switch different microphones to the voice processing inputs. Note that when in sound classification mode, only one microphone is used/required. It runs at 1.024 MHz sampling rate.

A stereo digital microphone, or two separate mono digital microphones, can send two microphone channels on one pin by sending the data for one channel on the rising edge and one channel on the falling edge. The selection for which clock edge is used to clock in the microphone data (rising/falling) is done via the Microphone Enable Configuration register (host writable over the HBI) or in the configuration record (loaded from Flash). Various digital microphone interfaces are presented in Figures 3 - 5.

An electret condenser microphone can be used with the digital microphone input by using a Digital Electret Microphone Pre-Amplifier device as shown in Figure 6.

Beamforming can be performed with 2 or 3 microphones. The Beamformer uses the signals from multiple microphones to determine the direction of arrival of various sound sources. The Beamformer accepts those sources that it determines are in the direction of interest and attenuates those that are deemed to be coming from other directions. By attenuating anything outside of the beam, the distance of microphone pick-up improves and interfering sounds are reduced. The Beamformer's beam width, steering angle, and out-of-beam attenuation are programmable. The physical spacing between microphones is important when implementing Beamforming. Beamforming with two microphones is most optimal when the microphones are spaced 50mm to 60mm apart. When using three microphones, the optimal spacing is 30mm apart. The microphones must also be oriented along the same plane and face the same direction. Please consult with Microsemi applications support for more information when optimizing the design for Beamforming.

In addition to Beamforming, the Microsemi *AcuEdge™* Technology Sound Location feature reports the angle at which a sound arrives at the microphone array (2 or 3 microphones).

Figure 3 - Single Mono Digital Microphone Interface – Full Duplex Communications Mode or Sound Classification Mode

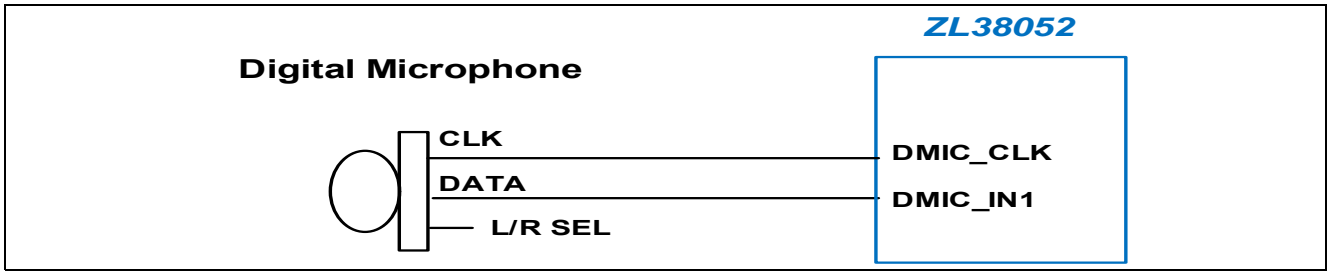


Figure 4 - Dual Microphone or Stereo Digital Microphone Interface – Full Duplex Communications Mode

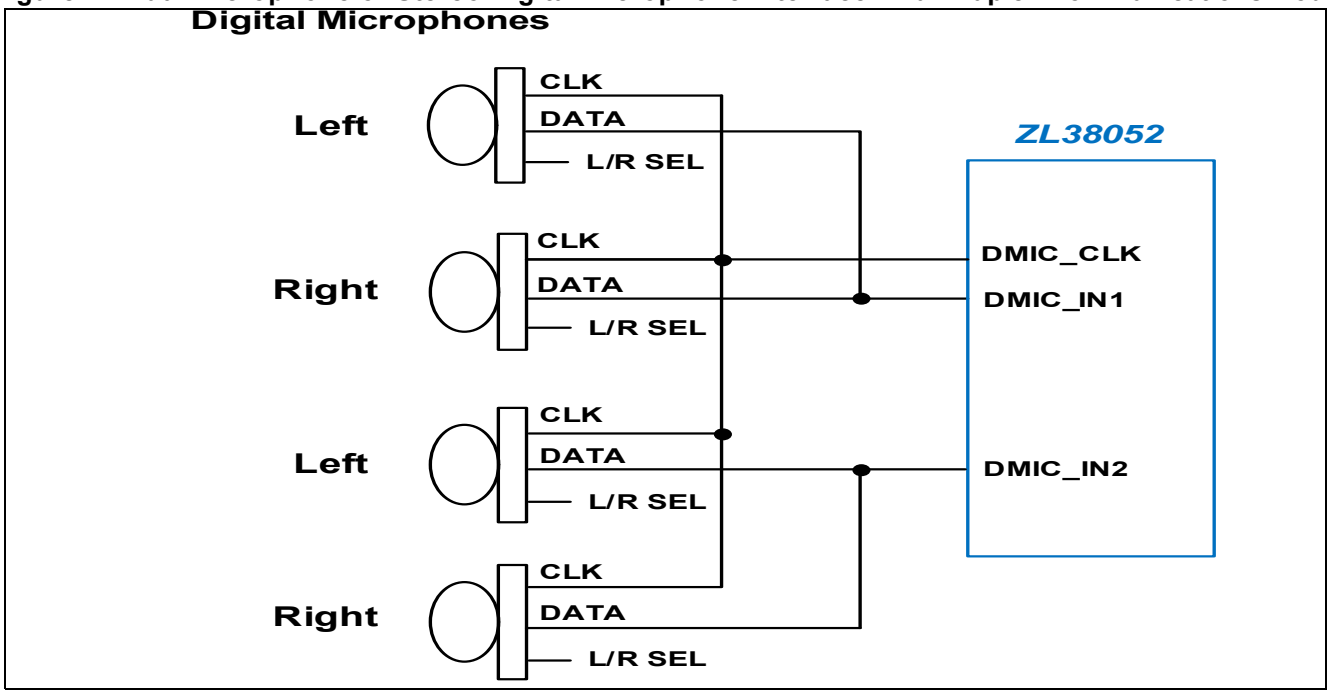
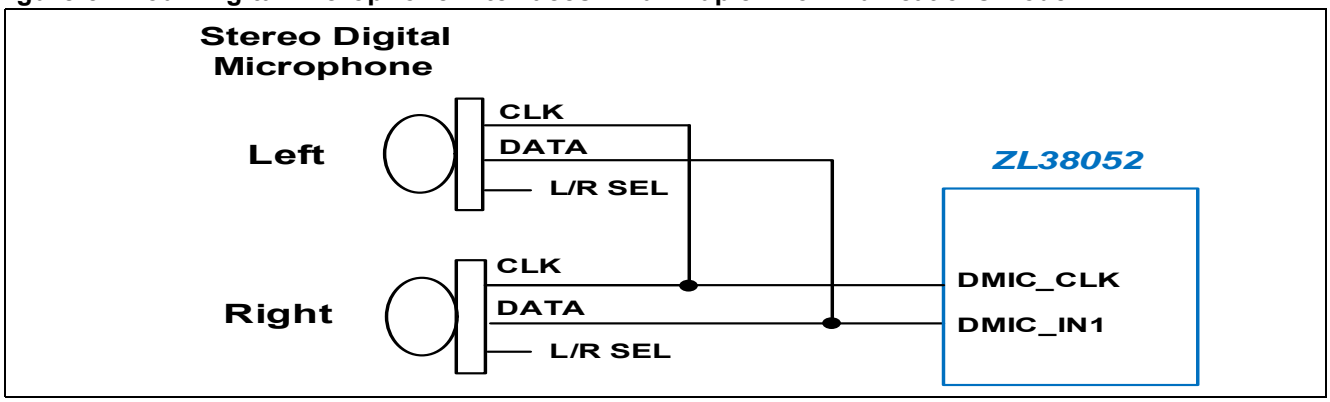


Figure 5 - Four Digital Microphone Interfaces – Full Duplex Communications Mode



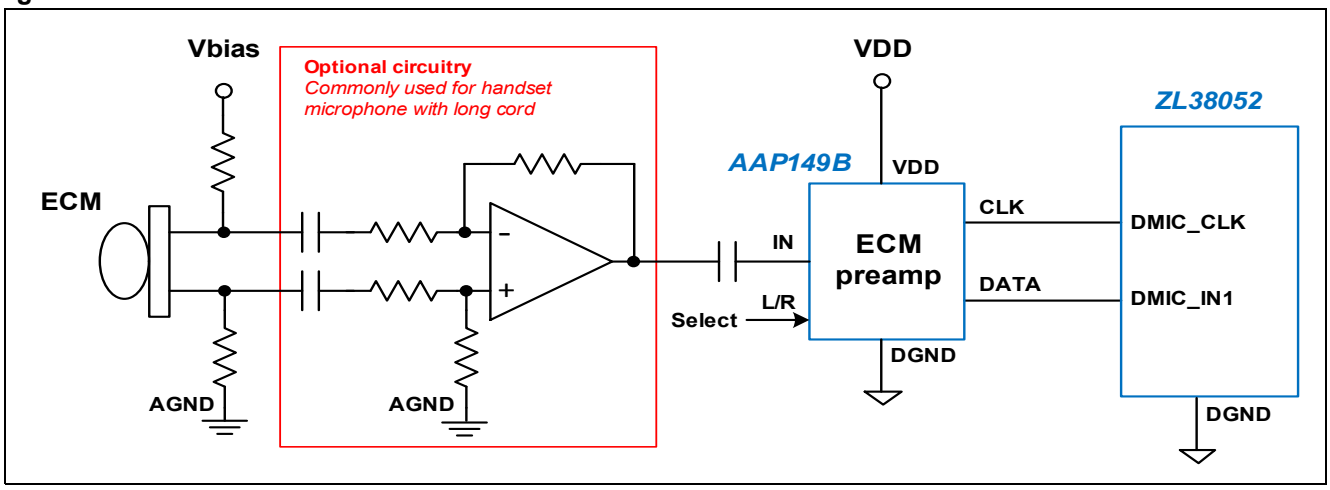
3.1.1 Analog Microphone Use

To use analog electret condenser microphones (ECM) with the digital microphone interface, a Digital Electret Microphone Pre-Amplifier device is required. Figure 6 illustrates an analog microphone connection.

The analog microphone is wired to an optional differential amplifier which amplifies and converts the microphone signal to single-ended. The microphone signals are then further amplified and digitized through the Digital Electret Microphone Pre-Amplifiers and applied to the ZL38052 digital microphone input. A Microsemi AAP149B ECM Pre-Amplifier is shown.

The ZL38052 provides the clock to activate the Digital Electret Microphone Pre-Amplifier.

Figure 6 - ECM Circuit



When using an analog microphone, operation in Low-Power mode is not recommended. For more information, see 10.4, “Device Operating Modes“ on page 43.

3.2 DAC Output

The ZL38052 has two 16-bit fully differential delta-sigma digital-to-analog converters. The two output DACs independently drive an analog output subsystem. Each subsystem is able to drive two output pins, representing four independent single-ended headphone outputs that can be driven by two independent data streams. The pins can be independently configured. Four analog gains on each headphone output are provided and can be set to: 1x, 0.5x, 0.333x, or 0.25x.

Note: Only the positive DAC outputs are available with the 56-ball WLCSP package. The 56-ball WLCSP package provides two independent single-ended headphone outputs that can be driven by two independent data streams.

The headphone amplifiers are self-protecting so that a direct short from the output to ground or a direct short across the terminals does not damage the device.

The ZL38052 provides audible pop suppression which reduces pop noise in the headphone earpiece when the device is powered on/off or when the device channel configurations are changed. This is especially important when driving a headphone single-ended through an external capacitor (see 3.2.2, “Output Driver Configurations“, configuration C).

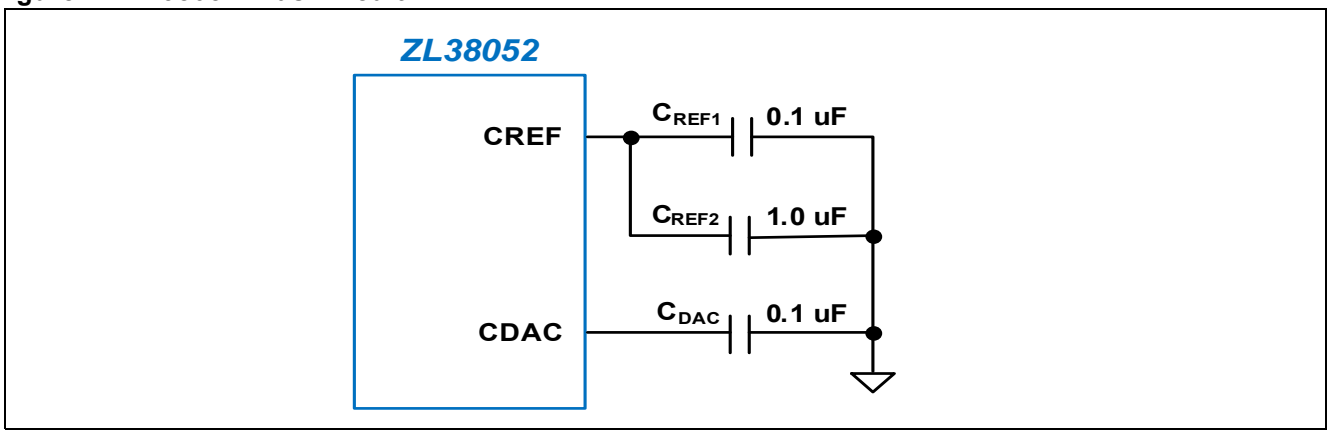
The DACs and headphone amplifiers can be powered down if they are not required for a given application. To fully power down the DACs, disable both the positive and negative outputs.

3.2.1 DAC Bias Circuit

The common mode bias voltage output signal (CREF) for the DAC output buffers must be decoupled through a 0.1 µF (C_{REF1}) and a 1.0 µF (C_{REF2}) ceramic capacitor to VSS. The positive DAC reference voltage output (CDAC) must be decoupled through a 0.1 µF (C_{DAC}) ceramic capacitor to VSS as shown in Figure 7.

All capacitors can have a 20% tolerance and should have a minimum voltage rating of 6.3 V.

Figure 7 - ZL38052 Bias Circuit



3.2.2 Output Driver Configurations

Figure 8 shows the different possible output driver configurations for the 64-pin QFN package. When using the 56-ball WLCSP package, only the positive outputs DAC1_P and DAC2_P are provided.

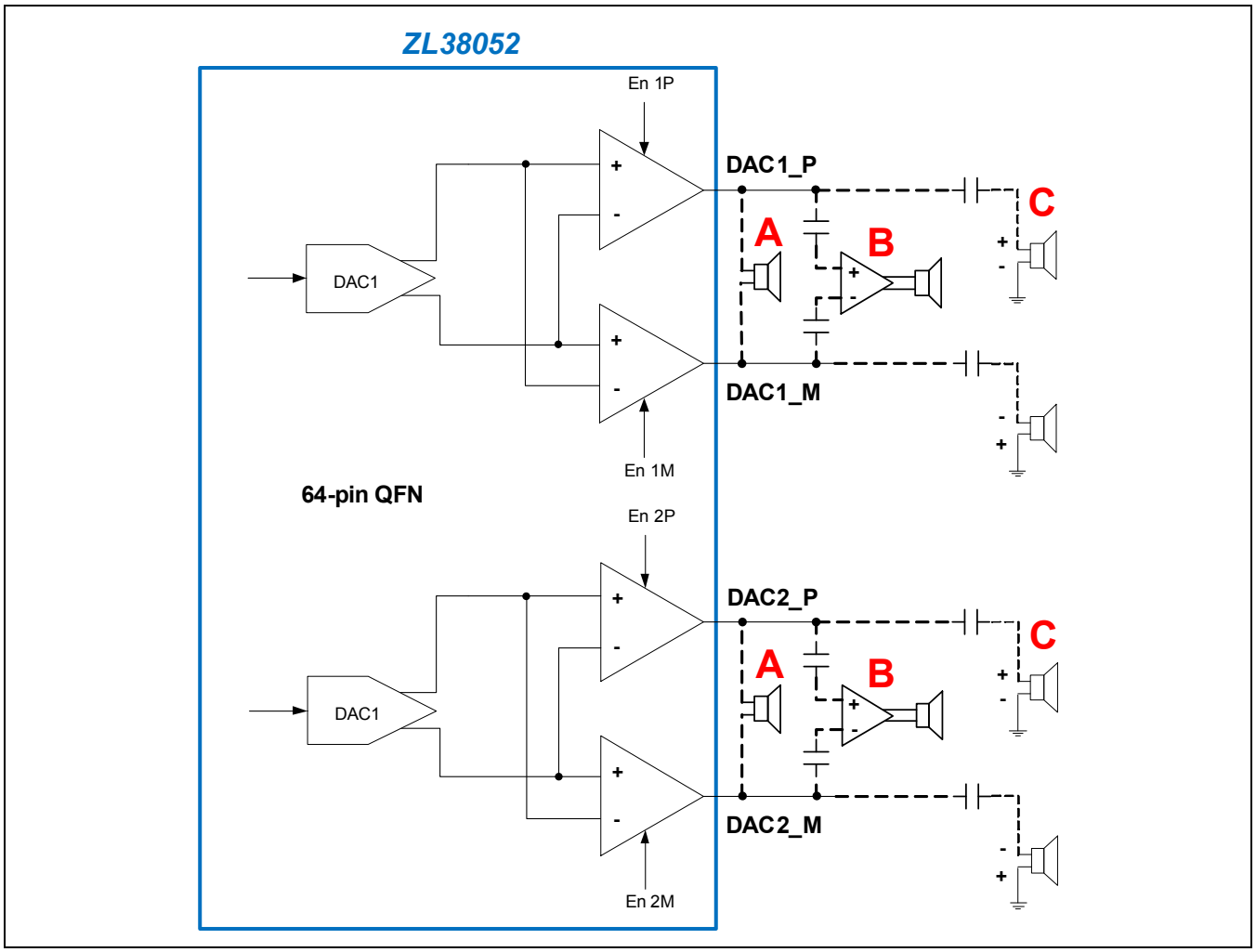
The two output DACs independently drive positive and negative headphone driver amplifiers. The output pins can be independently configured in the following ways:

A. 64-pin QFN – Direct differential drive of a speaker as low as 32 ohms. For this configuration an analog gain of 1x is commonly used. (Differentially driving a 16 ohm speaker is possible, but only with the same amount of power as in the single-ended case. The signal level must be reduced to not exceed ½ scale in this case.)

B. 64-pin QFN – Direct differential drive of a high impedance power amplifier. A Class D amplifier is recommended for this speaker driver. Use an ON Semiconductor® NCP2820 or equivalent. A 1 μF coupling capacitor is generally used with the Class D amplifier. The analog gain setting depends on the gain of the Class D amplifier, analog gain settings of 0.25x or 0.5x are commonly used.

C. Both packages – Driving either a high impedance or a capacitively coupled speaker as low as 16 ohms single-ended. For this configuration an analog gain of 1x is commonly used. The coupling capacitor value can vary from 10 μf to 100 μf depending on the type of earpiece used and the frequency response desired.

Figure 8 - Audio Output Configurations



4.0 Digital Interfaces

4.1 TDM Interface

The ZL38052 device has two generic TDM interfaces, TDM-A and TDM-B. Each interface consists of four signals:

- Data clock (PCLK/I2S_SCK)
- Data rate sync (FS/I2S_WS)
- Serial data input (DR/I2S_SDI)
- Serial data output (DX/I2S_SDO)

The TDM ports can be configured for Inter-IC Sound (I^2S) or Pulse-Code Modulation (PCM) operation.

Each TDM block is capable of being a master or a slave, however both highways must be synchronous to each other (derived from a common clock domain).

Operation of the TDM interfaces are subject to the following limitations.

Table 1 - Allowable TDM Configurations

TDM-A Mode	TDM-B Mode	Supported Sample Rates[3] (kHz)	Requirements / Limitations
Master	Master	8, 16, 48	Both TDM-A and TDM-B must be configured for the same data clock and data sync.
Master	Slave-Synchronous		The TDM-B sync rate must either be the same as the TDM-A sync rate or 48 kHz.
Slave[1]	Master	8, 16, 48[1]	
Slave[1]	Slave-Synchronous[2]		

Note 1: When TDM-A is a slave, then the device can be run without a crystal. However, this mode requires that the PCLKA and FSA signals are always present and PCLKA must be an integer multiple of 2.048 MHz. For crystal-less operation at power-on, PCLKA will be auto-detected with only 8 kHz and 16 kHz frame syncs being allowed.

Note 2: This combination requires that both TDM-A clock and TDM-B clock be physically connected to the same source.

Note 3: The Audio Processing block accepts these sample rates but the Audio Processing block always runs at a 16 kHz sampling rate.

While a TDM bus configuration may carry many encoded audio streams, the ZL38052 device can only address a maximum of 4 bi-directional audio streams per TDM bus. These four audio streams are referred to as channels #1 through #4, and each of these channels can be independently configured to decode any of the TDM bus's audio streams.

For a given TDM bus, once it is configured for a data sample rate and encoding, all data rates and encoding on that bus will be the same. 16-bit linear data will be sent on consecutive 8-bit timeslots (e.g., if timeslot N is programmed in the timeslot registers, the consecutive timeslot is N+1).

The TDM interface supports bit reversal (LSB first <– –> MSB first) and loopbacks within the TDM interface and from one interface to another (see "Cross Point Switch" on page 21).

The generic TDM interface supports the following mode and timing options.

4.1.1 I²S Mode

In I²S mode, the 4-wire TDM port conforms to the I²S protocol and the port pins become I2S_SCK, I2S_WS, I2S_SDI, and I2S_SDO (refer to Table 10 for pin definitions). Both TDM buses have I²S capability.

An I²S bus supports two bi-directional data streams, left and right channel, by using the send and receive data pins utilizing the common clock and word signals. The send data is transmitted on the I2S_SDO line and the receive data is received on the I2S_SDI line.

The I²S port can be used to connect external analog-to-digital converters or Codecs. The port can operate in master mode where the ZL38052 is the source of the port clocks, or slave mode where the word select and serial clocks are inputs to the ZL38052.

The word select (I2S_WS) defines the I²S data rate and sets the frame period when data is transmitted for the left and right channels. A frame consists of one left and one right audio channel. The I²S ports operate at 8, 16, and 48 kHz data rates as a slave or master (as specified in Table 1). Per the I²S standard, the word select is output using a 50% duty cycle.

The serial clock (I2S_SCK) rate sets the number of bits per word select frame period and defines the frequency of I2S_CLK. I²S data is input and output at the serial clock rate. Input data bits are received on I2S_SDI and output data bits are transmitted on I2S_SDO. Data bits are always MSB first. The number of clock and data bits per frame can be programmed as 8, 16, 32, 64, 96, 128, 192, 256, 384, 512, or 1024. Any input data bits that are received after the LSB are ignored.

The I^2S port operates in two frame alignment modes (I^2S and Left justified) which determine the data start in relation to the word select.

Figure 9 illustrates the I^2S mode, which is left channel first with I2S_WS (Left/Right Clock signal) low, followed by the right channel with I2S_WS high. The MSB of the data is clocked out starting on the second falling edge of I2S_SCK following the I2S_WS transition and clocked in starting on the second rising edge of I2S_SCK following the I2S_WS transition. Figure 9 shows I^2S operation with 32 bits per frame.

Figure 9 - I^2S Mode

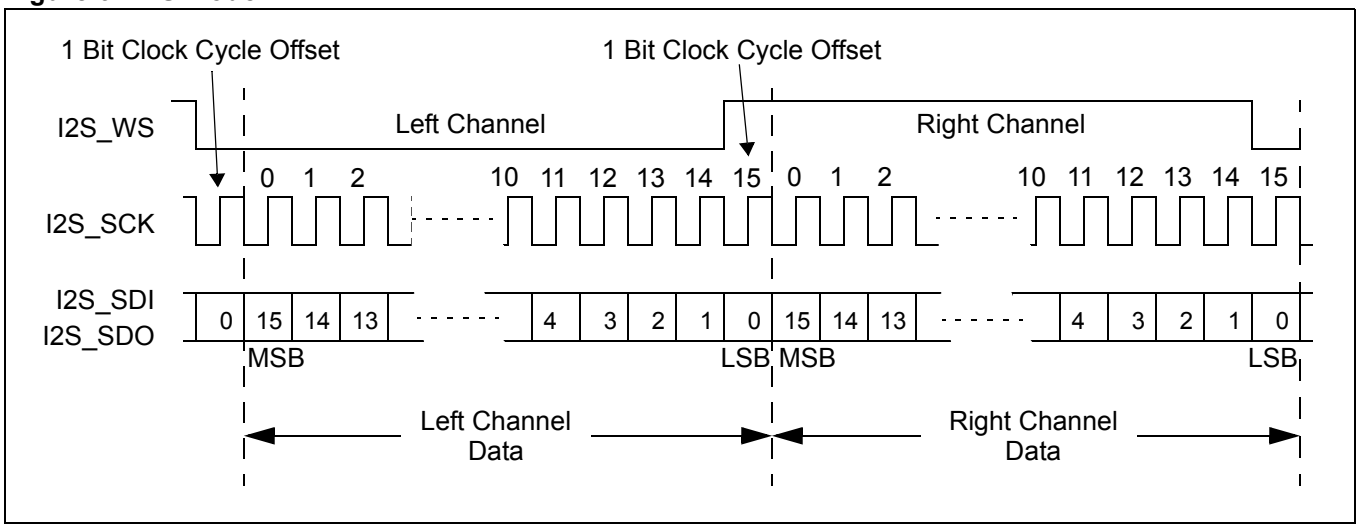
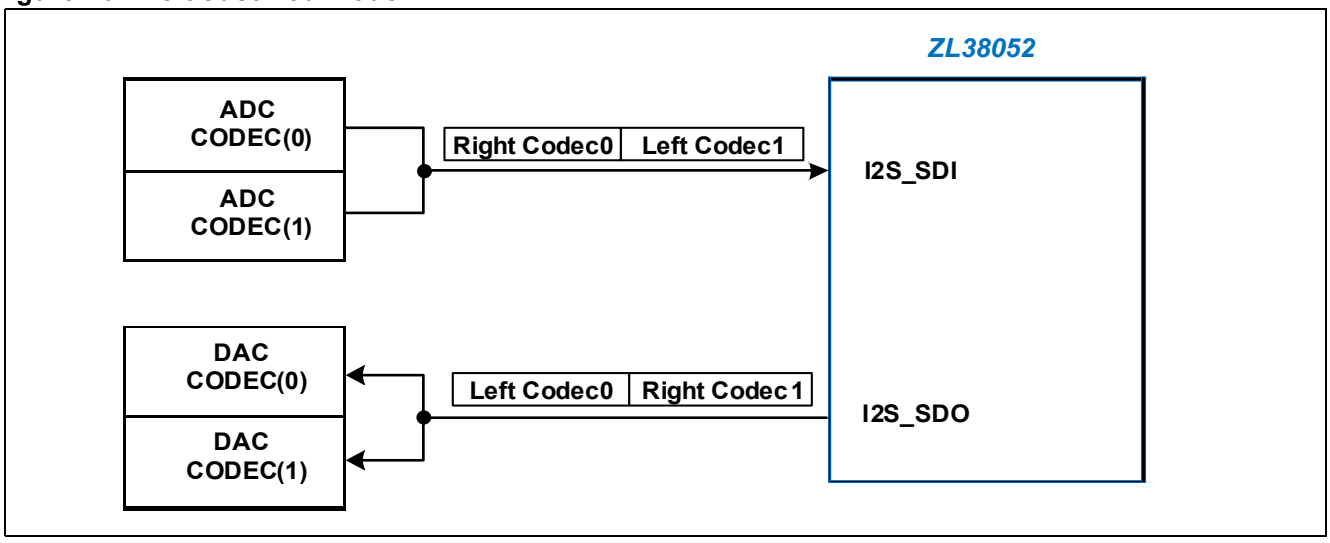


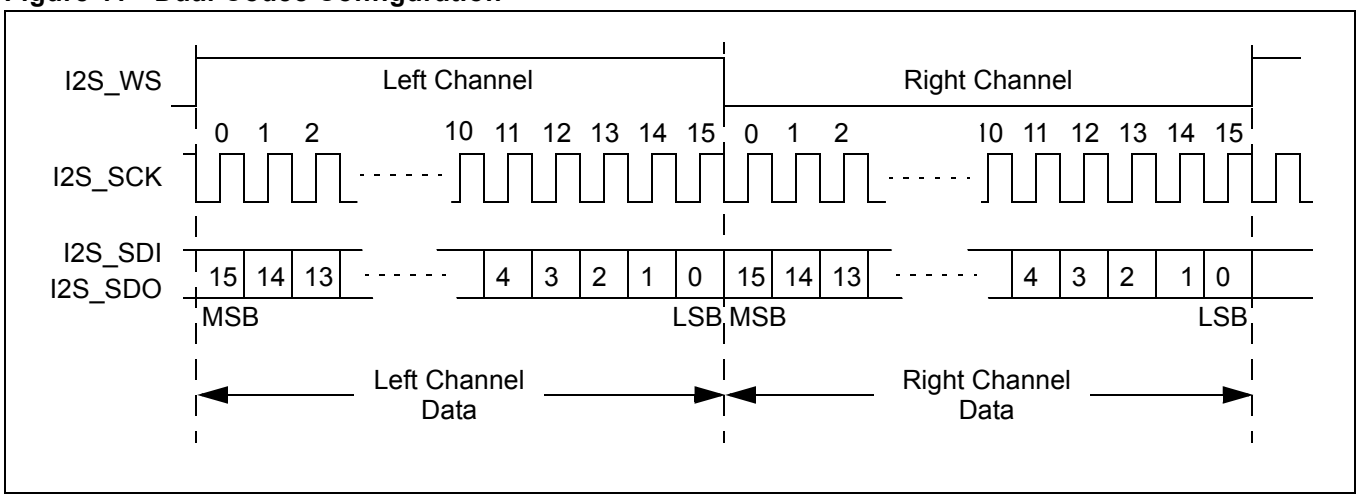
Figure 10 illustrates the left justified mode, which is left channel first associated with I2S_WS (Left/Right Clock signal) high, followed by the right channel associated with I2S_WS low. The MSB of the data is clocked out starting on the falling edge of I2S_SCK associated with the I2S_WS transition, and clocked in starting on the first rising edge of I2S_SCK following the I2S_WS transition.

Figure 10 - Left Justified Mode



Each I2S interface can support one dual channel Codec (Figure 11) through the Codec's I2S interface. The four 16-bit channel processing capacity of the DSP is spread across the two input channels from the ADCs of Codec(0) and Codec(1), and the two output channels to the DACs of Codec(0) and Codec(1).

Figure 11 - Dual Codec Configuration



Both I2S bus modes can support full bi-directional stereo communication.

The device supports I2S loopback.

See the *Microsemi AcuEdge™ Technology ZLS38052 Firmware Manual* for I2S port registers.

4.1.2 PCM Mode

Each of the PCM channels can be assigned an independent timeslot. The timeslots can be any 8-bit timeslot up to the maximum supported by the PCLK being used. The PCM ports can be configured for Narrowband G.711 A-law/μ-Law or Linear PCM or Wideband G.722 encoding. For a given TDM bus, once it is configured for a data sample rate and encoding, all data rates and encoding on that bus will be the same. 16-bit linear PCM will be sent on consecutive 8-bit timeslots (e.g., if timeslot N is programmed in the timeslot registers, the consecutive timeslot is N+1). The PCM interface can transmit/receive 8-bit compressed or 16-bit linear data with 8 kHz sampling (Narrowband), or 16-bit linear data with 16 kHz sampling (Wideband).

Wideband audio usually means the TDM bus is operating at a 16 kHz FS, but there are two other operating modes that support wideband audio using an 8 kHz FS:

- G.722 supports wideband audio with an 8 kHz FS. This uses a single 8-bit timeslot on the TDM bus.
- "Half-FS Mode" supports wideband audio with an 8 kHz FS signal. In this mode, 16-bit linear audio is received on two timeslot pairs; the first at the specified timeslot (N, N+1) and the second a half-frame later. In total, four 8-bit timeslots are used per frame, timeslots (N, N+1) and ((N + ((bits_per_frame)/16)), (N + 1 + ((bits_per_frame)/16))). The user programs the first timeslot and the second grouping is generated automatically 125/2 μs from the first timeslot.

The PCM voice/data bytes can occupy any of the available timeslots, except for PCM clock rates that have extra clocks in the last timeslot. If there is more than one extra clock in the last timeslot, the timeslot data will be corrupted, do not use the last timeslot for these clock frequencies (e.g., 3.088 MHz etc.).

The PCM block can be configured as a master or a slave and is compatible with the Texas Instruments Inc. McBSP mode timing format.

Figure 12 and Figure 13 illustrate the PCM format with slave timing, FS and PCLK are provided by the host. Slave mode accommodates frame sync pulses with various widths (see "GCI and PCM Timing Parameters" on page 51).

Figure 14 and Figure 15 illustrate the PCM format with master timing, FS and PCLK are provided by the ZL38052. Master mode outputs a frame sync pulse equal to one PCLK cycle.

Diagrams for PCM transmit on negative edge (xeDX = 0) and PCM transmit on positive edge (xeDX = 1) are shown for both slave and master timing.

Figure 12 - TDM – PCM Slave Functional Timing Diagram (8-bit, xeDX = 0)

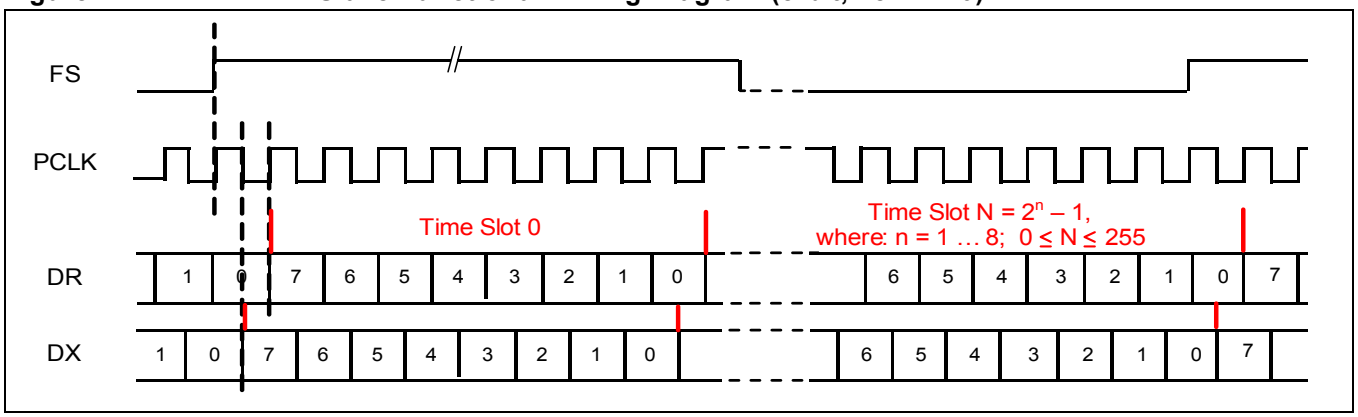


Figure 13 - TDM – PCM Slave Functional Timing Diagram (8-bit, xeDX = 1)

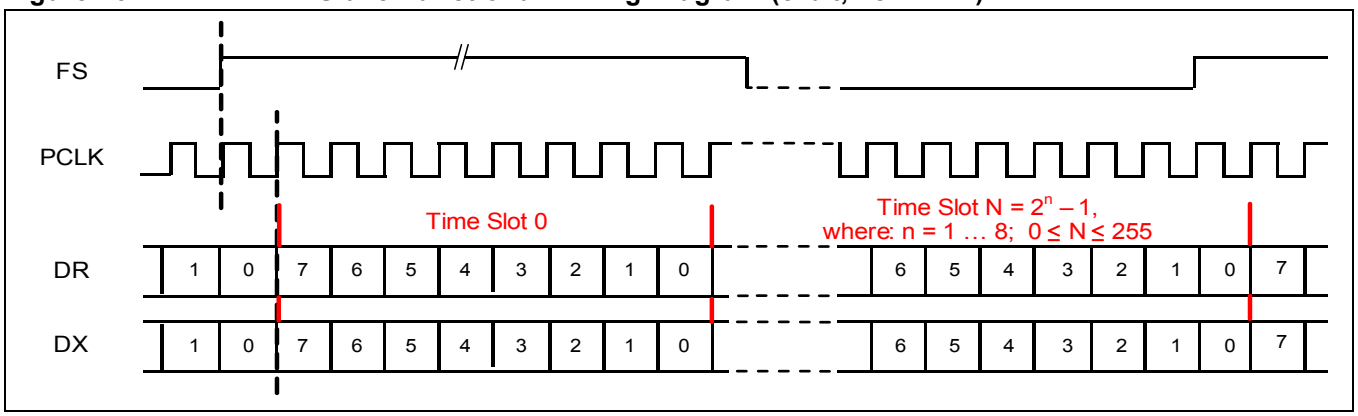


Figure 14 - TDM – PCM Master Functional Timing Diagram (8-bit, xeDX = 0)

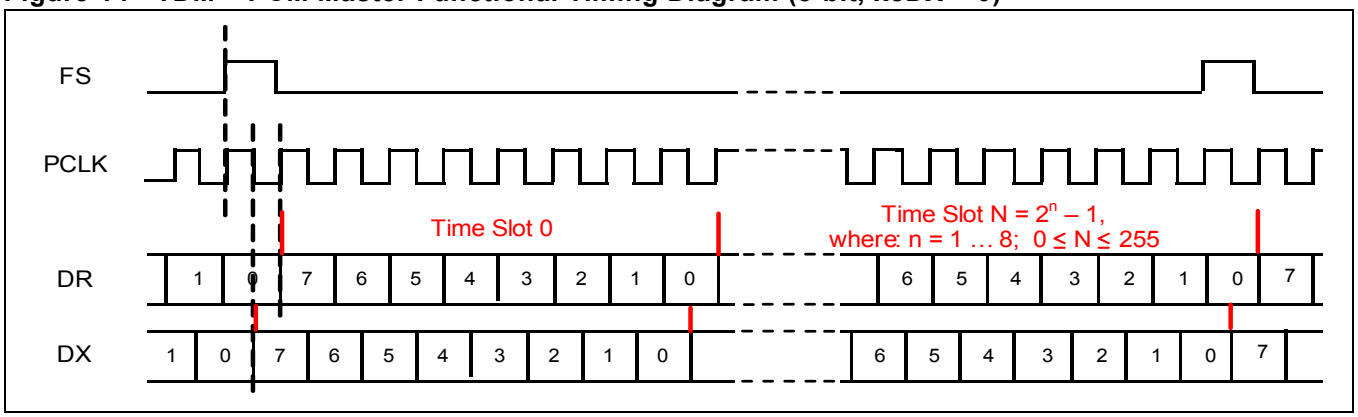
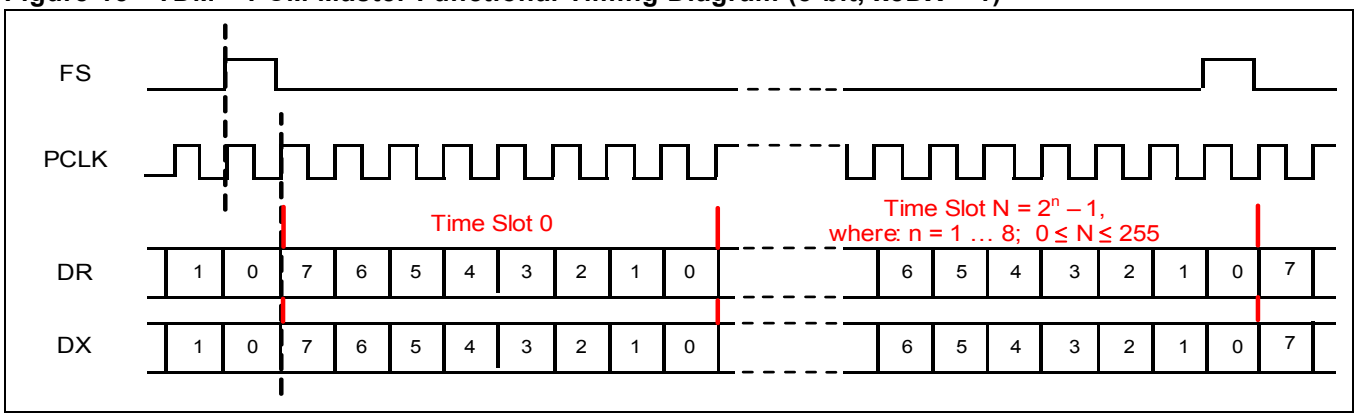


Figure 15 - TDM – PCM Master Functional Timing Diagram (8-bit, xeDX = 1)



4.1.3 GCI Mode

The GCI voice/data bytes can occupy any of the available timeslots. The GCI block can be configured as a master or a slave and supports a clock that has the same frequency as the data rate.

Note: Traditional GCI Monitor, Signalling, and Control channel bytes and double data rate are not supported.

Figure 16 illustrates the GCI format with slave timing, FS and PCLK are provided by the host. Slave mode accommodates frame sync pulses with various widths (see "GCI and PCM Timing Parameters" on page 51).

Figure 17 illustrates the GCI format with master timing, FS and PCLK are provided by the ZL38052. Master mode outputs a frame sync pulse equal to one PCLK cycle.

For both, first data bits are aligned with the rising edge of the frame sync pulse.

Figure 16 - TDM – GCI Slave Functional Timing Diagram

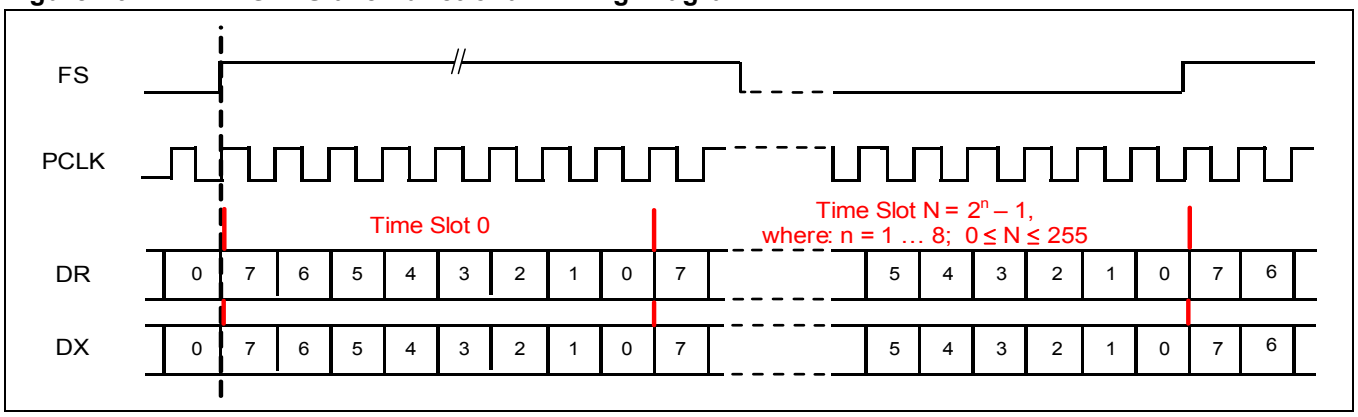
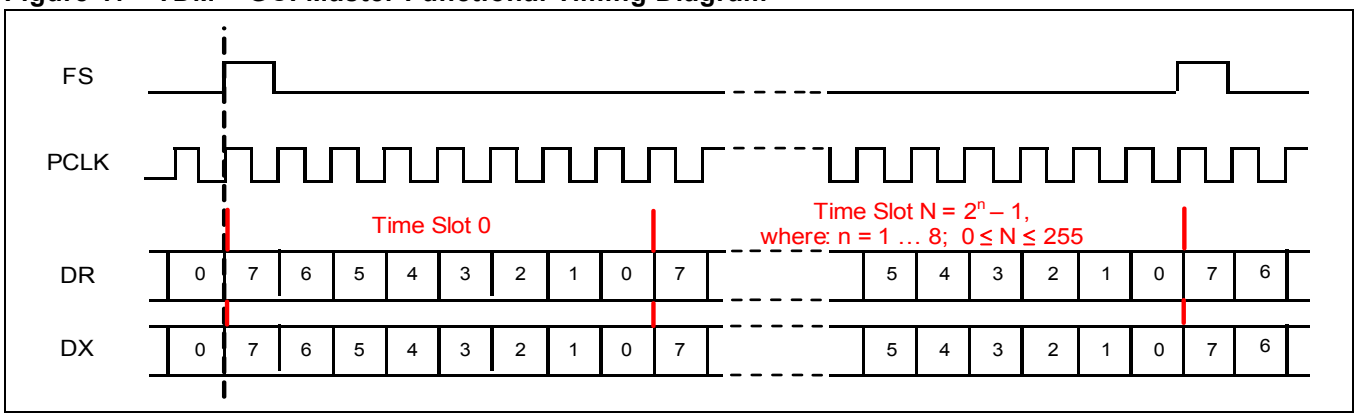


Figure 17 - TDM – GCI Master Functional Timing Diagram



4.2 Cross Point Switch

The ZL38052 contains a Cross Point Switch that allows any input port to be routed to any output port as well as routing the input/outputs to/from the audio processor functions. Refer to the *Microsemi AcuEdge™ Technology ZLS38052 Firmware Manual* for Cross Point Switch operation and control.

4.3 Host Bus Interface

The host bus interface (HBI) is the main communication port from a host processor to the ZL38052. It can be configured to be either a SPI Slave or an I^2C Slave port, either of which can be used to program or query the device.

The ZL38052 allows for automatic configuration between SPI and I^2C operation. For the HBI port, if the HCLK toggles for two cycles, the HBI will default to the SPI Slave, otherwise it will remain configured as I^2C (see Table 2). The HBI comes up listening in both SPI and I^2C modes, but with I^2C inputs selected. If HCLK is present, it switches the data selection before the first byte is complete so that no bits are lost. Once the port is determined to be SPI, a hardware reset is needed to change back to I^2C.

This port can read and write all of the memory and registers on the ZL38052. The port can also be used to boot the device, refer to "Device Booting and Firmware Swapping" on page 31.

Table 2 - HBI Slave Interface Selection

Description	Condition	Operating Mode	Notes
HBI Slave interface selection.	HCLK toggling	Host SPI bus	
	HDIN tied to VSS	Host I^2C bus. Slave address 45h (7-bit).	1
	HDIN tied to DVDD33	Host I^2C bus. Slave address 52h (7-bit).	

Note 1: By default, the HBI comes up as an I^2C interface. Toggling the HCLK pin will cause the host interface to switch to a SPI interface. If an I^2C interface is desired, HCLK needs to be tied to ground.

4.3.1 SPI Slave

The physical layer is a 4-wire SPI interface. Chip select and clock are both inputs.

The SPI Slave port can support byte, word, or command framing. Write and read diagrams for these framing modes are shown in Figure 18 – Figure 23. The SPI Slave chip select polarity, clock polarity, and sampling phase are fixed.

The ZL38052 command protocol is half duplex, allowing the serial in and serial out to be shorted together for a 3-wire connection. The chip select is active low. The data is output on the falling edge of the clock and sampled on the rising edge of the clock.

The SPI Slave supports access rates up to 25 MHz.

The outbound interrupt is always active low.

Figure 18 - SPI Slave Byte Framing Mode – Write

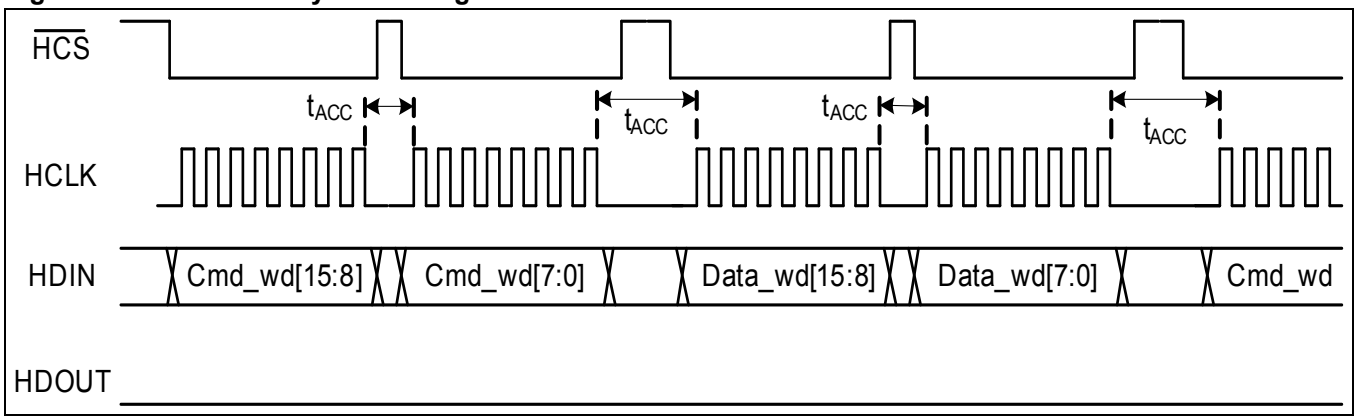


Figure 19 - SPI Slave Byte Framing Mode – Read

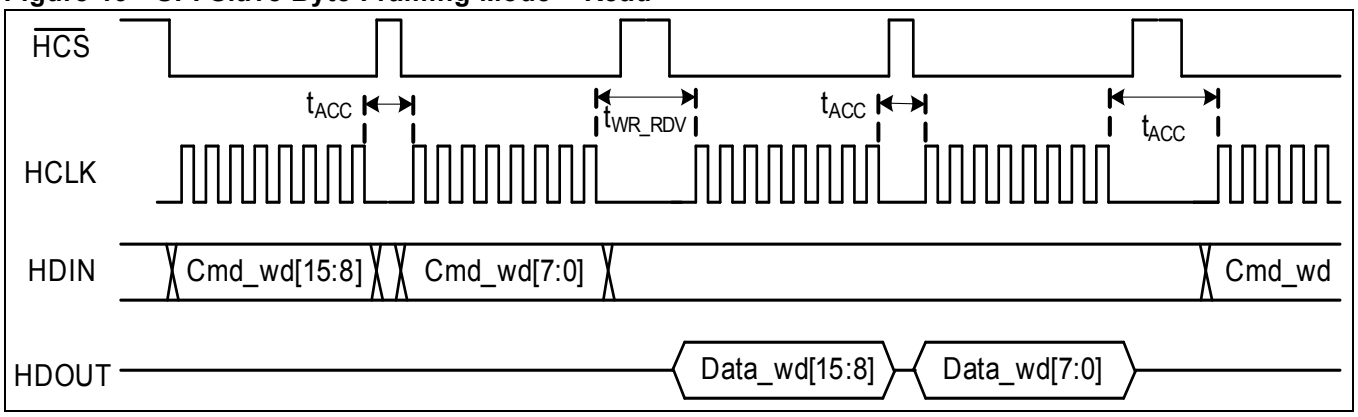


Figure 20 - SPI Slave Word Framing Mode – Write, Multiple Data Words

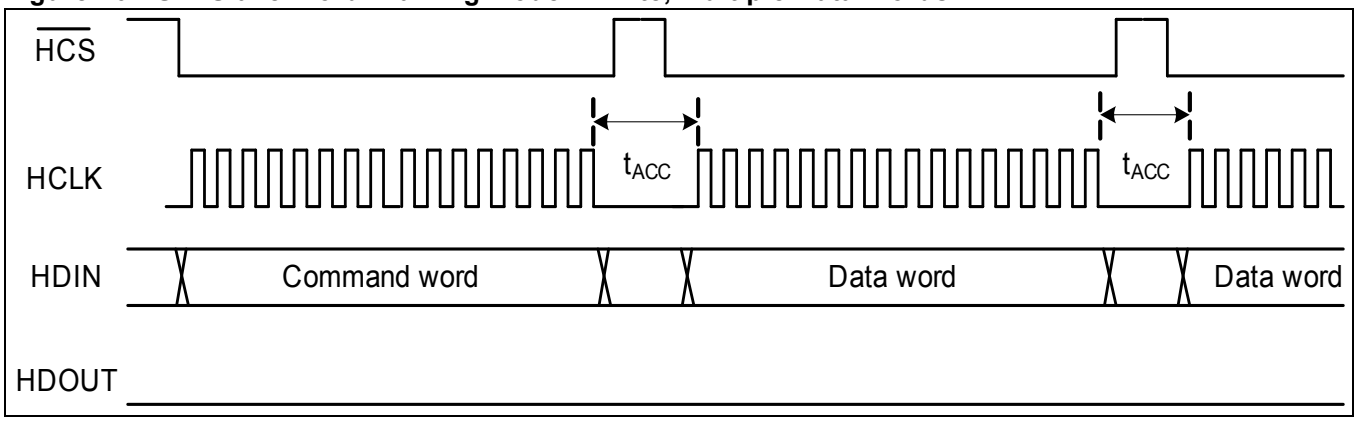


Figure 21 - SPI Slave Word Framing Mode – Read, Multiple Data Words

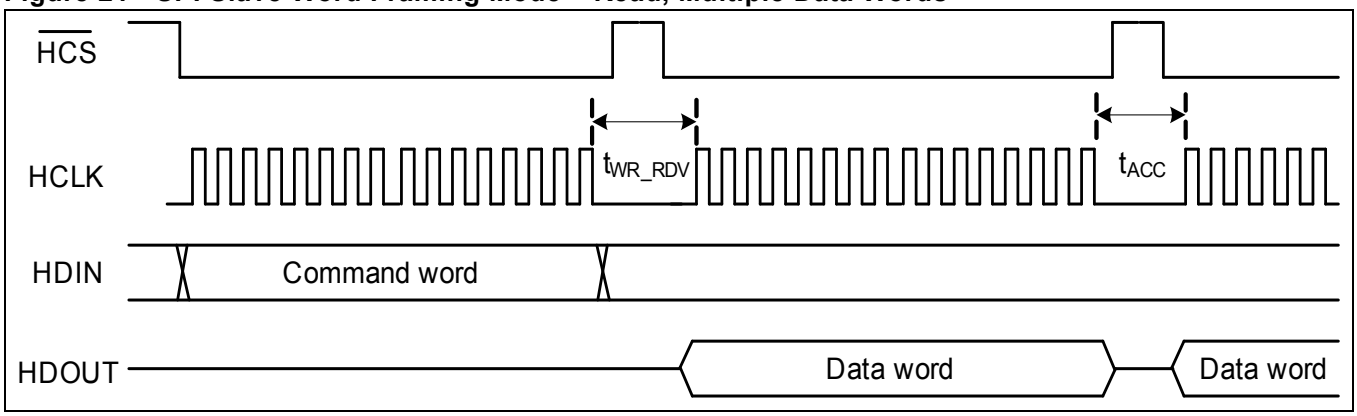


Figure 22 - SPI Slave Command Framing Mode – Write

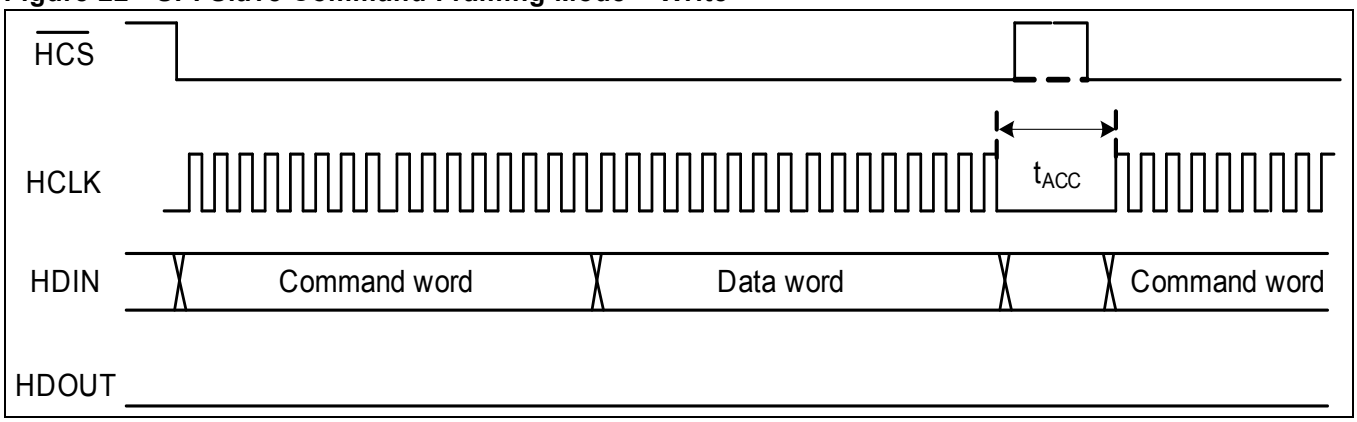
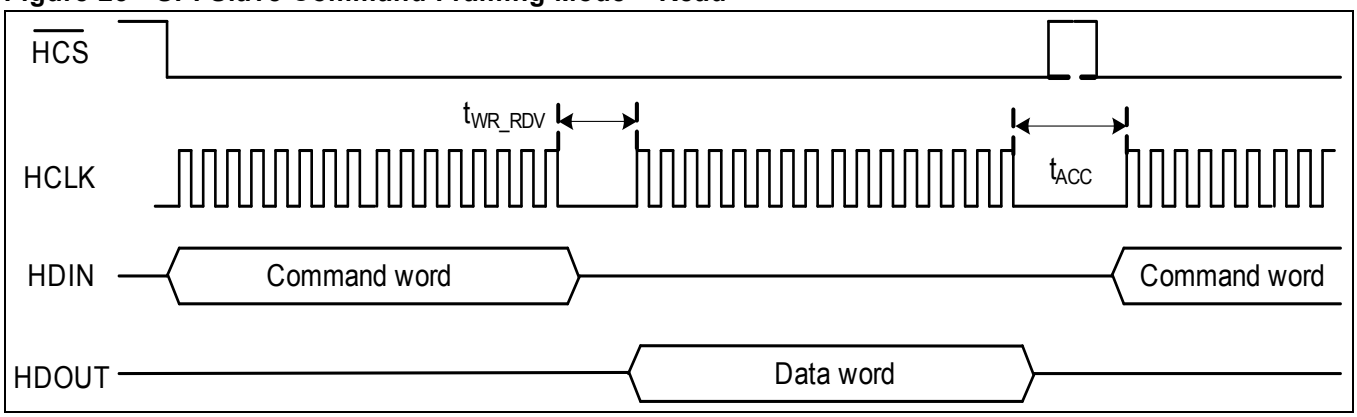


Figure 23 - SPI Slave Command Framing Mode – Read



4.3.2 I²C Slave

The I²C bus is similar to the Philips Semiconductor (NXP) 1998 Version 2.0, I²C standard. The ZL38052 I²C bus supports 7-bit addressing and transfer rates up to 400 kHz. External pull-up resistors are required on the I²C serial clock input ($\overline{HCS}$) and the I²C serial data input/output (HDOUT) when operating in this mode (note, the I²C slave pins are 3.3 V pins and are not 5 V tolerant).

The selection of the I²C slave address is performed at bootup by the strapping of the HDIN and HCLK pins, see Table 2.

4.3.3 UART

The ZL38052 device incorporates a two-wire UART (Universal Asynchronous Receiver Transmitter) interface with a fixed 115.2K baud transfer rate, 8 data bits, 1 stop and no parity. TX and RX pins allow bi-directional communication with a host. The UART pins must be made accessible on the PCB for debug and tuning purposes.

The UART port can be used as a debug tool and is used for tuning purposes.

4.3.4 Host Interrupt Pin

An internal host interrupt controller controls the active low interrupt pin which is part of the host bus interface. Associated with the interrupt controller is an event queue which reports status information for the interrupt.

Upon sensing the interrupt, the host reads the event queue to determine which event caused the interrupt. Events are enabled by the host processor, and are typically not used in a standalone (controllerless) design.

Refer to Events in the *Microsemi AcuEdge™ Technology ZLS38052 Firmware Manual* for Event ID Enumerations.

4.4 Master SPI

Like the HBI SPI Slave, the physical layer of the Master SPI is a 4-wire SPI interface supporting half duplex communication. It supports only one chip select which is multiplexed with GPIO_9.

The Master SPI is only accessible through boot ROM commands and is only used as the boot loading mechanism from an external serial Flash. The ZL38052 can automatically read the Flash data (program code and configuration record) through this interface upon the release of reset (Auto Boot), depending on the value of the bootstrap options.

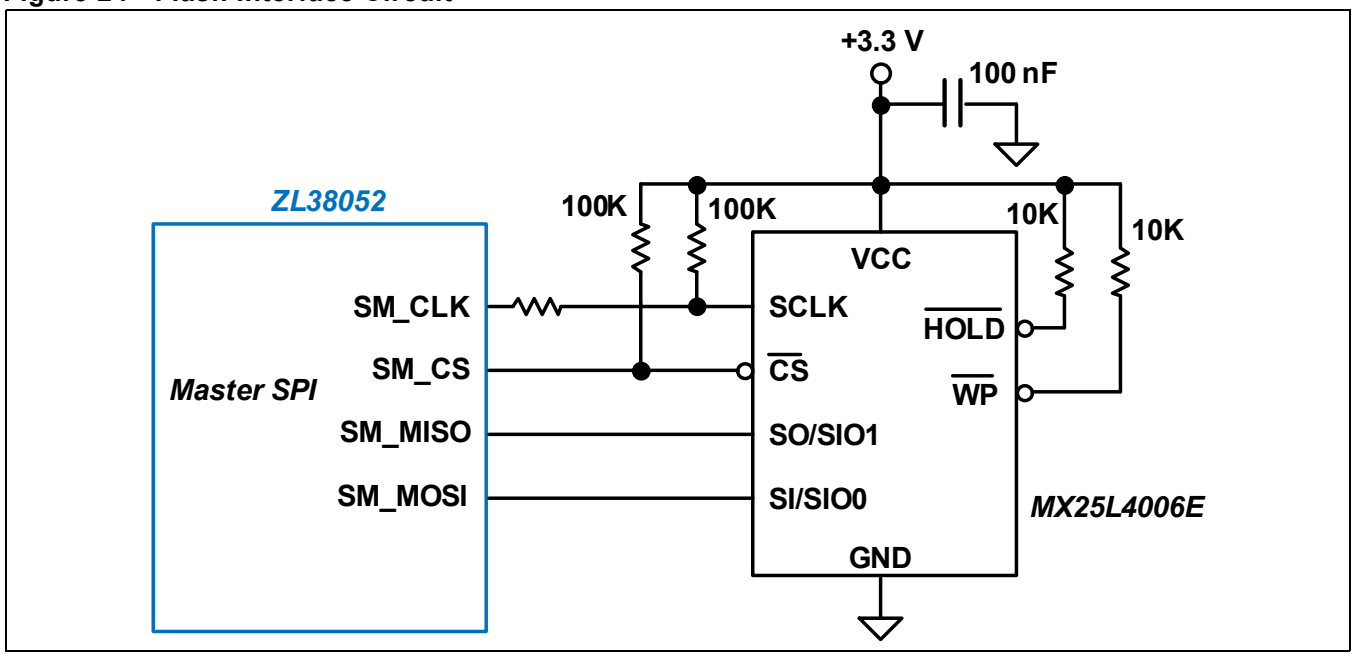
Note: An alternative to Auto Boot is to perform a Host Boot through the HBI port. Refer to 7.0, “Device Booting and Firmware Swapping“ on page 31.

4.4.1 Flash Interface

After power-up the ZL38052 will run its resident boot code, which establishes the initial setup of the Master SPI port and then loads the firmware from external Flash memory. This Flash firmware establishes the resident application and sets the modes of all the ZL38052 ports.

Figure 24 illustrates the connection of Flash memory to the ZL38052 Master SPI port. A 2 Mbit Flash is the minimum size required to store the program code and the configuration record of the ZL38052 device. The ZLE38000 demonstration hardware uses the Macronix™ MX25L4006E 4 Mbit CMOS Serial Flash device.

Figure 24 - Flash Interface Circuit



4.4.1.1 Flash Selection

The ZL38052 Boot ROM is designed to work with a wide variety of Flash devices. There are numerous Flash devices that the ZL38052 Boot ROM can recognize and program without host intervention other than a command to initialize the Flash. Other unrecognized devices may be utilized if they conform to characteristics of known devices and the host informs the ZL38052 Boot ROM of their type and size.

The ZL38052 identifies Flash devices (with a single binary image) with the ZL38052 boot ROM auto sensing the Flash type that complies with JEDEC *Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices.* The ZL38052 utilizes the *Serial Flash Discoverable Parameters* JEDEC standard JESD216B and the *Common Flash Interface* JESD68.01 JEDEC standard. The ZL38052 can identify devices by their JEDEC standard JEP106-K *Standard Manufacturer's Identification Code*.

A list of Flash devices that are identifiable by the ZL38052 Boot ROM are shown in Table 3. The size of these devices are all 2 Mbit or 4 Mbit, the Boot ROM will also recognize the size of 8 Mbit parts that are Type 1 or Type 2 devices (as defined in Table 4).