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## Features

### Inputs/Outputs

- Accepts differential or single-ended input
  - LVPECL, LVDS, CML, HCSL, LVCMOS
- Four precision LVPECL outputs
- Operating frequency up to 750 MHz

### Power

- Option for 2.5 V or 3.3 V power supply
- Core current consumption of 62 mA
- On-chip Low Drop Out (LDO) Regulator for superior power supply noise rejection

### Performance

- Ultra low additive jitter of 39 fs RMS

### Ordering Information

ZL40202LDG1	16 Pin QFN	Trays
ZL40202LDF1	16 Pin QFN	Tape and Reel

Matte Tin

Package size: 3 x 3 mm

-40°C to +85°C

## Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- Wireless communications
- High performance microprocessor clock distribution

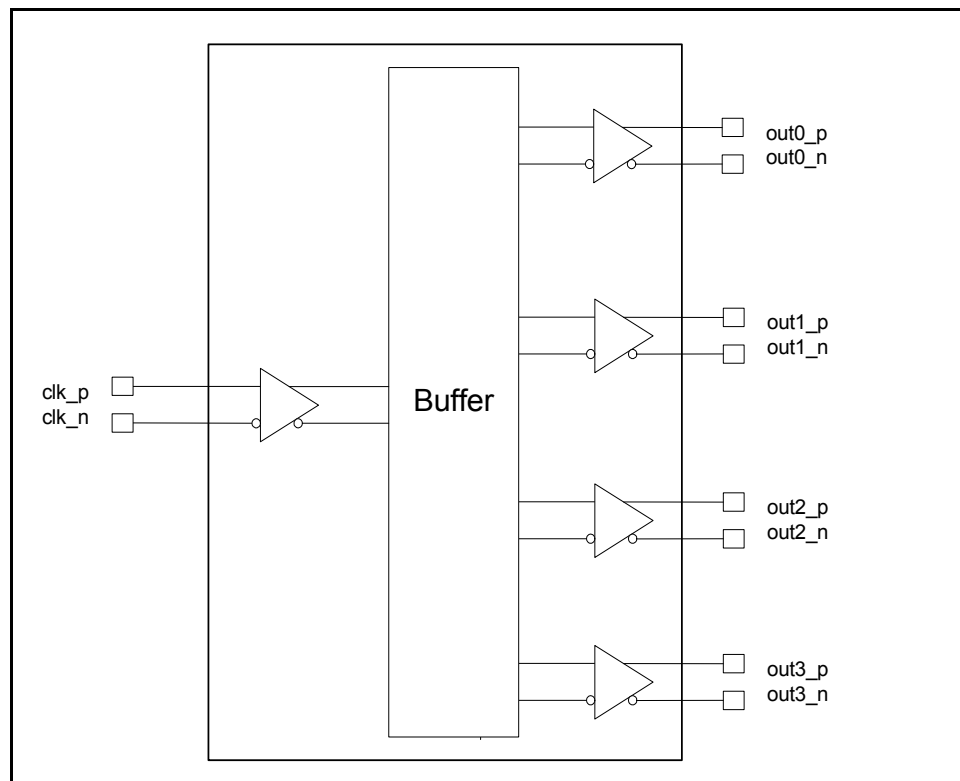


Figure 1 - Functional Block Diagram

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## Table of Contents

<b>Features</b> .....	<b>1</b>
<b>Applications</b> .....	<b>1</b>
<b>1.0 Package Description</b> .....	<b>4</b>
<b>2.0 Pin Description</b> .....	<b>4</b>
<b>3.0 Functional Description</b> .....	<b>5</b>
3.1 Clock Inputs .....	5
3.2 Clock Outputs .....	10
3.3 Device Additive Jitter .....	14
3.4 Power Supply .....	15
3.4.1 Sensitivity to power supply noise .....	15
3.4.2 Power supply filtering .....	15
3.4.3 PCB layout considerations .....	15
<b>4.0 AC and DC Electrical Characteristics</b> .....	<b>16</b>
<b>5.0 Performance Characterization</b> .....	<b>19</b>
<b>6.0 Typical Behavior</b> .....	<b>20</b>
<b>7.0 Package Thermal Characteristics</b> .....	<b>22</b>
<b>8.0 Mechanical Drawing</b> .....	<b>23</b>

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## List of Figures

Figure 1 - Functional Block Diagram	1
Figure 2 - Pin Connections	4
Figure 3 - LVPECL Input DC Coupled Thevenin Equivalent	5
Figure 4 - LVPECL Input DC Coupled Parallel Termination	6
Figure 5 - LVPECL Input AC Coupled Termination	6
Figure 6 - LVDS Input DC Coupled	7
Figure 7 - LVDS Input AC Coupled	7
Figure 8 - CML Input AC Coupled	8
Figure 9 - HCSL Input AC Coupled	8
Figure 10 - CMOS Input DC Coupled Referenced to VDD/2	9
Figure 11 - CMOS Input DC Coupled Referenced to Ground	9
Figure 12 - Simplified Output Driver	10
Figure 13 - LVPECL Basic Output Termination	10
Figure 14 - LVPECL Parallel Output Termination	11
Figure 15 - LVPECL Parallel Thevenin-Equivalent Output Termination	11
Figure 16 - LVPECL AC Output Termination for Externally Terminated LVPECL Inputs	12
Figure 17 - LVPECL AC Output Termination for Internally Terminated LVPECL Inputs	12
Figure 18 - LVPECL AC Output Termination for CML Inputs	13
Figure 19 - Additive Jitter	14
Figure 20 - Decoupling Connections for Power Pins	15
Figure 21 - Differential Output Voltage Parameter	17
Figure 22 - Input To Output Timing	18

## Change Summary

Below are the changes from the November 2012 issue to the February 2013 issue:

Page	Item	Change
6	Figure 4	Changed text to indicate the circuit is not recommended for VDD_driver=2.5V.
6	Figure 5	Changed pull-up and pull-down resistors from 2kOhm to 100Ohm.

## 1.0 Package Description

The device is packaged in a 16 pin QFN

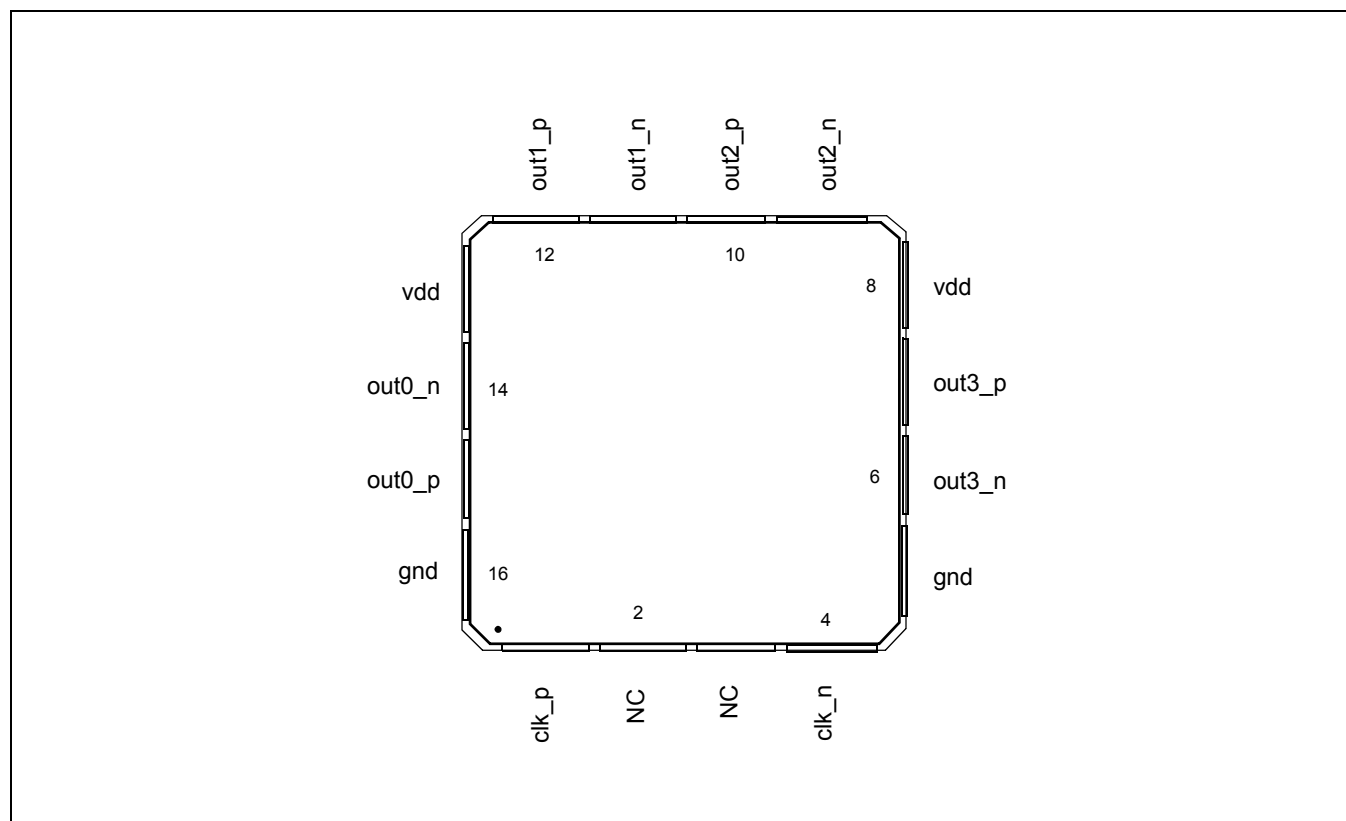


Figure 2 - Pin Connections

## 2.0 Pin Description

Pin #	Name	Description
1, 4	clk_p, clk_n,	<b>Differential Input (Analog Input).</b> Differential (or singled ended) input signals. For all input signal configuration see "Clock Inputs" on page 5
15,14, 12, 11, 10, 9, 7, 6	out0_p, out0_n out1_p, out1_n out2_p, out2_n out3_p, out3_n	<b>Differential Output (Analog Output).</b> Differential outputs.
8, 13	vdd	<b>Positive Supply Voltage.</b> 2.5 V <sub>DC</sub> or 3.3 V <sub>DC</sub> nominal.
5, 16	gnd	<b>Ground.</b> 0 V.
2, 3	NC	<b>No Connection.</b> Leave unconnected.

### 3.0 Functional Description

The ZL40202 is an LVPECL clock fanout buffer with four identical output clock drivers capable of operating at frequencies up to 750MHz.

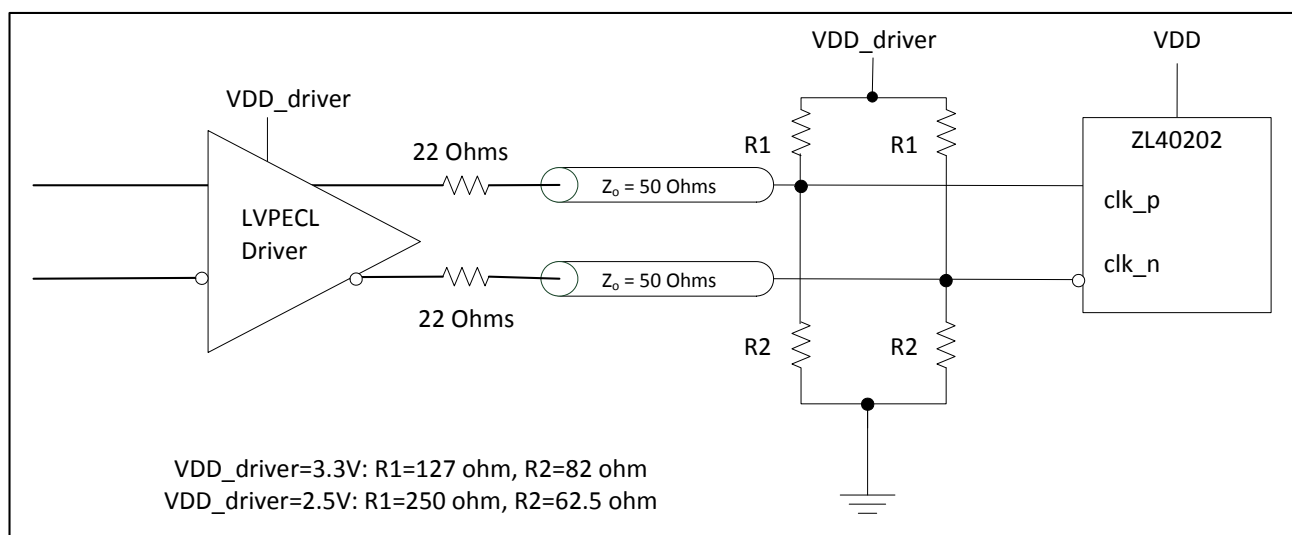
Inputs to the ZL40202 are externally terminated to allow use of precision termination components and to allow full flexibility of input termination. The ZL40202 can accept DC coupled LVPECL or LVDS and AC coupled LVPECL, LVDS, CML or HCSL input signals; single ended input signals can also be accepted. A pin compatible device with internal termination is also available.

The ZL40202 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V $\pm$ 5% or 3.3V $\pm$ 5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

The device block diagram is shown in Figure 1; its operation is described in the following sections.

### 3.1 Clock Inputs

The ZL40202 is adaptable to support different types of differential and single-ended input signals depending on the passive components used in the input termination. The application diagrams in the following figures allow the ZL40202 to accept LVPECL, LVDS, CML, HCSL and single-ended inputs.



**Figure 3 - LVPECL Input DC Coupled Thevenin Equivalent**

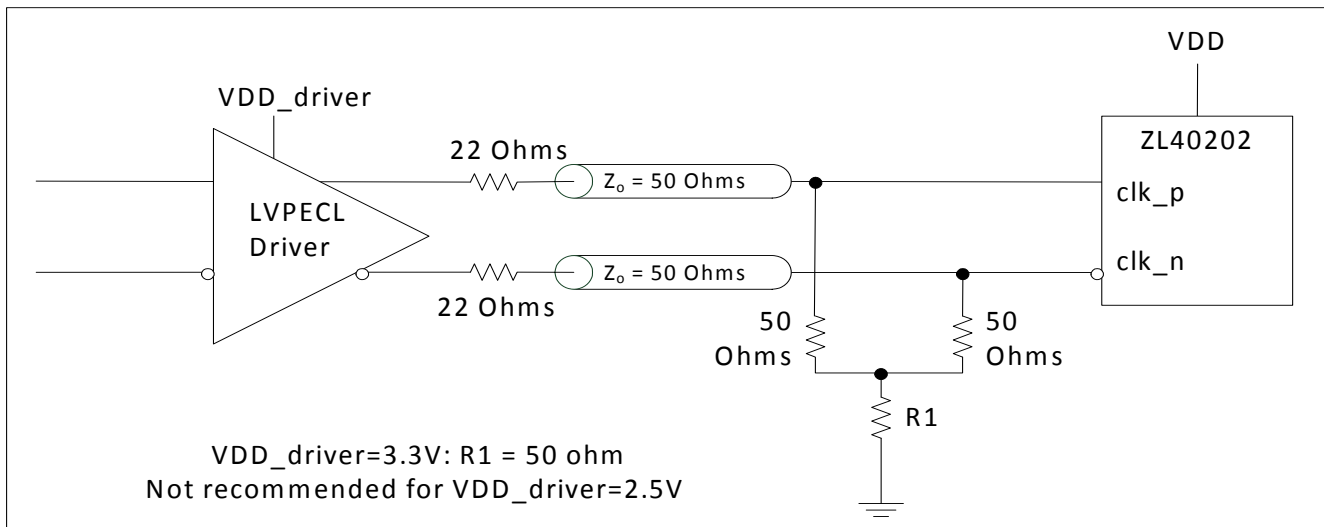


Figure 4 - LVPECL Input DC Coupled Parallel Termination

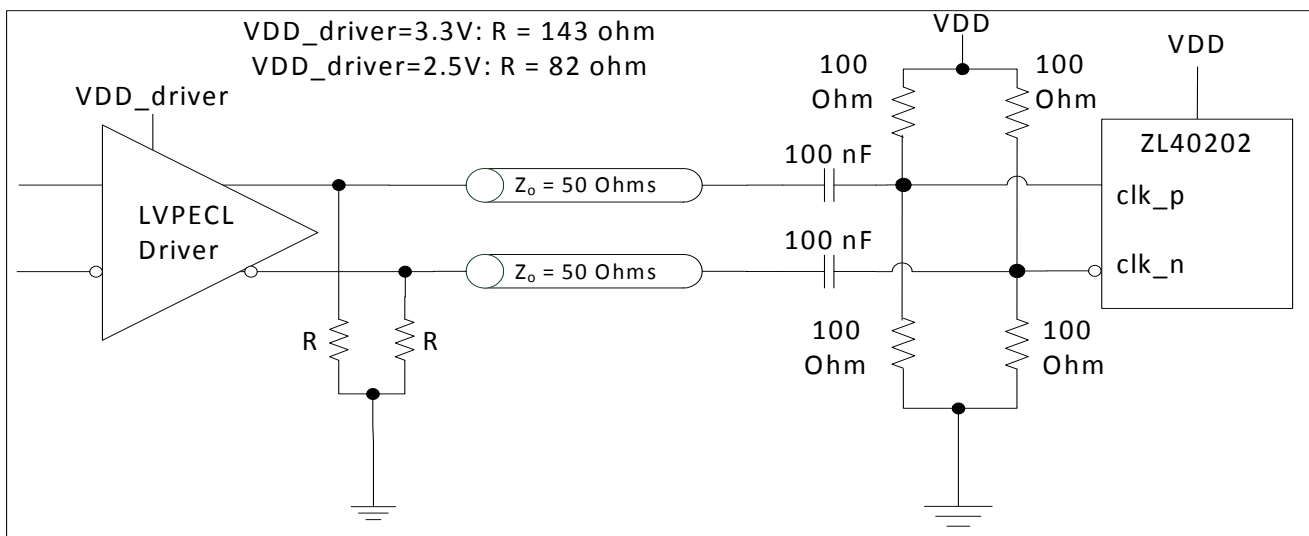


Figure 5 - LVPECL Input AC Coupled Termination



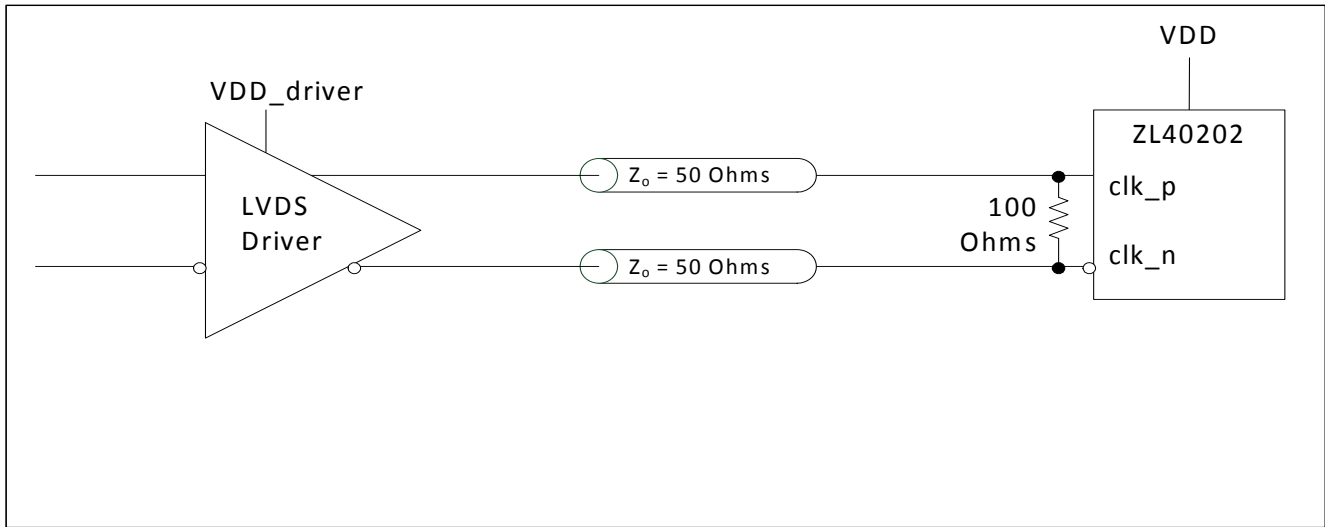


Figure 6 - LVDS Input DC Coupled

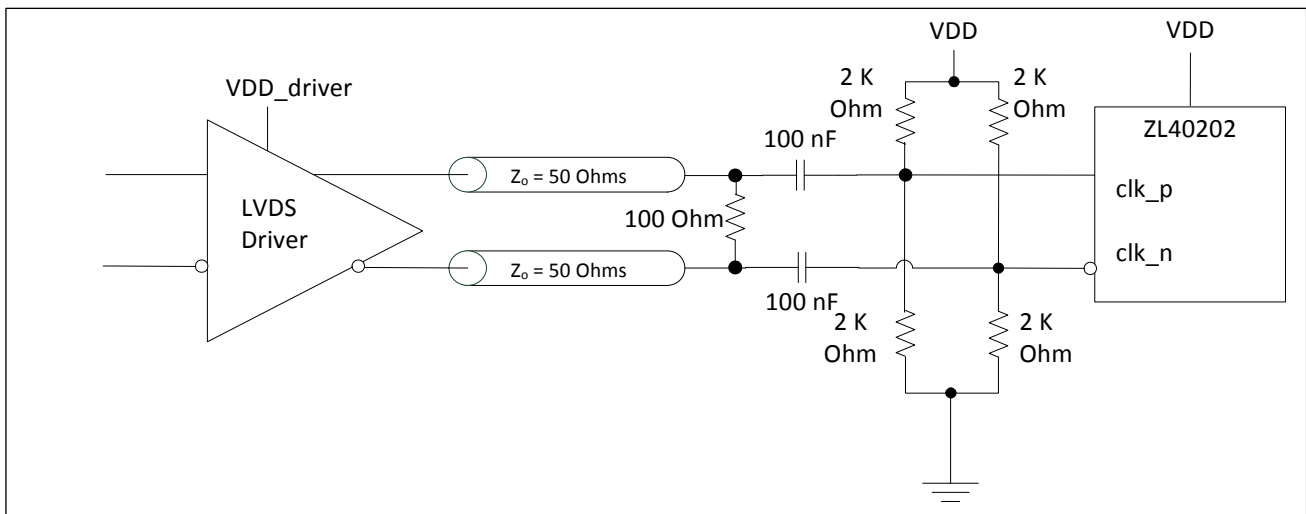


Figure 7 - LVDS Input AC Coupled

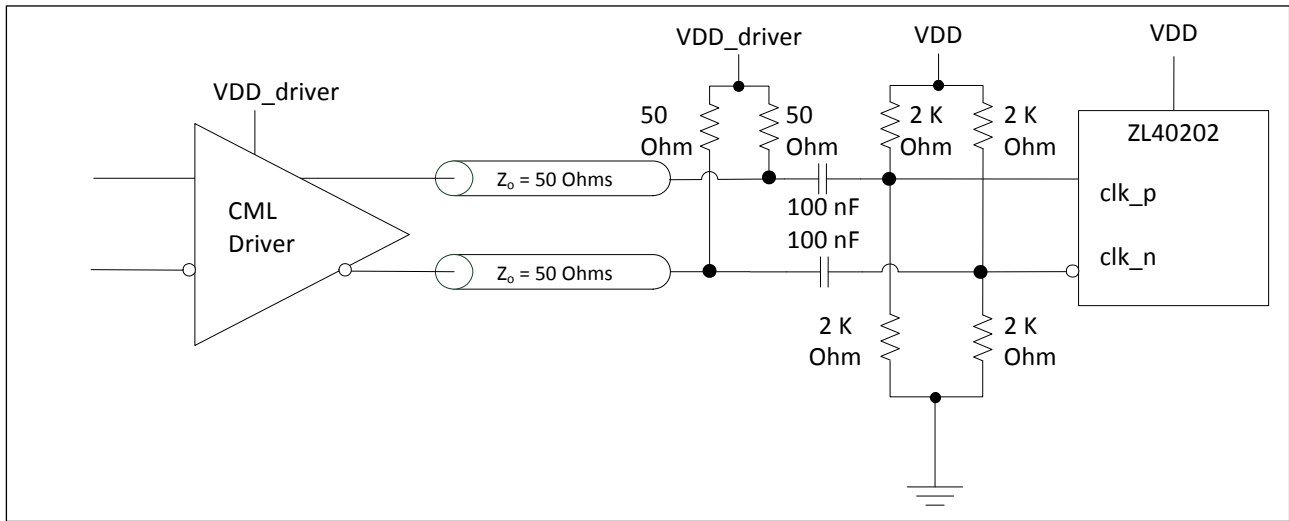


Figure 8 - CML Input AC Coupled

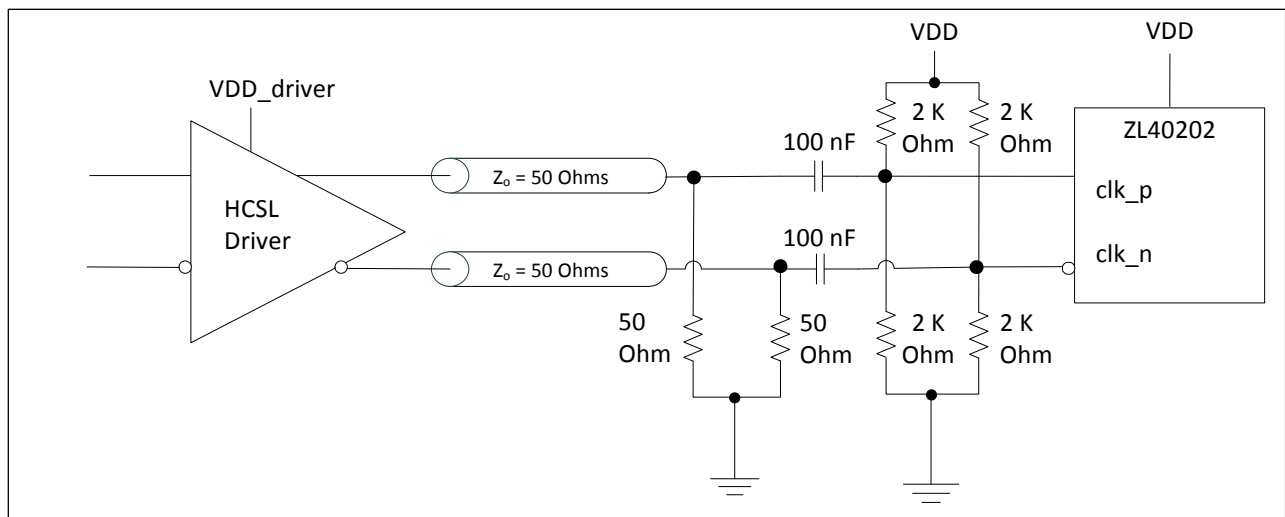
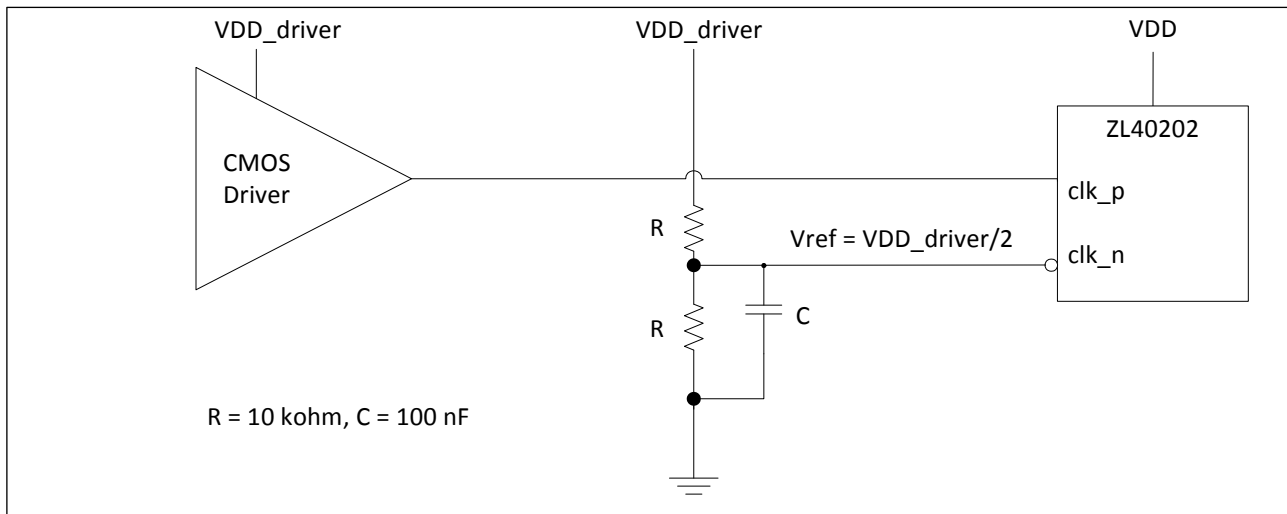
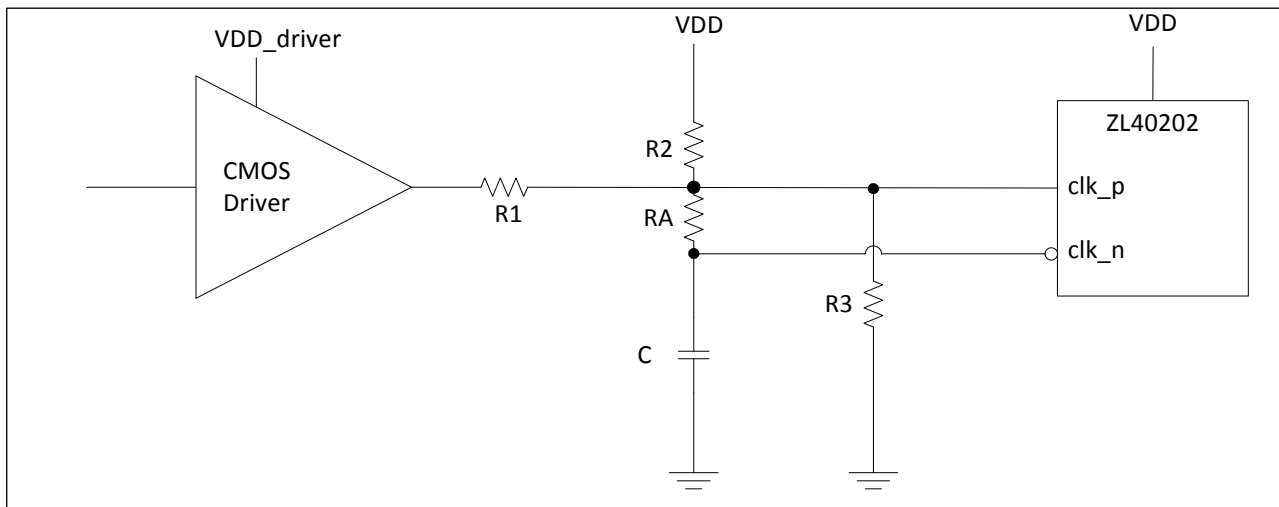


Figure 9 - HCSL Input AC Coupled



**Figure 10 - CMOS Input DC Coupled Referenced to VDD/2**



**Figure 11 - CMOS Input DC Coupled Referenced to Ground**

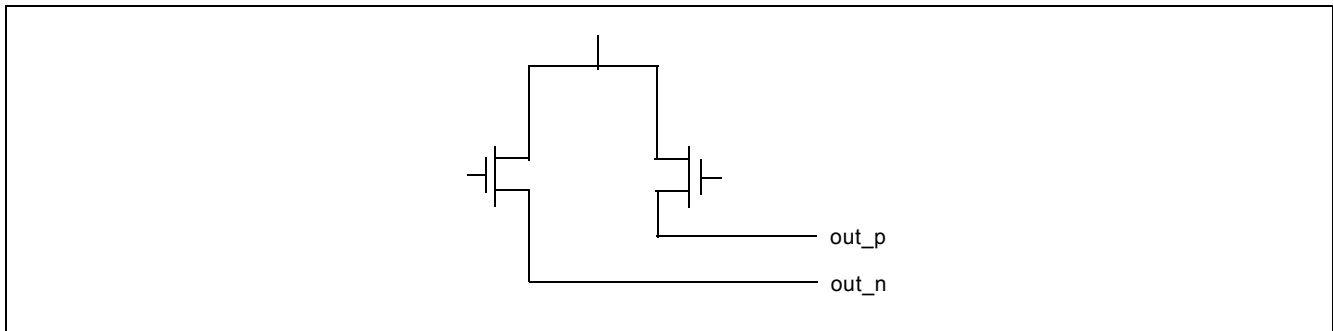
VDD_driver	R1 (k $\Omega$ )	R2 (k $\Omega$ )	R3 (k $\Omega$ )	RA (k $\Omega$ )	C (pF)
1.5	1.25	3.075	open	10	10
1.8	1	3.8	open	10	10
2.5	0.33	4.2	open	10	10
3.3	0.75	open	4.2	10	10

**Table 1 - Component Values for Single Ended Input Reference to Ground**

\* For frequencies below 100 MHz, increase C to avoid signal integrity issues.

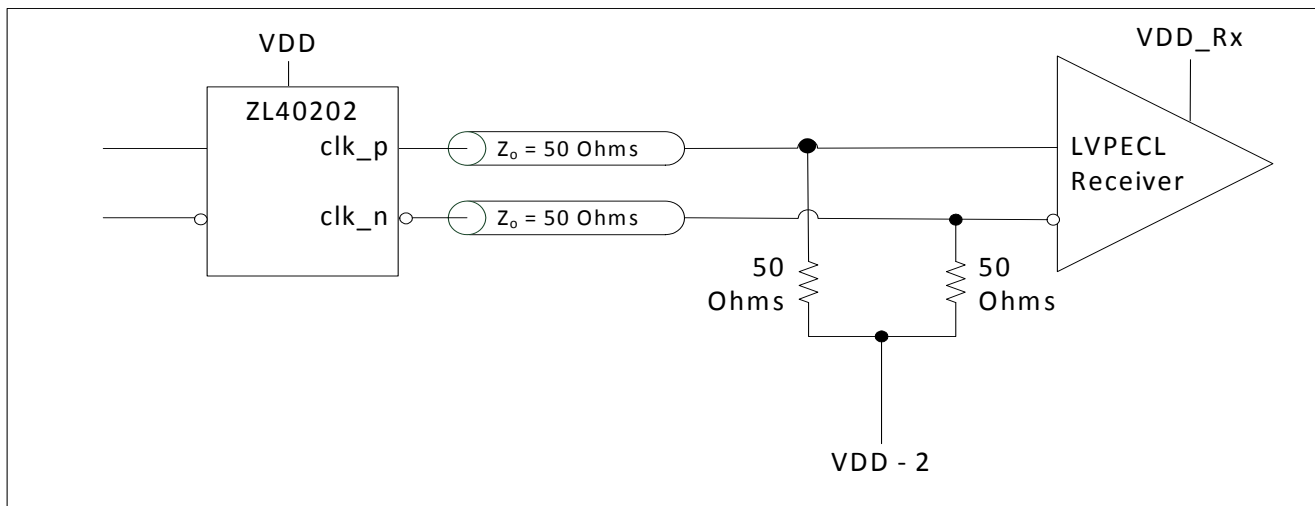
### 3.2 Clock Outputs

LVPECL has a very low output impedance and a differential signal swing between 1V and 1.6 V. A simplified diagram for the output stage is shown in Figure 12. The LVPECL to LVDS output termination is not shown since there is a separate device that has the same input and LVDS outputs.



**Figure 12 - Simplified Output Driver**

The methods to terminate the ZL40202 LVPECL drivers are shown in the following figures.



**Figure 13 - LVPECL Basic Output Termination**

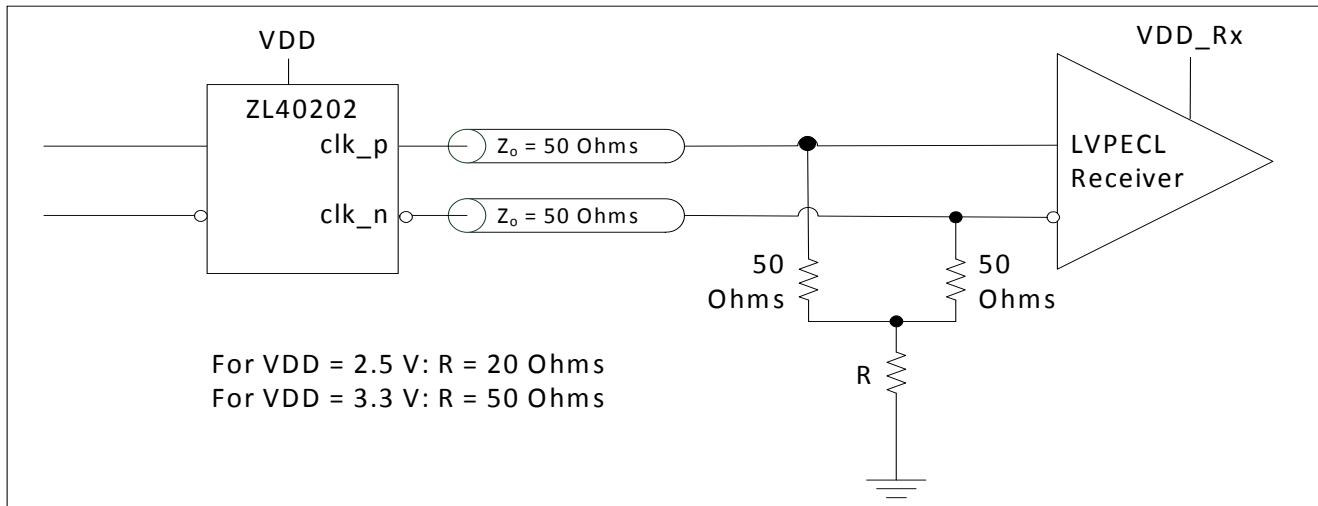


Figure 14 - LVPECL Parallel Output Termination

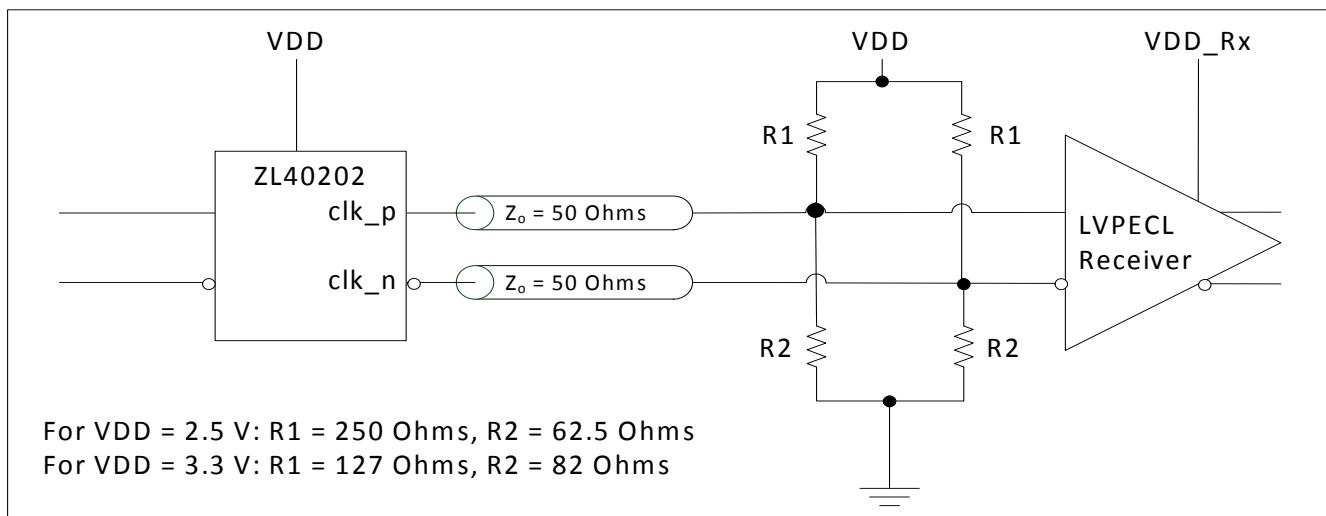


Figure 15 - LVPECL Parallel Thevenin-Equivalent Output Termination

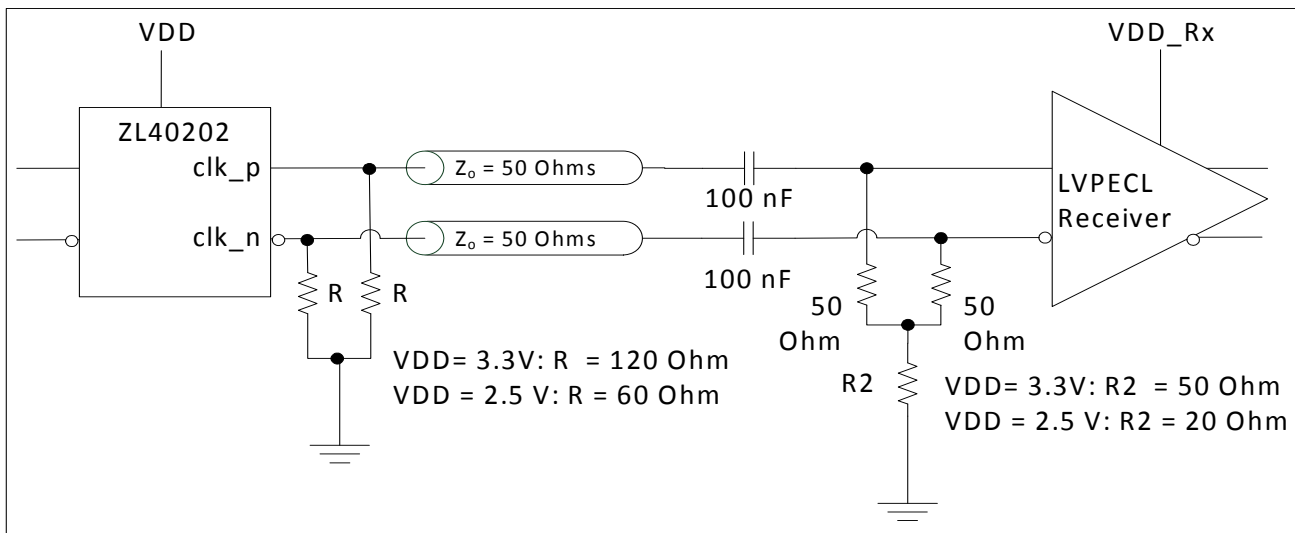


Figure 16 - LVPECL AC Output Termination for Externally Terminated LVPECL Inputs

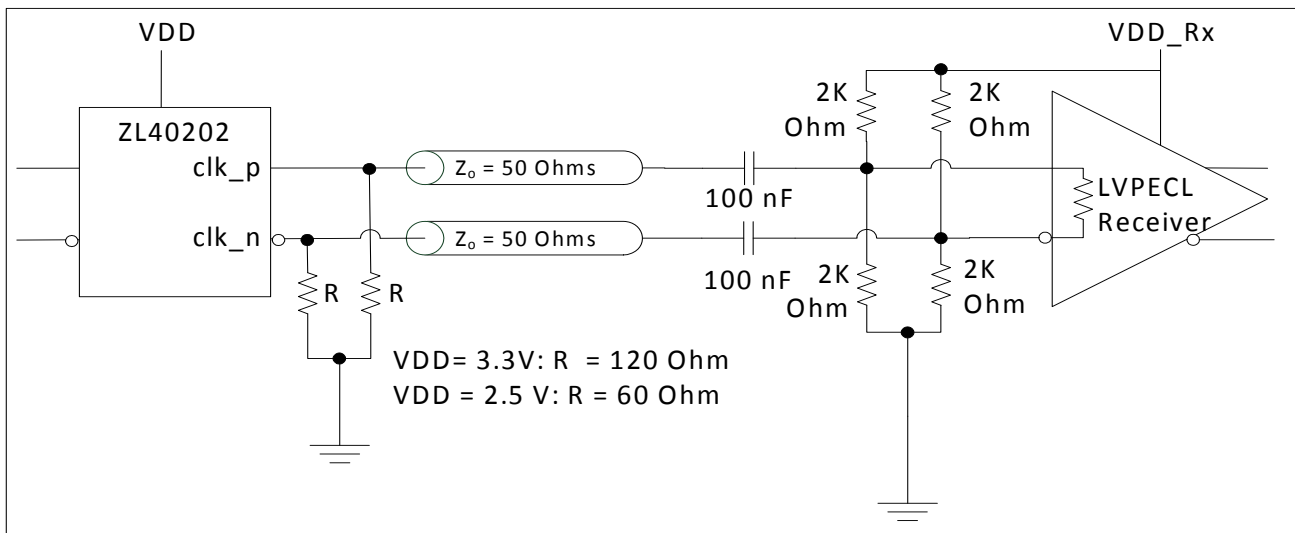
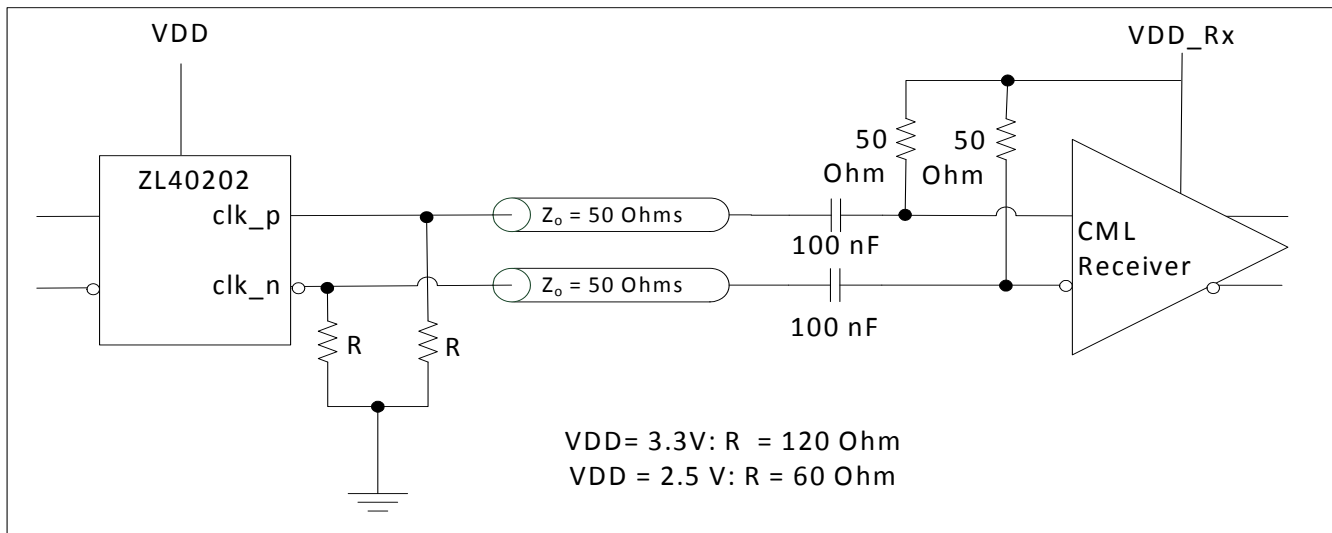


Figure 17 - LVPECL AC Output Termination for Internally Terminated LVPECL Inputs



**Figure 18 - LVPECL AC Output Termination for CML Inputs**

### 3.3 Device Additive Jitter

The ZL40202 clock fan out buffer is not intended to filter clock jitter. The jitter performance of this type of device is characterized by its additive jitter. Additive jitter is the jitter the device would add to a hypothetical jitter-free clock as it passes through the device. The additive jitter of the ZL40202 is random and as such it is not correlated to the jitter of the input clock signal.

The square of the resultant random RMS jitter at the output of the ZL40202 is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive jitter due to power supply noise. There may be additional deterministic jitter sources that are not shown in Figure 19.

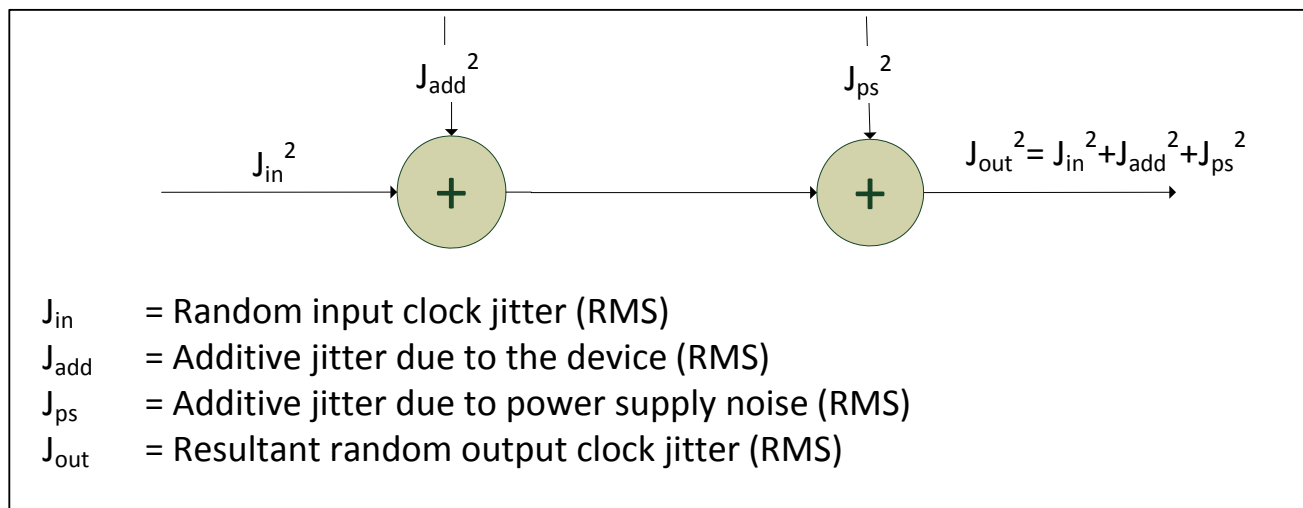


Figure 19 - Additive Jitter



### 3.4 Power Supply

This device operates with either a 2.5V supply or 3.3V supply.

#### 3.4.1 Sensitivity to power supply noise

Power supply noise from sources such as switching power supplies and high-power digital components such as FPGAs can induce additive jitter on clock buffer outputs. The ZL40202 is equipped with a low drop out (LDO) power regulator and on-chip bulk capacitors to minimize additive jitter due to power supply noise. The LDO regulator on the ZL40202 allows this device to have superior performance even in the presence of external noise sources. The on-chip regulation, recommended power supply filtering, and good PCB layout all work together to minimize the additive jitter from power supply noise.

The performance of these clock buffers in the presence of power supply noise is detailed in ZLAN-403, "Power Supply Rejection in Clock Buffers" which is available from Applications Engineering.

#### 3.4.2 Power supply filtering

For optimal jitter performance, the device should be isolated from the power planes connected to its power supply pins as shown in Figure 20.

- 10  $\mu\text{F}$  capacitors should be size 0603 or size 0805 X5R or X7R ceramic, 6.3 V minimum rating
- 0.1  $\mu\text{F}$  capacitors should be size 0402 X5R ceramic, 6.3 V minimum rating
- Capacitors should be placed next to the connected device power pins
- a 0.3 ohm resistor is recommended for the filter shown in Figure 20

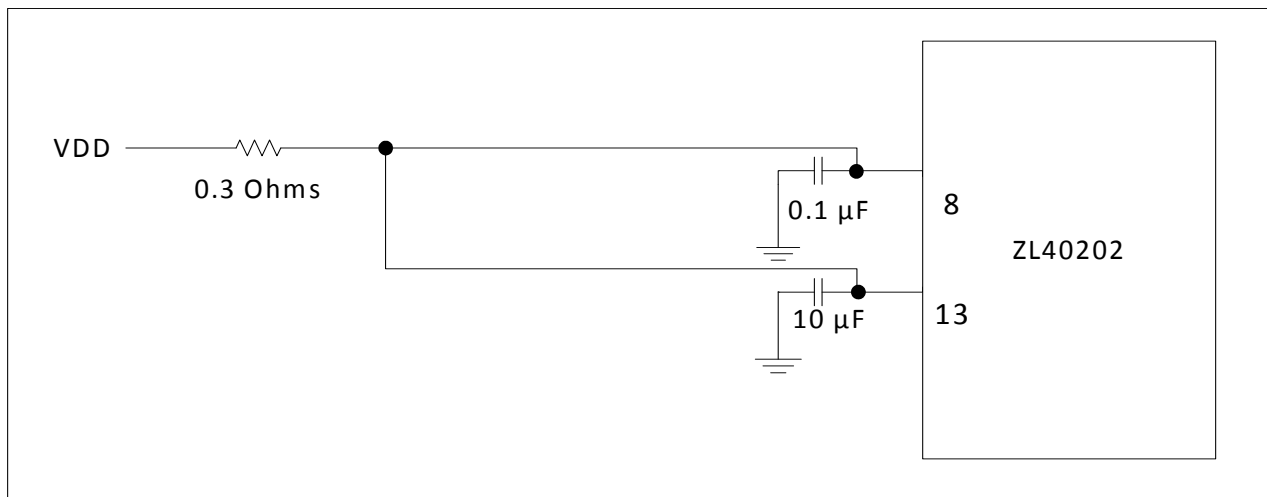


Figure 20 - Decoupling Connections for Power Pins

#### 3.4.3 PCB layout considerations

The power nets in Figure 20 can be implemented either as a plane island or routed power topology without changing the overall jitter performance of the device.

## 4.0 AC and DC Electrical Characteristics

### Absolute Maximum Ratings\*

	Parameter	Sym.	Min.	Max.	Units
1	Supply voltage	$V_{DD\_R}$	-0.5	4.6	V
2	Voltage on any digital pin	$V_{PIN}$	-0.5	$V_{DD}$	V
3	LVPECL output current	$I_{out}$		30	mA
4	Soldering temperature	T		260	°C
5	Storage temperature	$T_{ST}$	-55	125	°C
6	Junction temperature	$T_j$		125	°C
7	Voltage on input pin	$V_{input}$		$V_{DD}$	V
8	Input capacitance each pin	$C_p$		500	fF

\* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

\* Voltages are with respect to ground (GND) unless otherwise stated

### Recommended Operating Conditions\*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage 2.5 V mode	$V_{DD25}$	2.375	2.5	2.625	V
2	Supply voltage 3.3 V mode	$V_{DD33}$	3.135	3.3	3.465	V
3	Operating temperature	$T_A$	-40	25	85	°C

\* Voltages are with respect to ground (GND) unless otherwise stated

### DC Electrical Characteristics - Current Consumption

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply current LVPECL drivers - unloaded	$I_{dd\_unload}$		62		mA	Unloaded
2	Supply current LVPECL drivers - loaded (all outputs are active)	$I_{dd\_load}$		140		mA	Including power to $R_L = 50\Omega$

### DC Electrical Characteristics - Inputs and Outputs - for 3.3 V Supply

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Differential input common mode voltage	$V_{CM}$	1.1		2.0	V	
2	Differential input voltage difference	$V_{ID}$	0.25		1	V	
3	LVPECL output high voltage	$V_{OH}$	$V_{DD} - 1.40$			V	

**DC Electrical Characteristics - Inputs and Outputs - for 3.3 V Supply**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
4	LVPECL output low voltage	$V_{OL}$			$V_{DD}-1.62$	V	
5	LVPECL output differential voltage*	$V_{OD}$	0.5		0.9	V	

\* This parameter is measured from 125 MHz to 750 MHz

**DC Electrical Characteristics - Inputs and Outputs - for 2.5 V Supply**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Differential input common mode voltage	$V_{CM}$	1.1		1.6	V	
2	Differential input voltage difference	$V_{ID}$	0.25		1	V	
3	LVPECL output high voltage	$V_{OH}$	$V_{DD}-1.40$			V	
4	LVPECL output low voltage	$V_{OL}$			$V_{DD}-1.62$	V	
5	LVPECL output differential voltage*	$V_{OD}$	0.4		0.9	V	

\* This parameter is measured from 125 MHz to 750 MHz



**Figure 21 - Differential Output Voltage Parameter**

**AC Electrical Characteristics\* - Inputs and Outputs (see Figure 22) - for 2.5 and 3.3 V supplies.**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Maximum Operating Frequency	$1/t_p$			750	MHz	
2	Input to output clock propagation delay	$t_{pd}$	0	1	2	ns	
3	Output to output skew	$t_{out2out}$		50	100	ps	
4	Part to part output skew	$t_{part2part}$		80	300	ps	
5	Output clock Duty Cycle degradation	$t_{PWH}/t_{PWL}$	-2%	0%	2%	Duty Cycle	
6	LVPECL Output slew rate	$r_{sl}$	0.75	1.2		V/ns	

\* Supply voltage and operating temperature are as per Recommended Operating Conditions

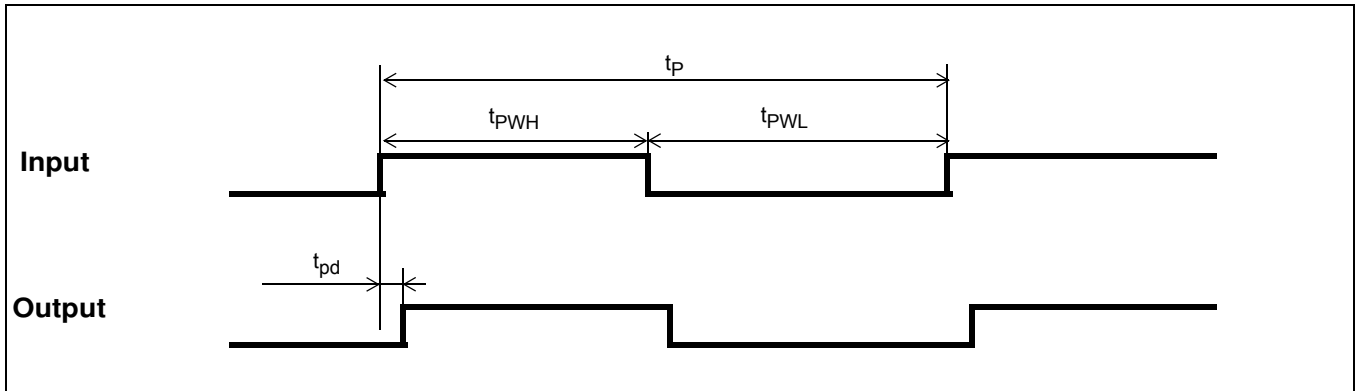


Figure 22 - Input To Output Timing

## 5.0 Performance Characterization

### Additive Jitter at 2.5 V\*

	Output Frequency (MHz)	Jitter Measurement Filter	Typical RMS (fs)	Notes
1	125	12 kHz - 20 MHz	112	
2	212.5	12 kHz - 20 MHz	80	
3	311.04	12 kHz - 20 MHz	70	
4	425	12 kHz - 20 MHz	65	
5	500	12 kHz - 20 MHz	56	
6	622.08	12 kHz - 20 MHz	46	
7	750	12 kHz - 20 MHz	44	

\*The values in this table were taken with an approximate input slew rate of 0.8 V/ns

### Additive Jitter at 3.3 V\*

	Output Frequency (MHz)	Jitter Measurement Filter	Typical RMS (fs)	Notes
1	125	12 kHz - 20 MHz	112	
2	212.5	12 kHz - 20 MHz	82	
3	311.04	12 kHz - 20 MHz	72	
4	425	12 kHz - 20 MHz	63	
5	500	12 kHz - 20 MHz	52	
6	622.08	12 kHz - 20 MHz	43	
7	750	12 kHz - 20 MHz	39	

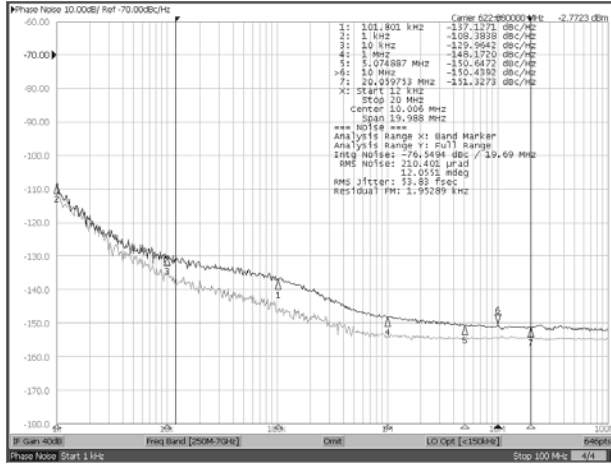
\*The values in this table were taken with an approximate input slew rate of 0.8 V/ns

### Additive Jitter from a Power Supply Tone\*

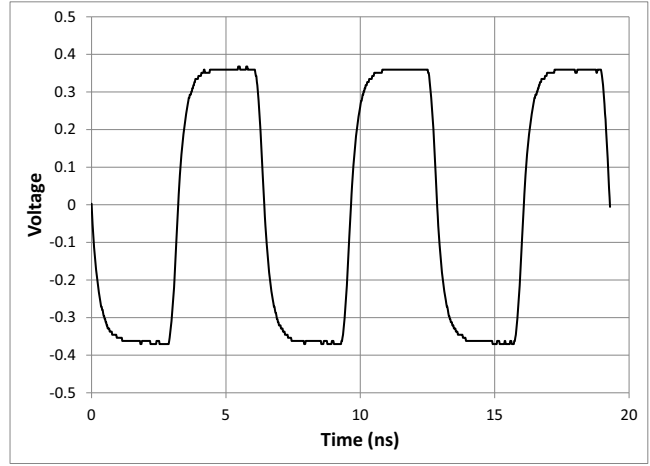
Carrier frequency	Parameter	Typical	Units	Notes
125MHz	25 mV at 100 kHz	159	fs RMS	
750MHz	25 mV at 100 kHz	82	fs RMS	

\* The values in this table are the additive periodic jitter caused by an interfering tone typically caused by a switching power supply. For this test, measurements were taken over the full temperature and voltage range for  $V_{DD} = 3.3$  V. The magnitude of the interfering tone is measured at the DUT.

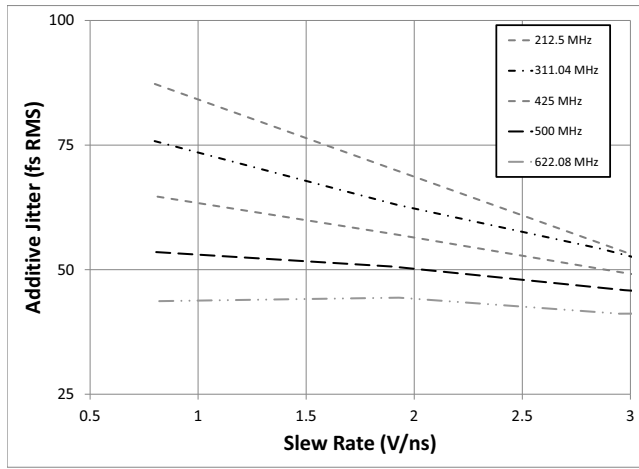
### 6.0 Typical Behavior



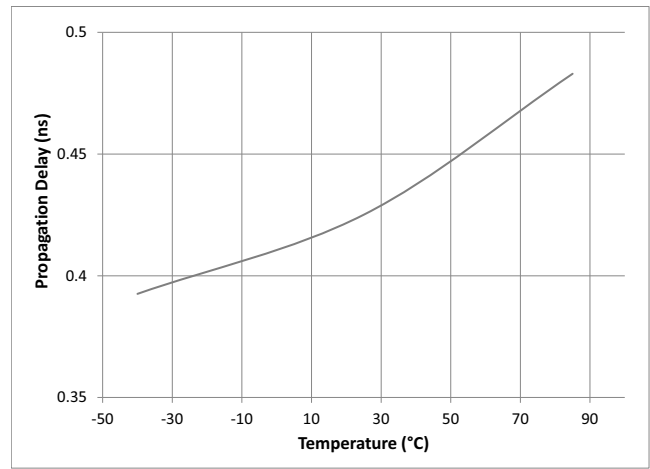
Typical Phase Noise at 622.08 MHz



Typical Waveform at 155.52 MHz

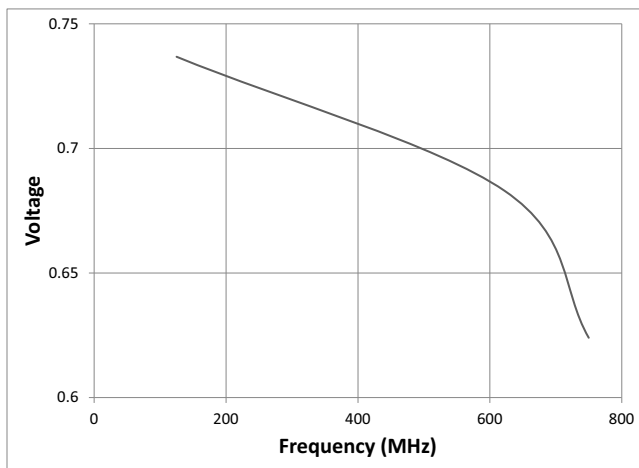


Input Slew Rate versus Additive Jitter

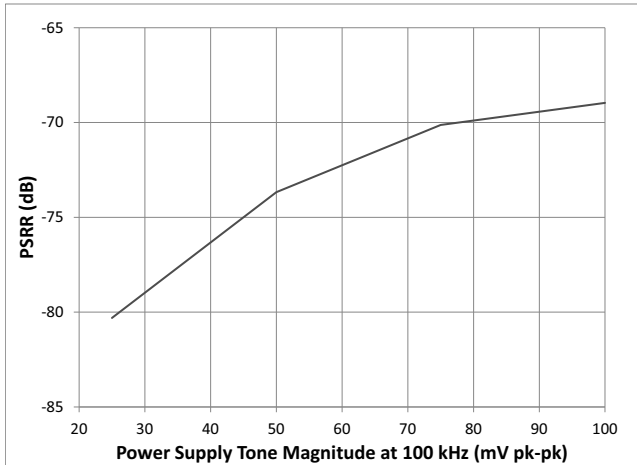


Propagation Delay versus Temperature

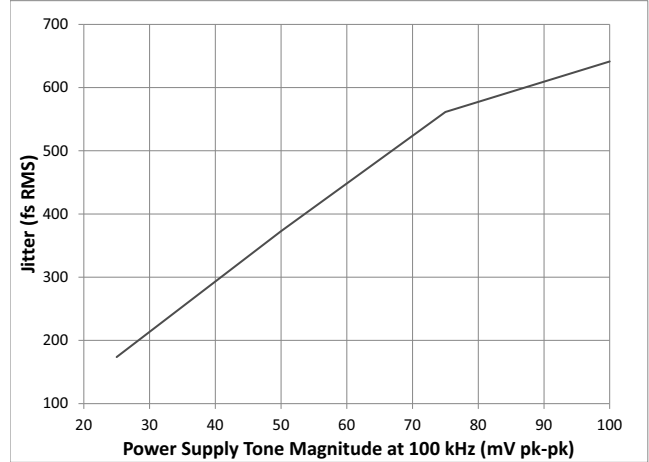
Note: This is for a single device. For more details see the characterization section.



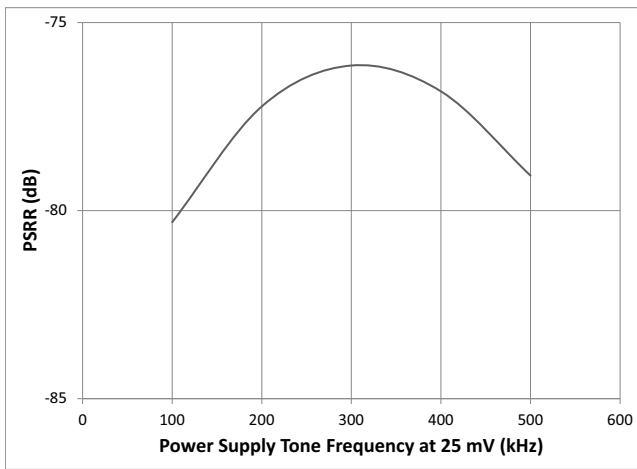
V<sub>OD</sub> versus Frequency



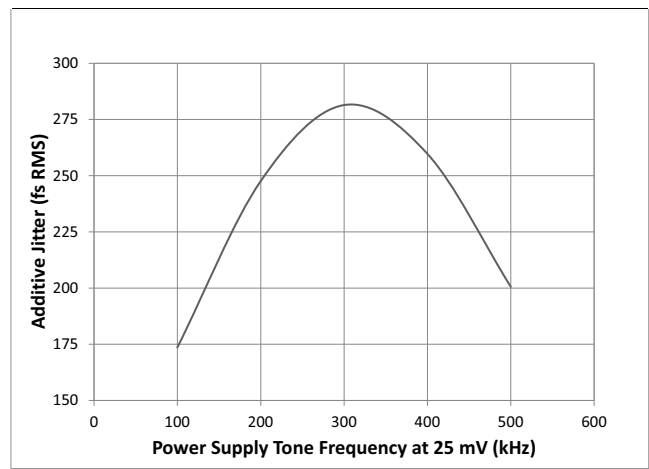
Power Supply Tone Magnitude versus PSRR (at 100 kHz) at 125 MHz



Power Supply Tone Magnitude versus Additive Jitter (at 100 kHz) at 125 MHz



Power Supply Tone Frequency (at 25 mV) versus PSRR at 125 MHz



Power Supply Tone Frequency (at 25 mV) versus Additive Jitter at 125 MHz

## 7.0 Package Thermal Characteristics

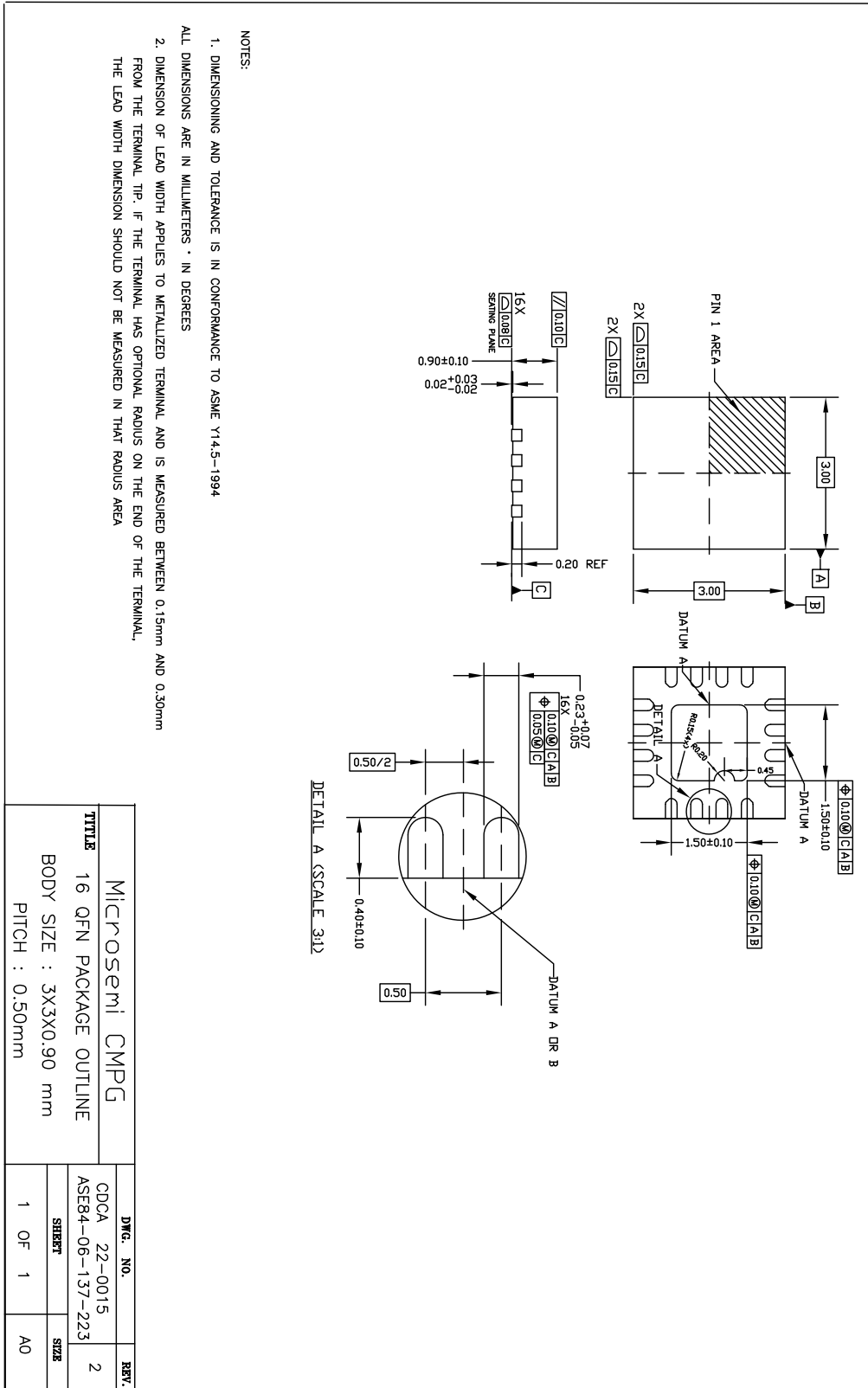
### Thermal Data

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	$\Theta_{JA}$	Still Air	67.9	$^{\circ}\text{C}/\text{W}$
		1 m/s	61.6	
		2 m/s	58.1	
Junction to Case Thermal Resistance	$\Theta_{JC}$	Still Air	44.1	$^{\circ}\text{C}/\text{W}$
Junction to Board Thermal Resistance	$\Theta_{JB}$	Still Air	23.2	$^{\circ}\text{C}/\text{W}$
Maximum Junction Temperature*	$T_{jmax}$		125	$^{\circ}\text{C}$
Maximum Ambient Temperature	$T_A$		85	$^{\circ}\text{C}$

\* Proper thermal management must be practiced to ensure that  $T_{jmax}$  is not exceeded.



### 8.0 Mechanical Drawing





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