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## Features

### Inputs/Outputs

- Accepts two differential or single-ended inputs
  - LVPECL, LVDS, CML, HCSL, LVCMOS
- On-chip input termination resistors and biasing for AC coupled inputs
- Eight precision LVPECL outputs
- Operating frequency up to 750 MHz

### Power

- Options for 2.5 V or 3.3 V power supply
- Core current consumption of 122 mA
- On-chip Low Drop Out (LDO) Regulator for superior power supply rejection

### Performance

- Ultra low additive jitter of 33 fs RMS

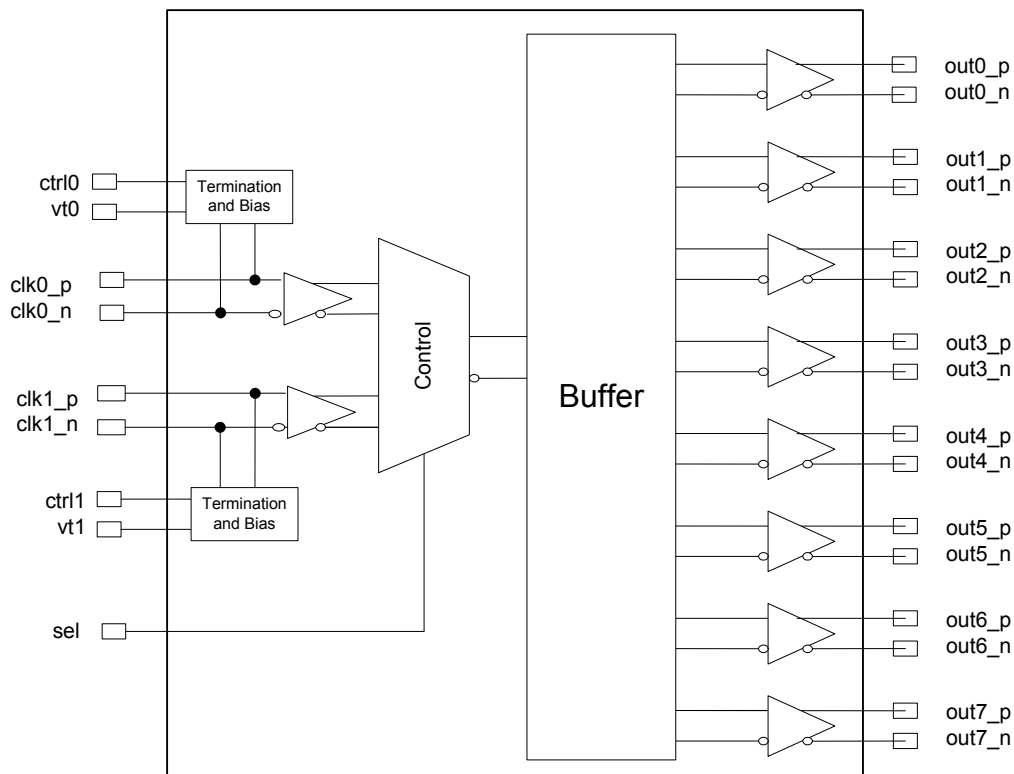
### Ordering Information

ZL40225LDG1	32 Pin QFN	Trays
ZL40225LDF1	32 Pin QFN	Tape and Reel

Matte Tin  
 Package size: 5 x 5 mm  
 -40°C to +85°C

## Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Redundant clock distribution
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- Wireless communications
- High performance microprocessor clock distribution



**Figure 1 - Functional Block Diagram**

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## Change Summary

Below are the changes from the November 2012 issue to the February 2013 issue:

Page	Item	Change
7	Figure 4	Changed text to indicate the circuit is not recommended for VDD_driver=2.5V.

### 1.0 Package Description

The device is packaged in a 32 pin QFN

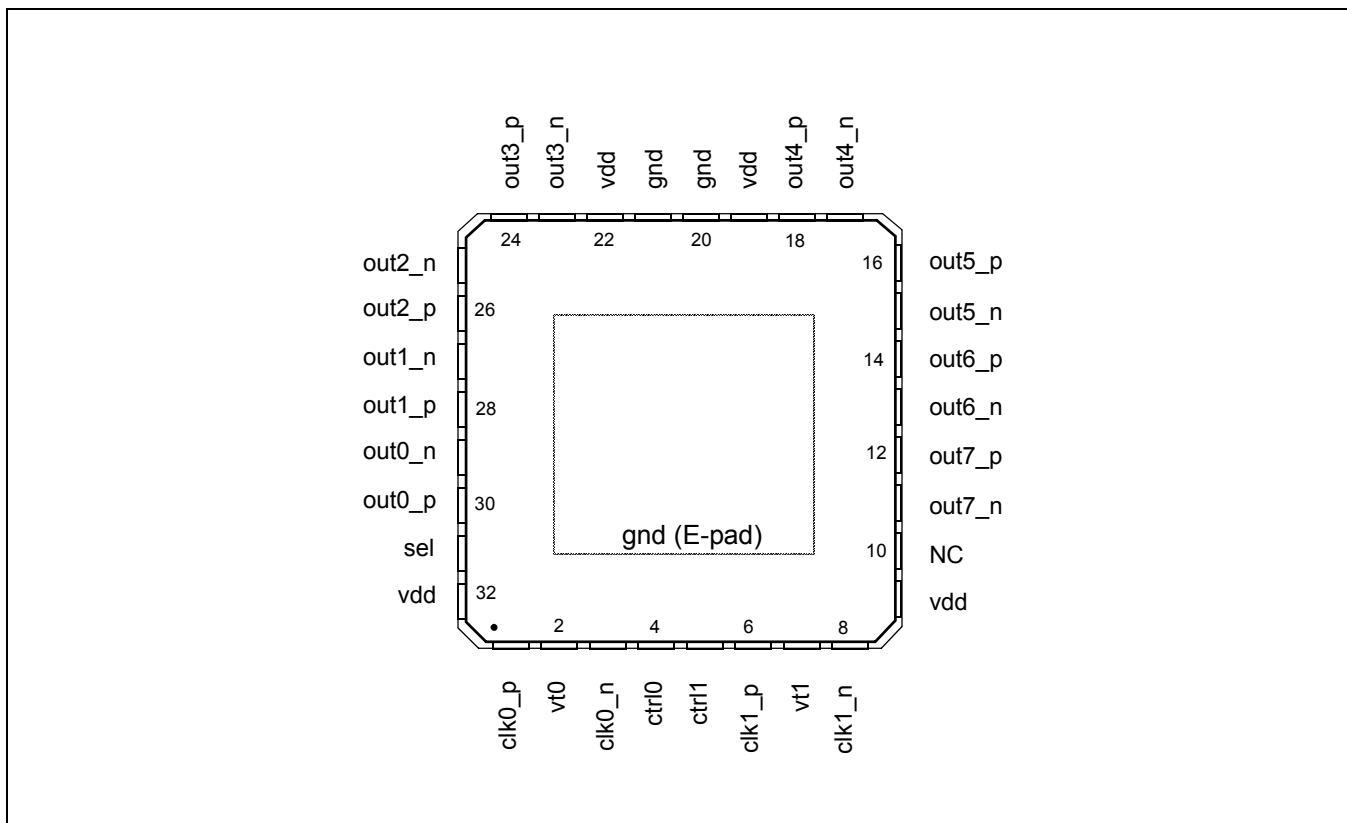


Figure 2 - Pin Connections

## 2.0 Pin Description

### Pin Description

Pin #	Name	Description
1,3, 6, 8	clk0_p, clk0_n, clk1_p, clk1_n	<b>Differential Input (Analog Input).</b> Differential input signals.
30, 29, 28, 27, 26, 25, 24, 23, 18, 17, 16, 15, 14, 13, 12, 11	out0_p, out0_n out1_p, out1_n out2_p, out2_n out3_p, out3_n out4_p, out4_n out5_p, out5_n out6_p, out6_n out7_p, out7_n	<b>Differential Output (Analog Output).</b> Differential outputs.
9, 19, 22, 32	vdd	<b>Positive Supply Voltage.</b> 2.5V <sub>DC</sub> or 3.3 V <sub>DC</sub> nominal.
20, 21	gnd	<b>Ground.</b> 0 V.
2, 7	vt0, vt1	<b>On-Chip Input Termination Node (Analog).</b> Center tap between internal 50 Ohm termination resistors. For a DC coupled LVPECL input connect this pin through a resistor to ground; 50 Ohms for 3.3V LVPECL or 20 Ohms for 2.5V LVPECL. For a DC coupled LVDS input or for an AC coupled differential input, leave this pin unconnected.
4, 5	ctrl0, ctrl1	<b>Digital Control for On-Chip Input Termination (Input).</b> Selects differential input mode; 0: DC coupled LVPECL or LVDS modes 1: AC coupled differential modes These pins are internally pulled down to GND.
10	NC	<b>No Connection.</b> Leave unconnected.
31	sel	<b>Input Select (Input).</b> Selects the reference input that is buffered; 0: clk0 1: clk1 This pin is internally pulled down to GND.

### 3.0 Functional Description

The ZL40225 is an LVPECL clock fan out buffer with two input and eight output clock drivers capable of operating at frequencies up to 750MHz.

The ZL40225 provides an internal input termination network for DC and AC coupled inputs; optional input biasing for AC coupled inputs is also provided. The ZL40225 can accept DC or AC coupled LVPECL and LVDS input signals, AC coupled CML or HCSL input signals, and single ended signals. A pin compatible device with external termination is also available.

The ZL40225 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V $\pm$ 5% or 3.3V $\pm$ 5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

The device block diagram is shown in Figure 1; its operation is described in the following sections.

#### 3.1 Clock Inputs

The device has a differential input equipped with two on-chip 50 Ohm termination resistors arranged in series with a center tap. The input can accept many differential and single-ended signals with AC or DC coupling as appropriate. A control pin is available to enable internal biasing for AC coupled inputs. A block diagram of the input stage is in Figure 3.

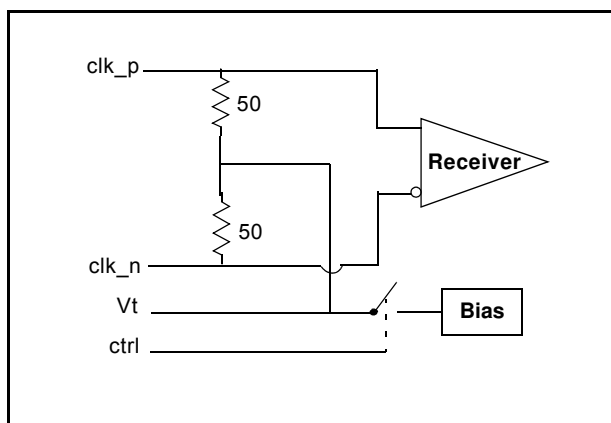


Figure 3 - Simplified Diagram of Input Stage

#### 3.2 Clock Input Selection

The select line chooses which input clock is routed to the outputs.

Sel	Active Input
0	clk0
1	clk1

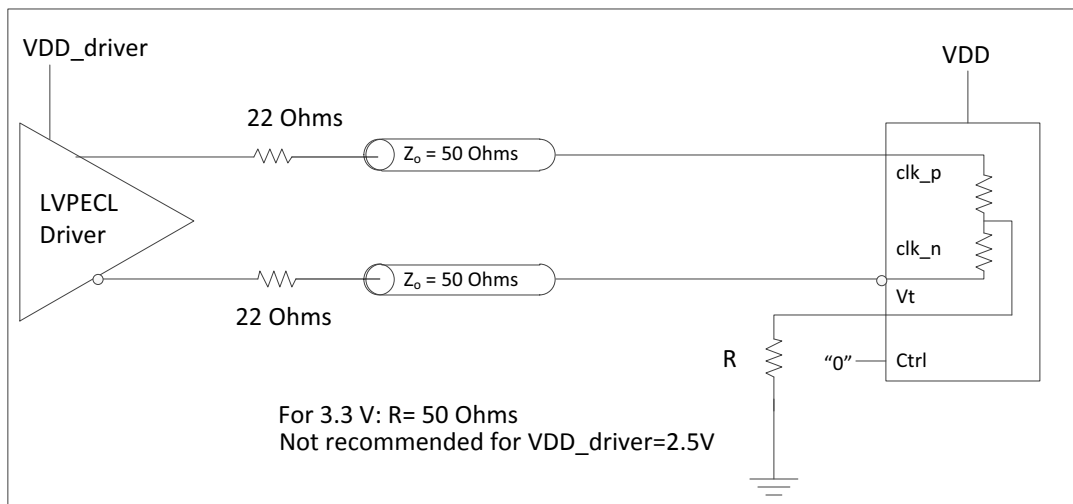
Table 1 - Input Selection



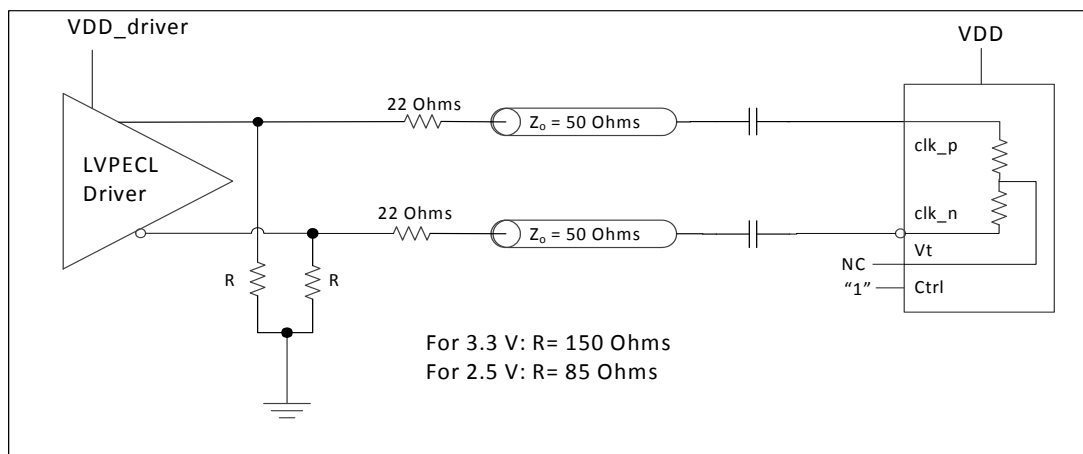
### 3.2.1 Clock Input Terminations

This following figures give the components values and configuration for the various circuits compatible with the input stage and the use of the  $V_t$  and  $ctrl$  pins in each case.

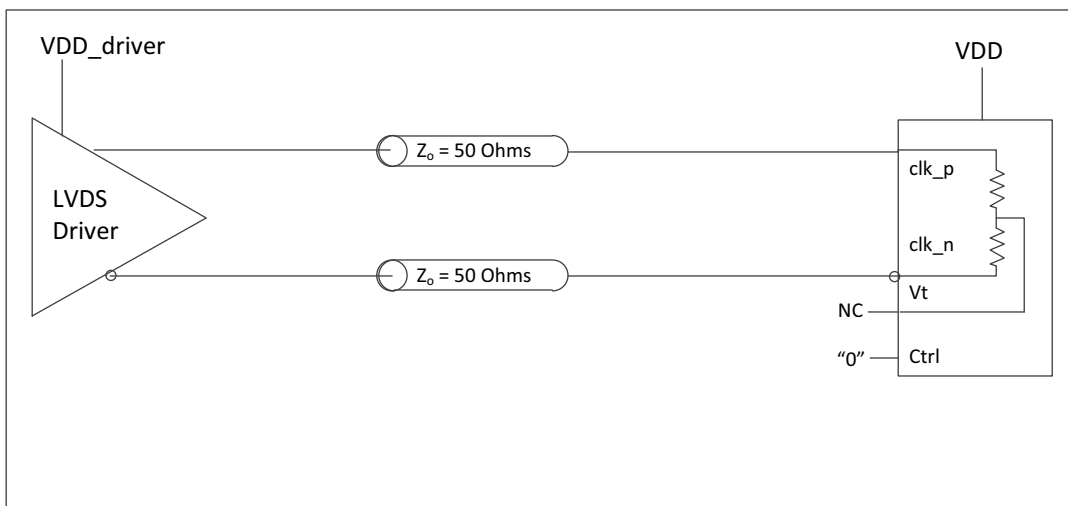
In the following diagrams were the  $ctrl$  pin is "1" and the  $V_t$  pin is not connected, the  $V_t$  pin can be instead connected to  $V_{DD}$  with a capacitor. A capacitor can also help in Figure 4 between  $V_t$  and  $V_{DD}$ . This capacitor will minimize the noise at the point between the two internal termination resistors and improve the overall performance of the device.



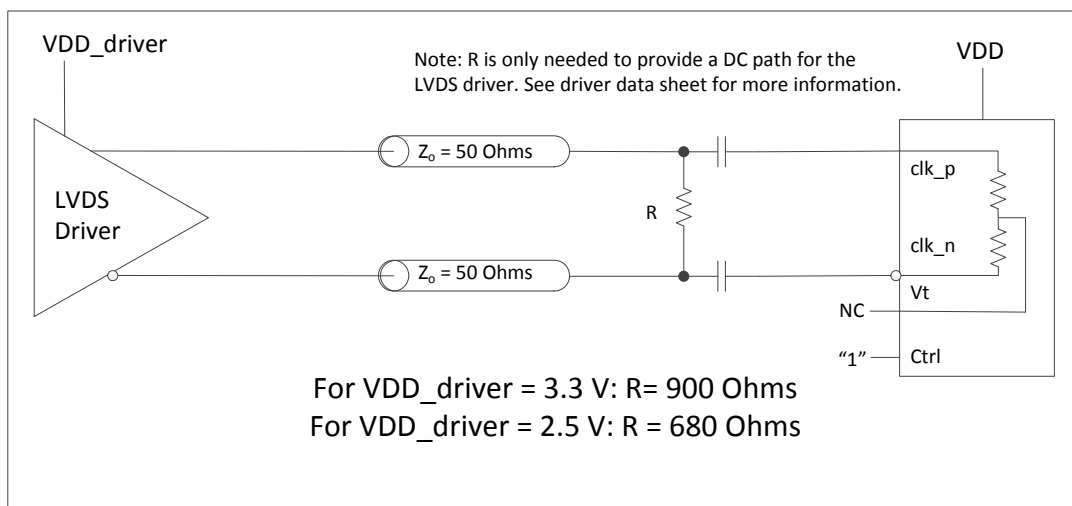
**Figure 4 - Clock Input - LVPECL - DC Coupled**



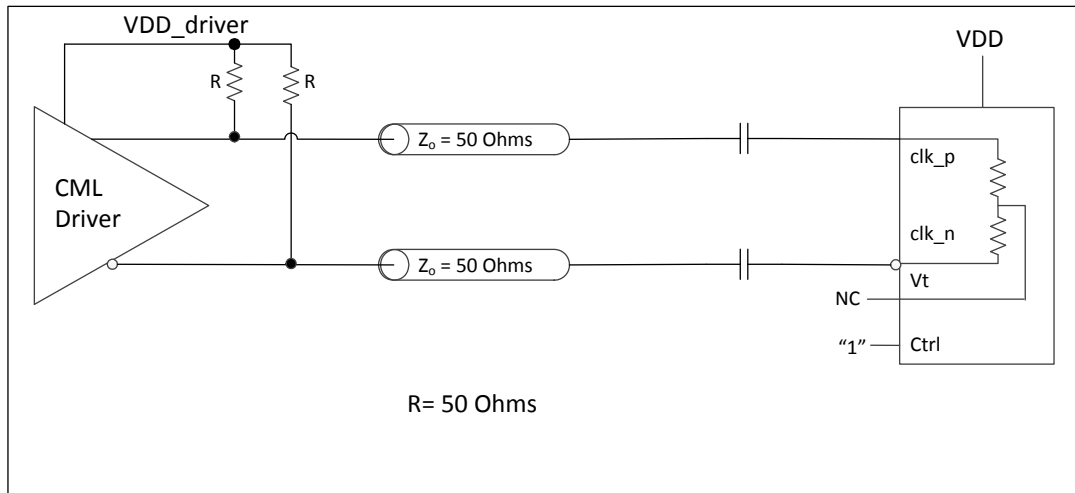
**Figure 5 - Clock Input - LVPECL - AC Coupled**



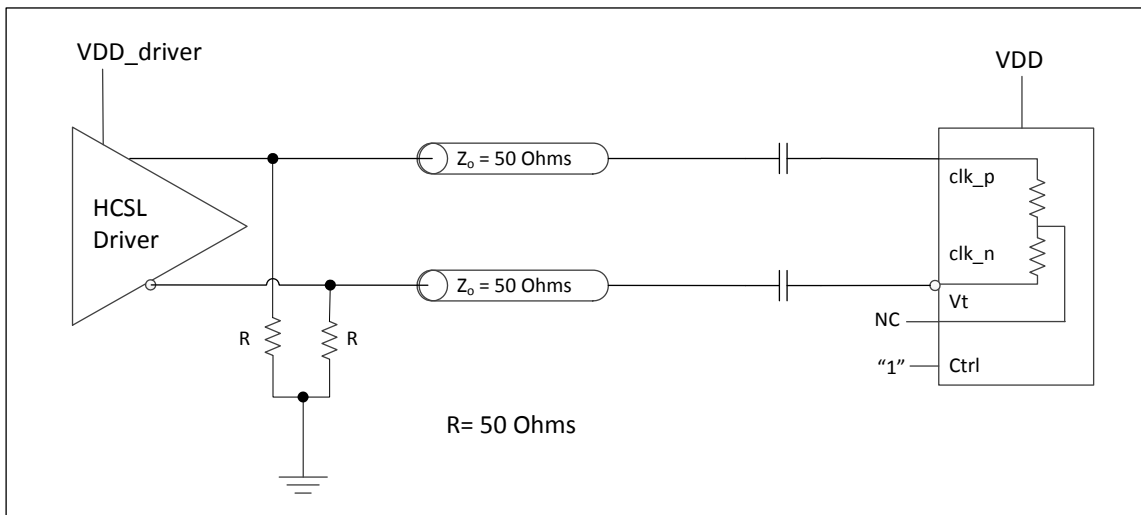
**Figure 6 - Clock Input - LVDS - DC Coupled**



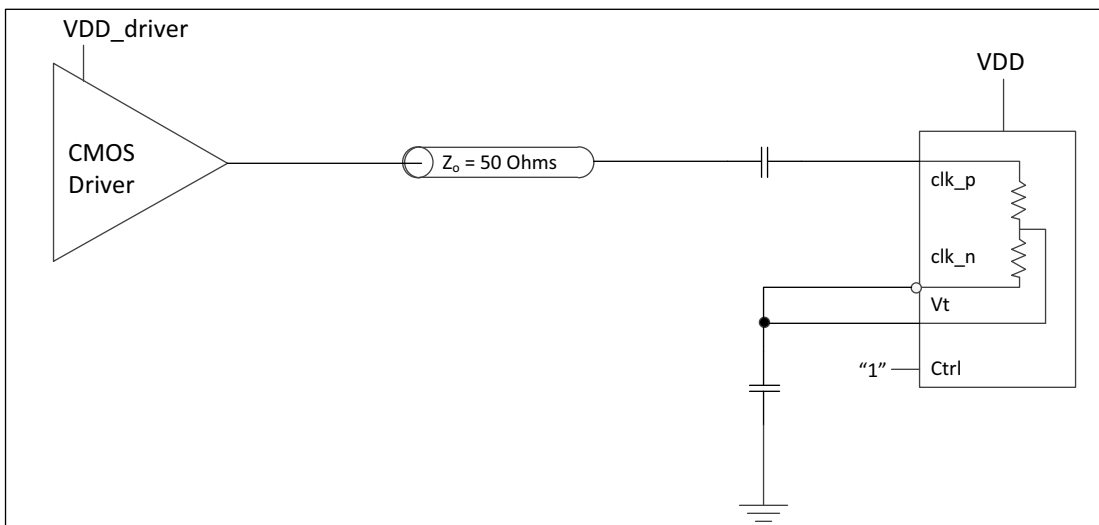
**Figure 7 - Clock Input - LVDS - AC Coupled**



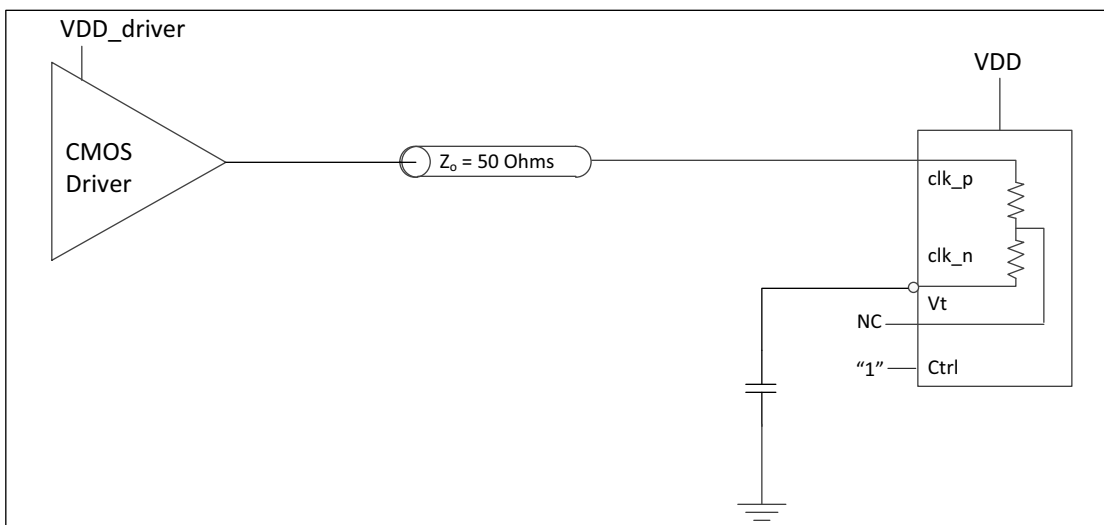
**Figure 8 - Clock Input - CML- AC Coupled**



**Figure 9 - Clock Input - HCSL- AC Coupled**



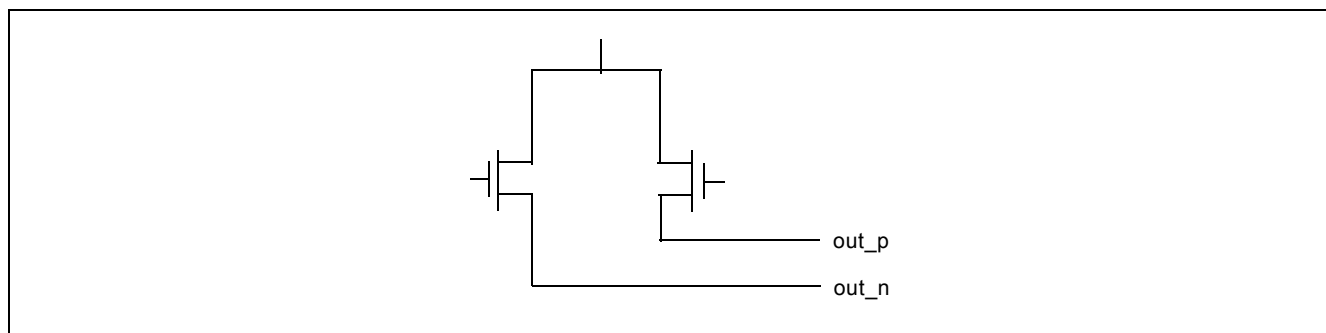
**Figure 10 - Clock Input - AC-coupled Single-Ended**



**Figure 11 - Clock Input - DC-coupled 3.3V CMOS**

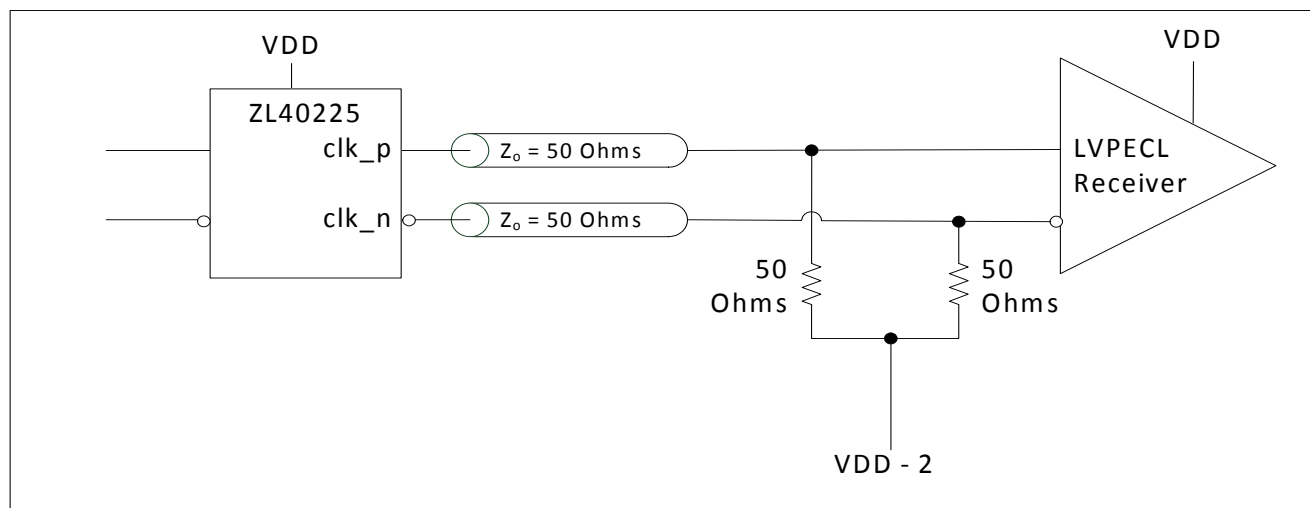
### 3.3 Clock Outputs

LVPECL has a very low output impedance and a differential signal swing between 1V and 1.6 V. A simplified diagram for the output stage is shown in Figure 12. The LVPECL to LVDS output termination is not shown since there is a different device with the same inputs and LVDS outputs.



**Figure 12 - Simplified Output Driver**

The methods to terminate the ZL40225 LVPECL drivers are shown in the following figures.



**Figure 13 - LVPECL Basic Output Termination**

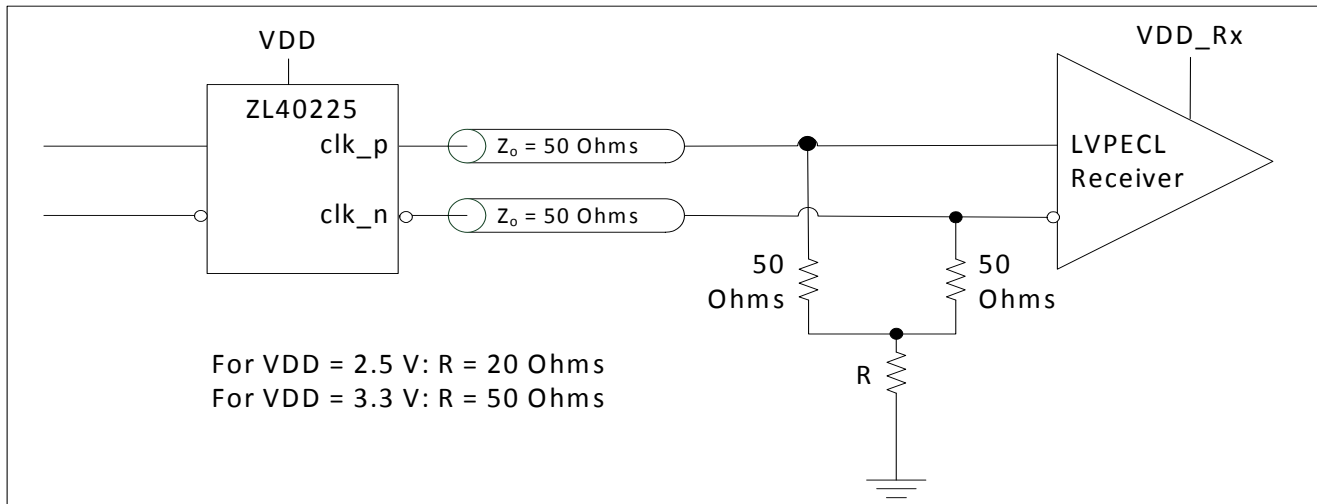


Figure 14 - LVPECL Parallel Output Termination

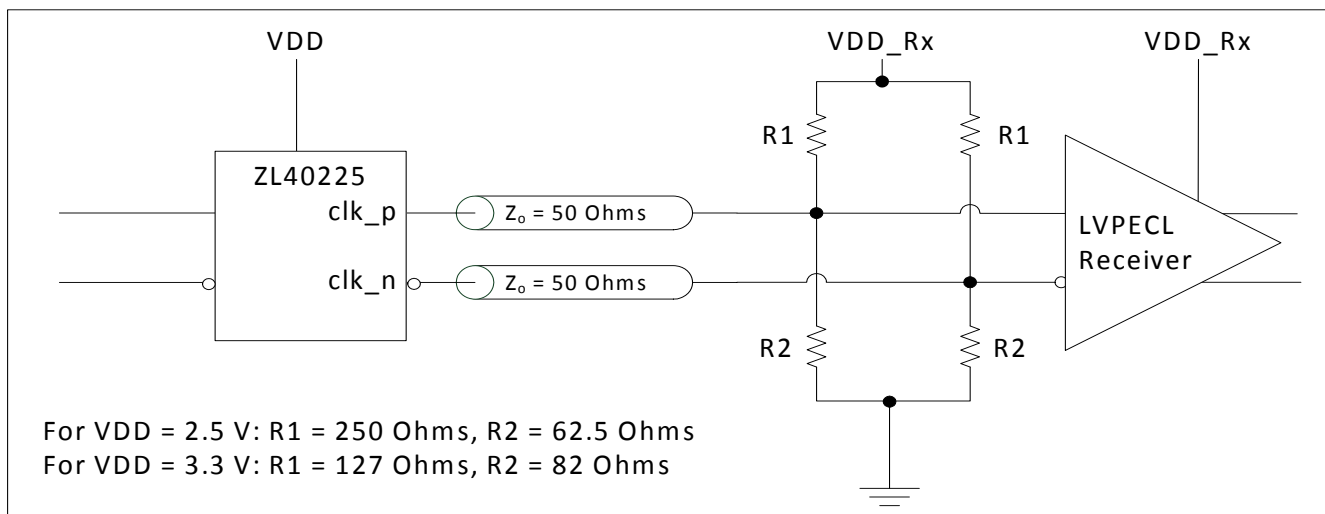


Figure 15 - LVPECL Parallel Thevenin-Equivalent Output Termination

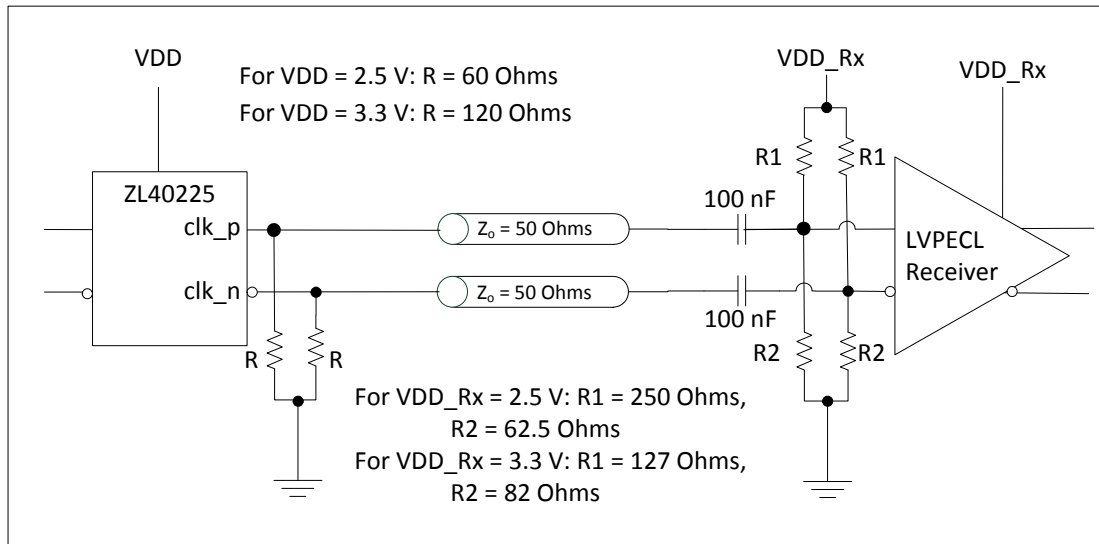


Figure 16 - LVPECL AC Output Termination

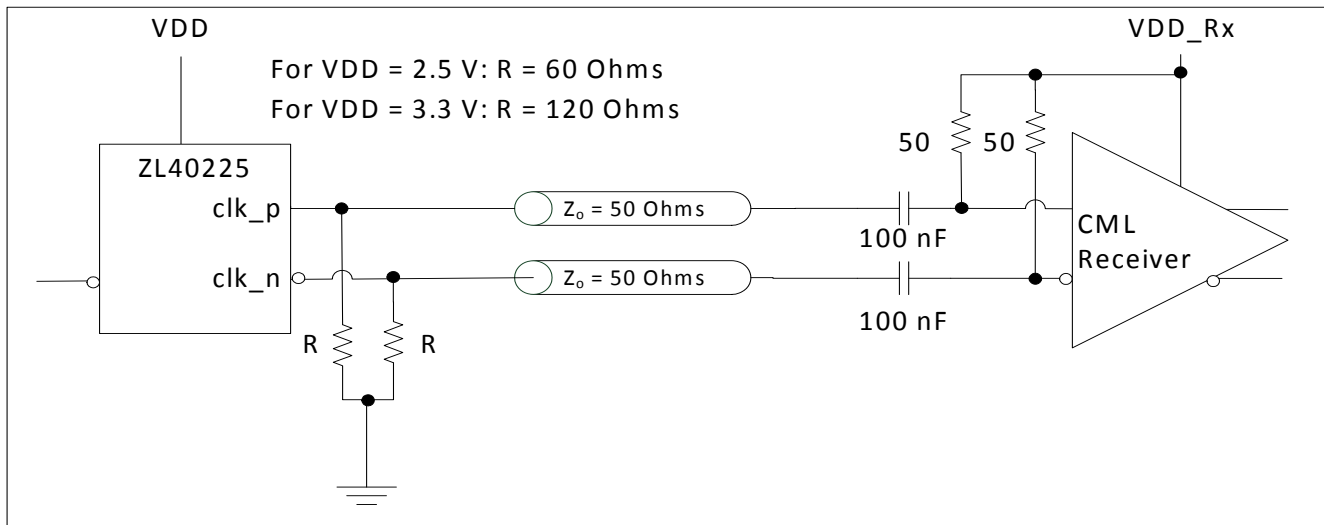


Figure 17 - LVPECL AC Output Termination for CML Inputs

### 3.4 Device Additive Jitter

The ZL40225 clock fanout buffer is not intended to filter clock jitter. The jitter performance of this type of device is characterized by its additive jitter. Additive jitter is the jitter the device would add to a hypothetical jitter-free clock as it passes through the device. The additive jitter of the ZL40225 is random and as such it is not correlated to the jitter of the input clock signal.

The square of the resultant random RMS jitter at the output of the ZL40225 is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive random jitter due to power supply noise. There may be additional deterministic jitter sources, but they are not shown in Figure 18.

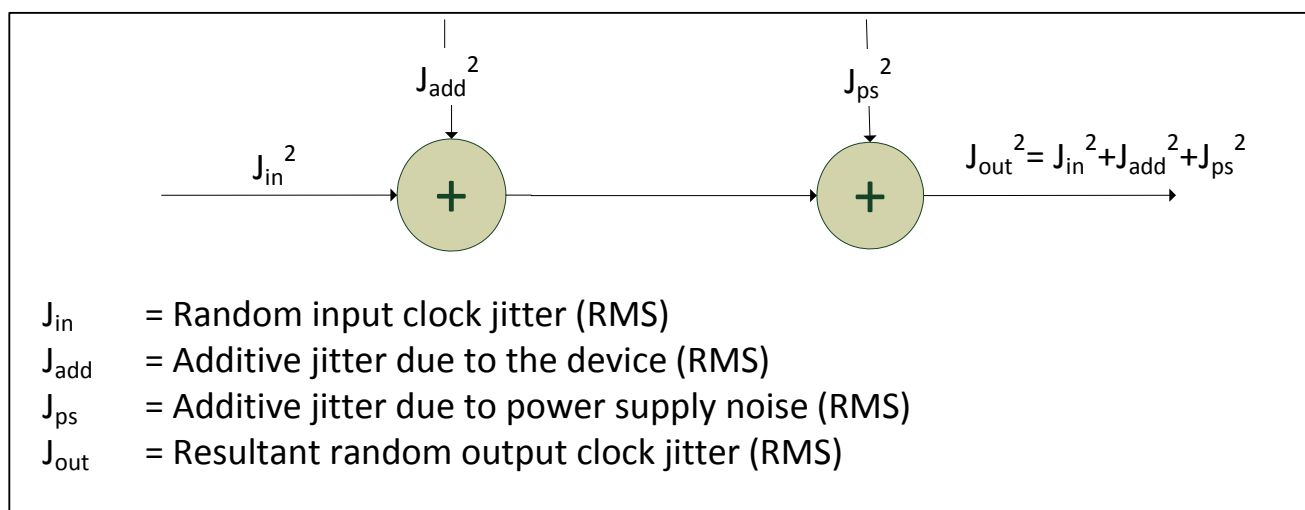


Figure 18 - Additive Jitter



### 3.5 Power Supply

This device operates with either a 2.5V supply or 3.3V supply.

#### 3.5.1 Sensitivity to power supply noise

Power supply noise from sources such as switching power supplies and high-power digital components such as FPGAs can induce additive jitter on clock buffer outputs. The ZL40225 is equipped with a low drop out (LDO) power regulator and on-chip bulk capacitors to minimize additive jitter due to power supply noise. The on-chip regulation, recommended power supply filtering, and good PCB layout all work together to minimize the additive jitter from power supply noise.

#### 3.5.2 Power supply filtering

For optimal jitter performance, the ZL40225 should be isolated from the power planes connected to its power supply pins as shown in Figure 19.

- 10  $\mu\text{F}$  capacitors should be size 0603 or size 0805 X5R or X7R ceramic, 6.3 V minimum rating
- 0.1  $\mu\text{F}$  capacitors should be size 0402 X5R ceramic, 6.3 V minimum rating
- Capacitors should be placed next to the connected device power pins

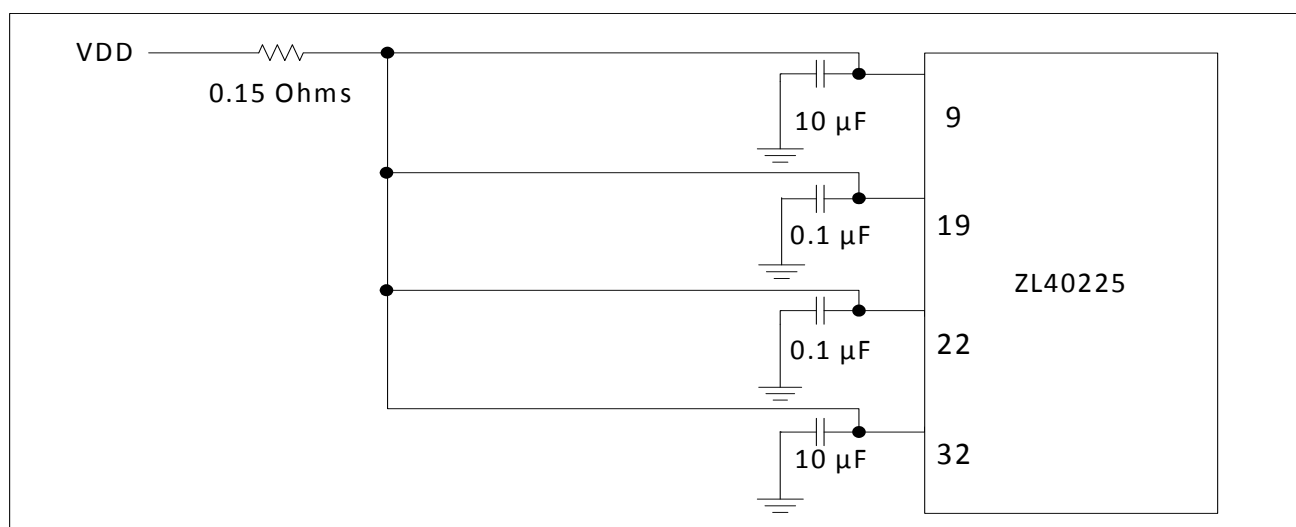


Figure 19 - Decoupling Connections for Power Pins

#### 3.5.3 PCB layout considerations

The power supply filtering shown in Figure 19 can be implemented either as a plane island, or as a routed power topology with equal results.

## 4.0 Electrical Characteristics

### Absolute Maximum Ratings\*

	Parameter	Sym.	Min.	Max.	Units
1	Supply voltage	$V_{DD\_R}$	-0.5	4.6	V
2	Voltage on any digital pin	$V_{PIN}$	-0.5	$V_{DD}$	V
4	LVPECL output current	$I_{out}$		30	mA
5	Soldering temperature	T		260	°C
6	Storage temperature	$T_{ST}$	-55	125	°C
7	Junction temperature	$T_j$		125	°C
8	Voltage on input pin	$V_{input}$		$V_{DD}$	V
9	Input capacitance each pin	$C_p$		500	fF

\* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

\* Voltages are with respect to ground (GND) unless otherwise stated

### Recommended Operating Conditions\*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage 2.5 V mode	$V_{DD25}$	2.375	2.5	2.625	V
2	Supply voltage 3.3 V mode	$V_{DD33}$	3.135	3.3	3.465	V
3	Operating temperature	$T_A$	-40	25	85	°C

\* Voltages are with respect to ground (GND) unless otherwise stated

### DC Electrical Characteristics - Current Consumption

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply current LVPECL drivers - unloaded	$I_{dd\_unload}$		122		mA	
2	Supply current LVPECL drivers - loaded (all outputs are active)	$I_{dd\_load}$		257		mA	Including power to $R_L = 50\Omega$

### DC Electrical Characteristics - Inputs and Outputs - for 3.3 V Supply

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS control logic high-level input voltage	$V_{CIH}$	$0.7 \cdot V_{DD}$			V	
2	CMOS control logic low-level input voltage	$V_{CIL}$			$0.3 \cdot V_{DD}$	V	
3	CMOS control logic Input leakage current	$I_{IL}$		1		$\mu A$	$V_I = V_{DD}$ or 0 V
4	Differential input common mode voltage	$V_{CM}$	1.1		2.0	V	

**DC Electrical Characteristics - Inputs and Outputs - for 3.3 V Supply**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
5	Differential input voltage difference	$V_{ID}$	0.25		1	V	
6	Differential input resistance	$V_{IR}$	80	100	120	ohm	
7	LVPECL output high voltage	$V_{OH}$	$V_{DD} - 1.40$			V	
8	LVPECL output low voltage	$V_{OL}$			$V_{DD} - 1.62$	V	
9	LVPECL output differential voltage*	$V_{OD}$	0.5		0.9	V	

\* This parameter is measured from 125 MHz to 750 MHz

**DC Electrical Characteristics - Inputs and Outputs - for 2.5 V Supply**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS control logic high-level input voltage	$V_{CIH}$	$0.7 \cdot V_{DD}$			V	
2	CMOS control logic low-level input voltage	$V_{CIL}$			$0.3 \cdot V_{DD}$	V	
3	CMOS control logic Input leakage current	$I_{IL}$		1		$\mu A$	$V_I = V_{DD}$ or 0 V
4	Differential input common mode voltage	$V_{CM}$	1.1		1.6	V	
5	Differential input voltage difference	$V_{ID}$	0.25		1	V	
6	Differential input resistance	$V_{IR}$	80	100	120	ohm	
7	LVPECL output high voltage	$V_{OH}$	$V_{DD} - 1.40$			V	
8	LVPECL output low voltage	$V_{OL}$			$V_{DD} - 1.62$	V	
9	LVPECL output differential voltage*	$V_{OD}$	0.4		0.9	V	

\* This parameter is measured from 125 MHz to 750 MHz

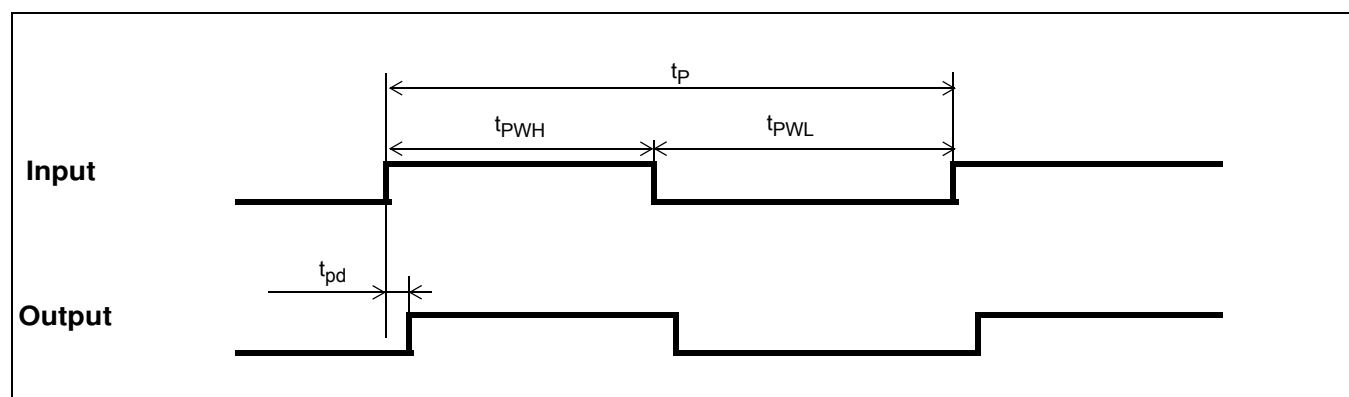


**Figure 20 - Differential Voltage Parameter**

**AC Electrical Characteristics\* - Inputs and Outputs (see Figure 21) - for 2.5/3.3 V supply.**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Maximum Operating Frequency	$1/t_p$			750	MHz	
2	Input to output clock propagation delay	$t_{pd}$	0	1	2	ns	
3	Output to output skew	$t_{out2out}$		50	100	ps	
4	Part to part output skew	$t_{part2part}$		80	300	ps	
5	Output clock Duty Cycle degradation	$t_{PWH}/t_{PWL}$	-2	0	2	Percent	
6	LVPECL Output slew rate	$r_{sl}$	0.75	1.2		V/ns	
7	Reference transition time	$t_{switch}$		0.5	1	us	

\* Supply voltage and operating temperature are as per Recommended Operating Conditions



**Figure 21 - Input To Output Timing**

## 5.0 Performance Characterization

### Additive Jitter at 2.5 V\*

	Output Frequency (MHz)	Jitter Measurement Filter	Typical RMS (fs)	Notes
1	125	12 kHz - 20 MHz	136	
2	212.5	12 kHz - 20 MHz	109	
3	311.04	12 kHz - 20 MHz	92	
4	425	12 kHz - 20 MHz	68	
5	500	12 kHz - 20 MHz	55	
6	622.08	12 kHz - 20 MHz	38	
7	750	12 kHz - 20 MHz	33	

\*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

### Additive Jitter at 3.3 V\*

	Output Frequency (MHz)	Jitter Measurement Filter	Typical RMS (fs)	Notes
1	125	12 kHz - 20 MHz	122	
2	212.5	12 kHz - 20 MHz	92	
3	311.04	12 kHz - 20 MHz	79	
4	425	12 kHz - 20 MHz	61	
5	500	12 kHz - 20 MHz	50	
6	622.08	12 kHz - 20 MHz	40	
7	750	12 kHz - 20 MHz	37	

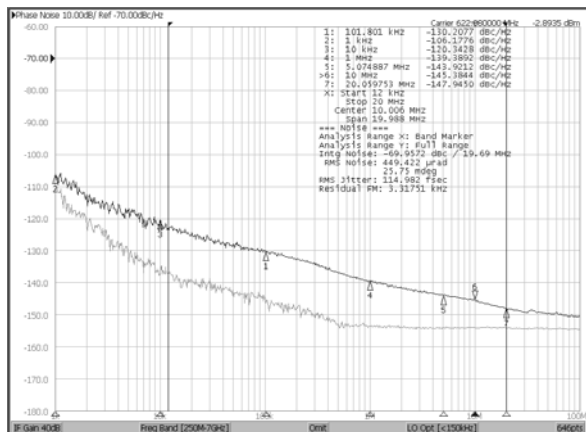
\*The values in this table were taken with an approximate slew rate of 0.8 V/ns

### Additive Jitter from a Power Supply Tone\*

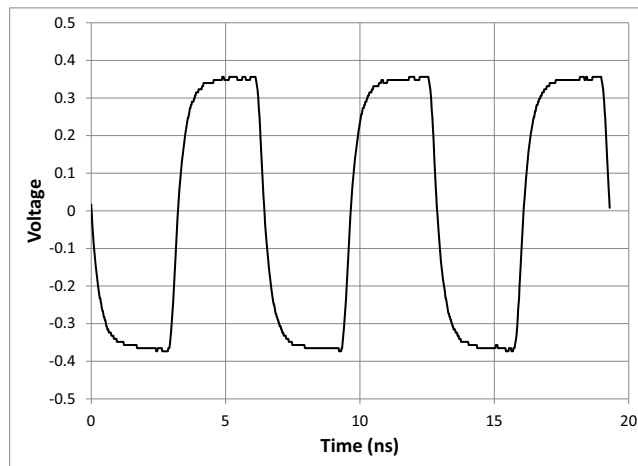
Carrier frequency	Parameter	Typical	Units	Notes
125MHz	25 mV at 100 kHz	85	fs RMS	
750MHz	25 mV at 100 kHz	61	fs RMS	

\* The values in this table are the additive periodic jitter caused by an interfering tone typically caused by a switching power supply. For this test, measurements were taken over the full temperature and voltage range for  $V_{DD} = 2.5$  V. The magnitude of the interfering tone is measured at the DUT.

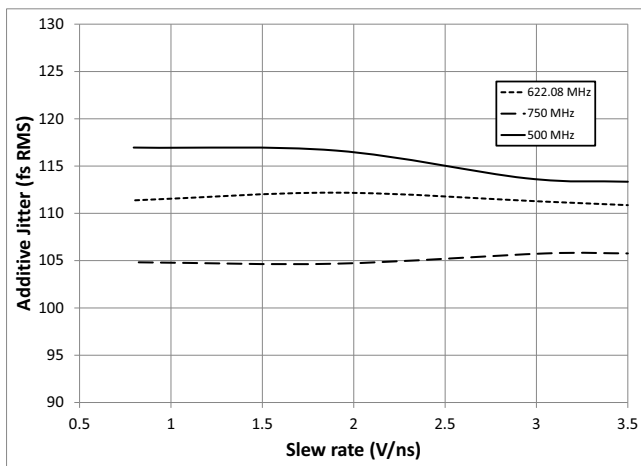
### 6.0 Typical Behavior



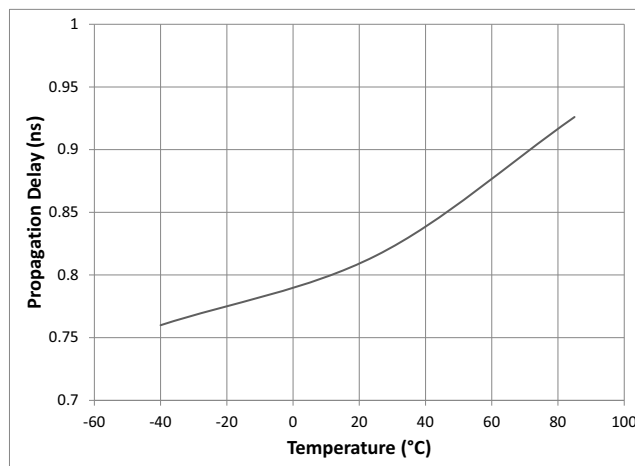
Typical Phase Noise at 622.08 MHz



Typical Waveform at 155.52 MHz

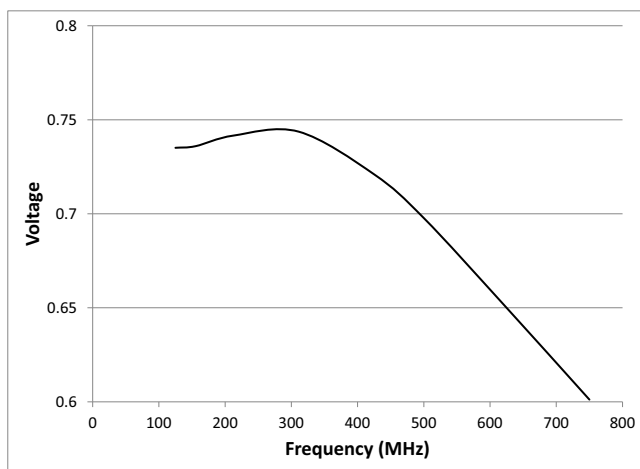


Input Slew Rate versus Additive Jitter

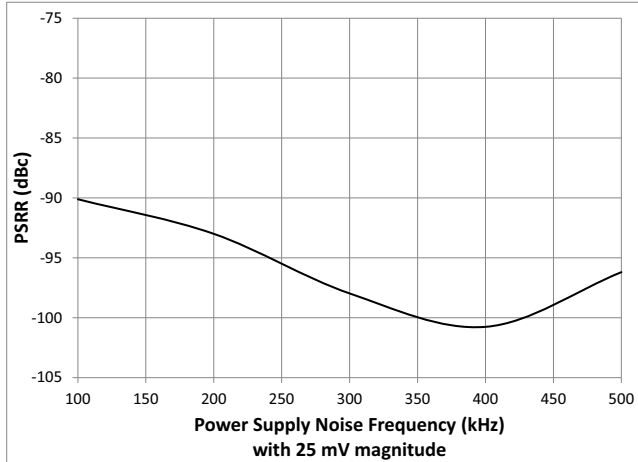


Propagation Delay versus Temperature

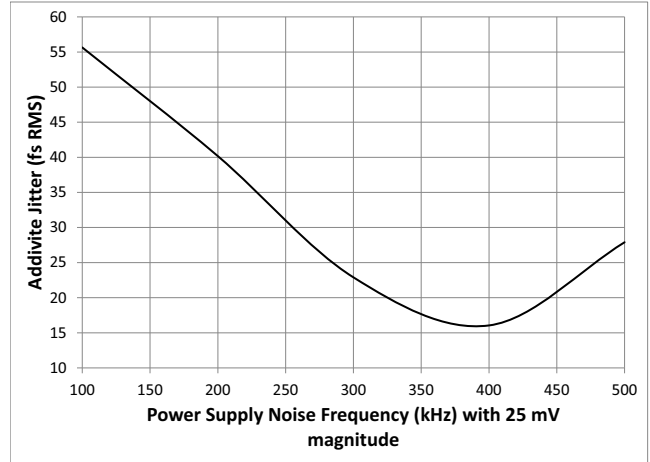
Note: This is for a single device. For more details see the



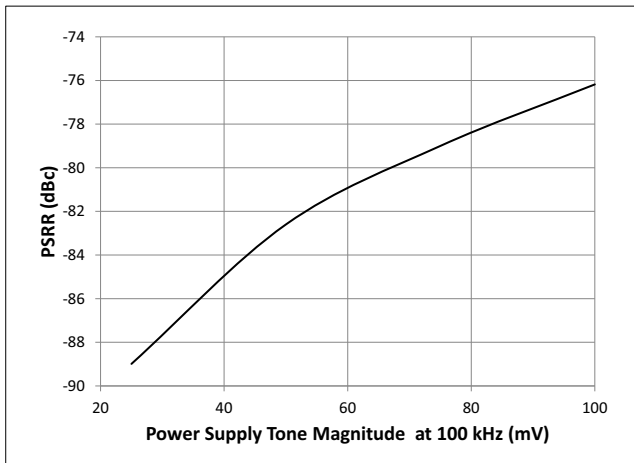
V<sub>OD</sub> versus Frequency



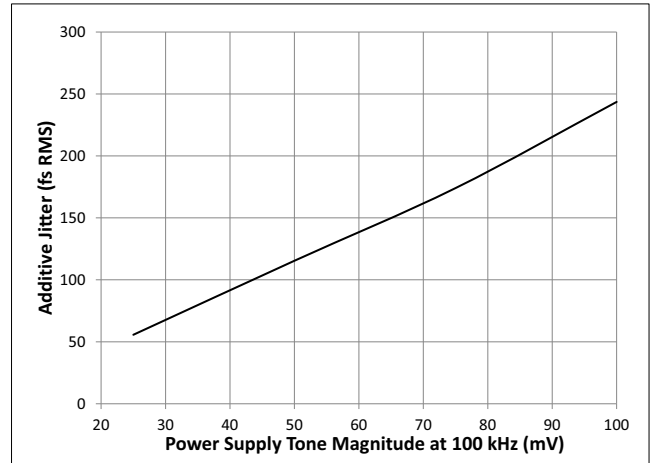
Power Supply Tone Frequency (at 25 mV) versus PSRR at 125 MHz



Power Supply Tone Frequency (at 25 mV) versus Additive Jitter at 125 MHz



Power Supply Tone Magnitude (at 100 kHz) versus PSRR at 125 MHz



Power Supply Tone Magnitude (at 100 kHz) versus Additive Jitter at 125 MHz

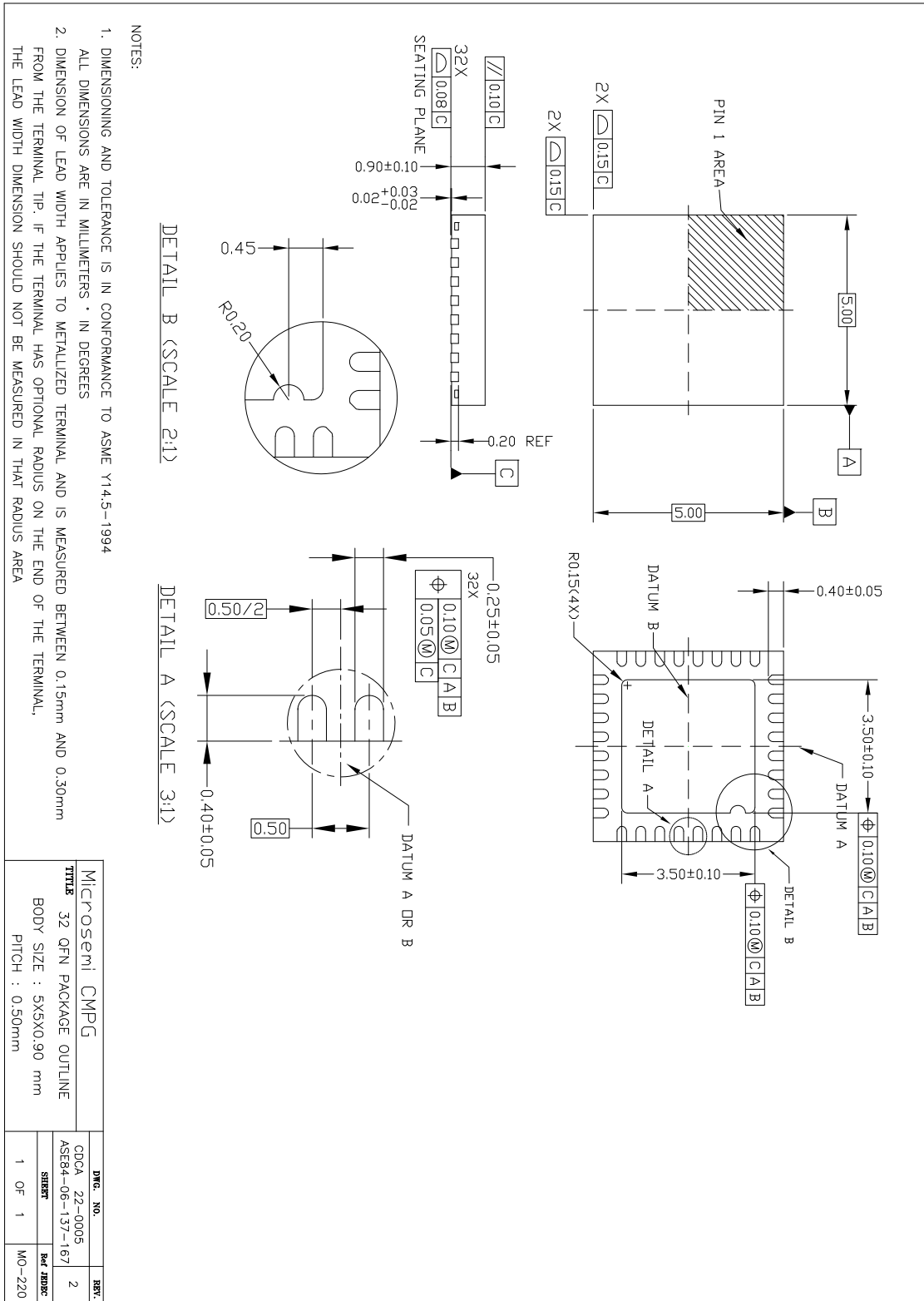
## 7.0 Package Characteristics

### Thermal Data

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	$\Theta_{JA}$	Still Air	37.4	$^{\circ}\text{C}/\text{W}$
		1 m/s	33.1	
		2 m/s	31.5	
Junction to Case Thermal Resistance	$\Theta_{JC}$		24.4	$^{\circ}\text{C}/\text{W}$
Junction to Board Thermal Resistance	$\Theta_{JB}$		19.5	$^{\circ}\text{C}/\text{W}$
Maximum Junction Temperature*	$T_{jmax}$		125	$^{\circ}\text{C}$
Maximum Ambient Temperature	$T_A$		85	$^{\circ}\text{C}$



### 8.0 Mechanical Drawing





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