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Low Skew, Low Additive Jitter 10 output LVPECL/LVDS/HCSL Fanout Buffer with one LVCMOS output

Features

- 3 to 1 input Multiplexer: Two inputs accept any differential (LVPECL, HCSL, LVDS, SSTL, CML, LVCMOS) or a single ended signal and the third input accepts a crystal or a single ended signal
- Ten differential LVPECL/LVDS/HCSL outputs
- One LVCMOS output
- Ultra-low additive jitter: 24fs (integration band: 12kHz to 20MHz at 625MHz clock frequency)
- Supports clock frequencies from 0 to 1.6GHz
- Supports 2.5V or 3.3V power supplies on LVPECL/LVDS/HCSL outputs
- Supports 1.5V, 1.8V, 2.5V or 3.3V on LVCMOS output
- Embedded Low Drop Out (LDO) Voltage regulator provides superior Power Supply Noise Rejection
- Maximum output to output skew of 40ps
- Device controlled via SPI or hardware control pins

Ordering Information

ZL40230LDG1	48 Pin QFN	Trays
ZL40230LDF1	48 pin QFN	Tape and Reel

Package size: 7 x 7 mm

-40°C to +85°C

Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3/4 clock distribution
- Wireless communications
- High performance microprocessor clock distribution
- Test Equipment

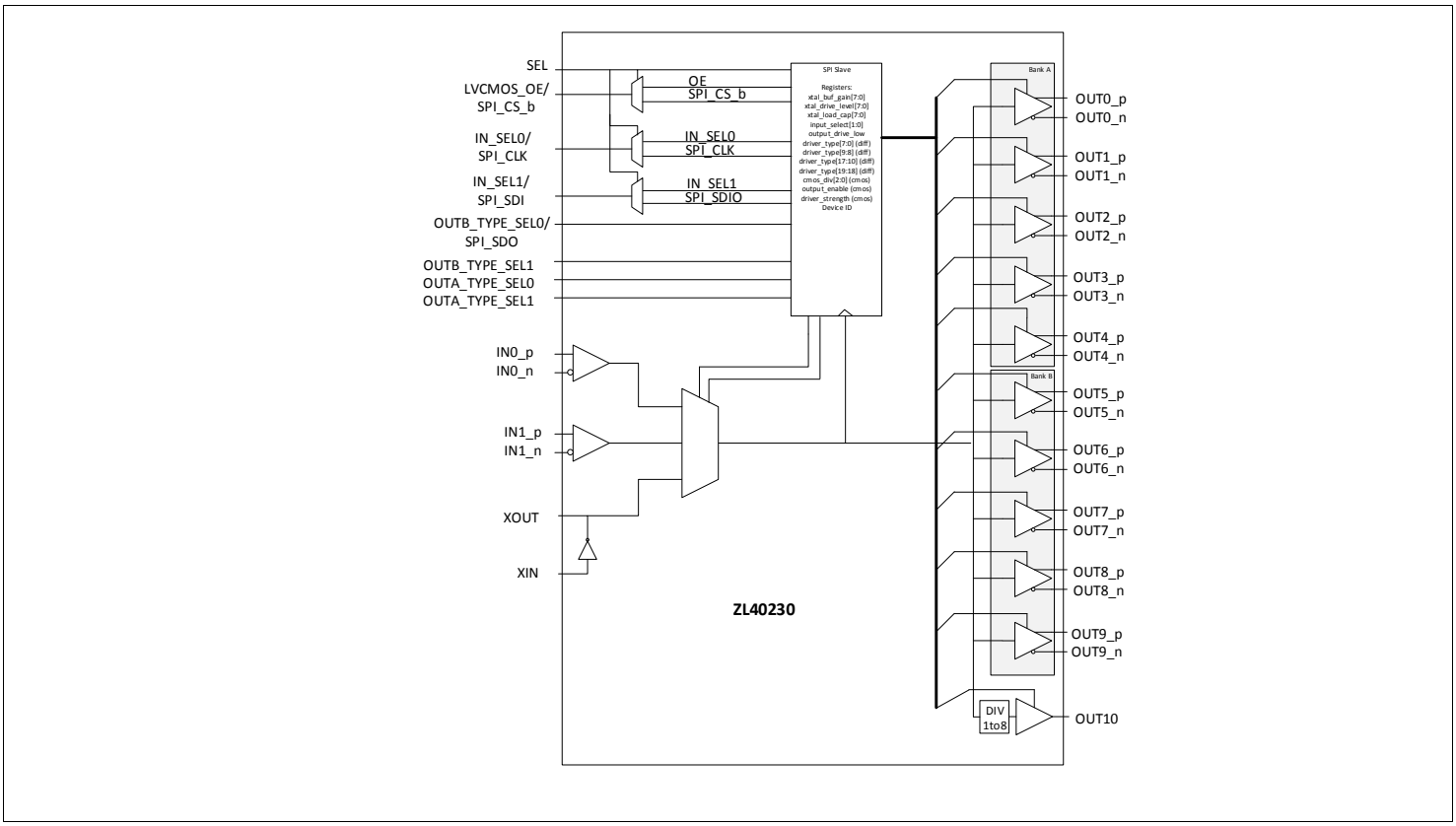

Figure 1. Functional Block Diagram

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Pin Diagram

The device is packaged in a 7x7mm 48-pin QFN.

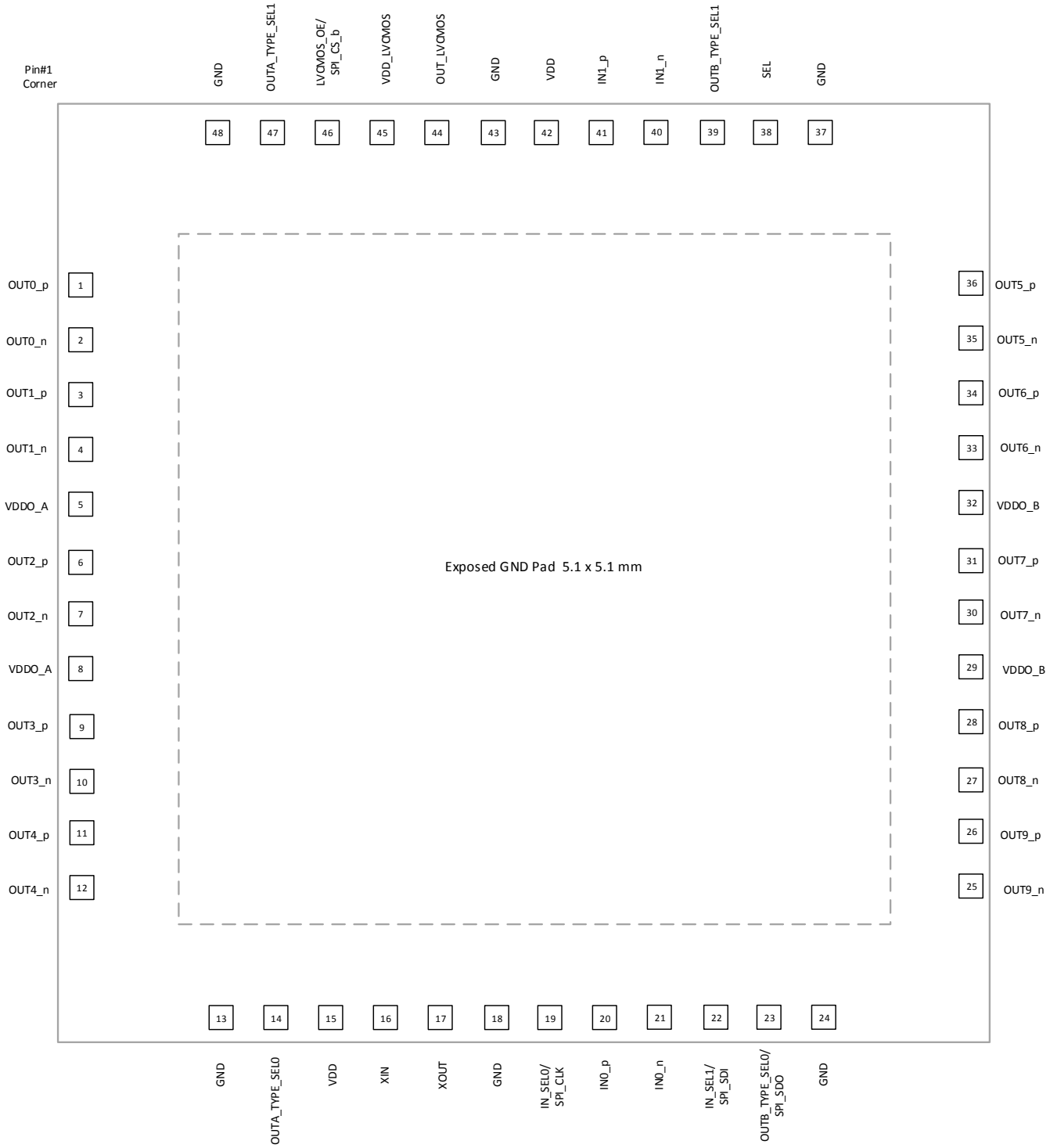

Figure 2. Pin Diagram

Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 300kΩ internal pull-up resistor, I_{PD} – input with 300kΩ internal pull-down resistor, I_{APU} – input with 31kΩ internal pull-up resistor, I_{APD} – input with 30kΩ internal pull-down resistor, $I_{APU/APD}$ – input biased to VDD/2 with 60kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/O – Input/Output pin, NC – No connect, P – power supply pin.

Table 1 Pin Descriptions

#	Name	I/O	Description
Input Reference			
20 21 41 40	IN0_p IN0_n IN1_p IN1_n	I_{APD} $I_{APU/APD}$ I_{APD} $I_{APU/APD}$	**Differential/Single Ended References 0 and 1** Input frequency range 0Hz to 1.6GHz. Non inverting inputs (_p) are pulled down with internal 30kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60kΩ internal resistors (30kΩ equivalent) to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).
Output Clocks			
1 2 3 4 6 7 9 10 11 12 36 35 34 33 31 30 28 27 26 25	OUT0_p OUT0_n OUT1_p OUT1_n OUT2_p OUT2_n OUT3_p OUT3_n OUT4_p OUT4_n OUT5_p OUT5_n OUT6_p OUT6_n OUT7_p OUT7_n OUT8_p OUT8_n OUT9_p OUT9_n	O	**Ultra Low Additive Jitter Differential LVPECL/HCSL/LVDS Outputs 0 to 9** Output frequency range 0 to 1.6GHz In SPI bus controlled mode (SEL pin pulled high on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output is programmable via SPI bus In Hardware control mode (SEL pin pulled low on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output bank is controlled via OUTA/B_TYPE_SEL0/1 pins.
44	OUT_LVCMOS	O	**Ultra Low Additive Jitter LVCMOS Output 0 to 9** Output frequency range 0 to 250MHz
Control			

<table>
<tr><td>19</td><td>IN_SEL0/SPI_CLK</td><td>I_{PD} or I_{PU}</td><td>Input Select 0 or Clock for Serial Interface When SEL pin is low this pin is Input Select 0 hardware control input pin and it is pulled-down with 300 kΩ resistor. When SEL pin is high this pin provides clock for serial micro-port interface and it is pulled-up with 300 kΩ resistor.

<table>
<tr><th>IN_SEL1</th><th>IN_SEL0</th><th>OUTN</th></tr>
<tr><td>0</td><td>0</td><td>Input 0 (IN0)</td></tr>
<tr><td>0</td><td>1</td><td>Input 1 (IN1)</td></tr>
<tr><td>1</td><td>0</td><td>Crystal Oscillator or overdrive</td></tr>
<tr><td>1</td><td>1</td><td>Crystal Bypass</td></tr>
</table></td></tr>
<tr><td>22</td><td>IN_SEL1/SPI_SDI</td><td>I_{PD} or I_{PU}</td><td>Input Select 1 or Serial Interface Input. When SEL pin is low this pin is Input Select 1 hardware control pin and it is pulled-down with 300 kΩ resistor. When SEL pin is high this pin is serial interface input stream and it is pulled-up with 300 kΩ resistor. The serial data stream holds the access command, the address and the write data bits.</td></tr>
<tr><td>23</td><td>OUTB_TYPE_SEL0
SPI_SDO</td><td>I/O</td><td>Output Signal for Bank B or Serial Interface Output.
When SEL pin is low this pin and pin 39 select type of the output Bank B (outputs 5 to 9).
<table>
<tr><th>OUTB_TYPE_SEL1</th><th>OUTB_TYPE_SEL0</th><th>Output 5 to 9</th></tr>
<tr><td>0</td><td>0</td><td>LVPECL</td></tr>
<tr><td>0</td><td>1</td><td>LVDS</td></tr>
<tr><td>1</td><td>0</td><td>HCSL</td></tr>
<tr><td>1</td><td>1</td><td>High-Z (Disabled)</td></tr>
</table>
When SEL pin is high this pin is Serial interface output stream. As an output the serial stream holds the read data bits.</td></tr>
<tr><td>39</td><td>OUTB_TYPE_SEL1</td><td>I_{PD}</td><td>Output Signal for Bank B
When SEL pin is low this pin and pin 23 selects type of the output Bank B (outputs 5 to 9).
When SEL pin is high this pin is unused and it should be left unconnected or connected to GND for mechanical support.</td></tr>
<tr><td>46</td><td>LVCMOS_OE/
SPI_CS_b</td><td>I_{PD} or I_{PU}</td><td>LVCMOS Output Enable or Chip Select for Serial Interface.
When SEL pin is low this pin is LVCMOS Output Enable hardware control input and it is pulled-down with 300 kΩ resistor.
When SEL pin is high this pin is serial interface chip select and it is pulled-up with 300 kΩ resistor--this is an active low signal.</td></tr>
</table>

<table>
<tr><td>14
47</td><td>OUTA_TYPE_SEL0
OUTA_TYPE_SEL1</td><td>I_{PD}</td><td>Output Signal for Bank A:
When SEL pin is low these two pins Selects Type of the output for Bank A (Outputs 0 to 4)

<table><tr><td>OUTA_TYPE_SEL1</td><td>OUTA_TYPE_SEL0</td><td>Output 0 to 4</td></tr><tr><td>0</td><td>0</td><td>LVPECL</td></tr><tr><td>0</td><td>1</td><td>LVDS</td></tr><tr><td>1</td><td>0</td><td>HCSL</td></tr><tr><td>1</td><td>1</td><td>High-Z (Disabled)</td></tr></table>
When SEL pin is high these two pins are unused and should be left unconnected or connected to GND for mechanical support.</td></tr>
<tr><td colspan="4">Crystal Oscillator</td></tr>
<tr><td>16</td><td>XIN</td><td>I</td><td>Crystal Oscillator Input or crystal bypass mode or crystal overdrive mode</td></tr>
<tr><td>17</td><td>XOUT</td><td>O</td><td>Crystal Oscillator Output</td></tr>
<tr><td colspan="4">Hardware/SPI Control selection</td></tr>
<tr><td>38</td><td>SEL</td><td>I</td><td>Select control.
When this pin is low, the device is controlled via hardware pins, IN_SEL0/1 and OE.
When this pin is high, the device is controlled via SPI port.

Any change of SEL pin value requires power cycle. Hence, SEL pin cannot be changed on the fly.</td></tr>
<tr><td colspan="4">Power and Ground</td></tr>
<tr><td>15
42</td><td>VDD</td><td>P</td><td>Positive Supply Voltage. Connect to 3.3V or 2.5V supply.</td></tr>
<tr><td>5
8</td><td>VDDO_A</td><td>P</td><td>Positive Supply Voltage for Differential Outputs Bank A Connect to 3.3V or 2.5V power supply. VDDO_A does not have to be connected to the same voltage level as VDD or VDDO_B.
These pins power up differential outputs OUT[0:4]_p/n.</td></tr>
<tr><td>29
32</td><td>VDDO_B</td><td>P</td><td>Positive Supply Voltage for Differential Outputs Bank B Connect to 3.3V or 2.5V power supply. VDDO_B does not have to be connected to the same voltage level as VDD or VDDO_A.
These pins power up differential outputs OUT[5:9]_p/n.</td></tr>
<tr><td>45</td><td>VDD_LVCMOS</td><td>P</td><td>Power Supply Voltage for LVCMOS Output Connect to 3.3V, 2.5V, 1.8V or 1.5V power supply.</td></tr>
</table>

13 18 24 43 37 48	GND	P	**Ground** Connect to the ground
E-Pad	GND	P	**Ground.** Connect to the ground

Functional Description

The ZL40230 is a programmable or hardware pin controlled low additive jitter, low power 3 x 10 LVPECL/HCSL/LVDS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML) or single ended (LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins. All the other components for building crystal oscillator are built in device such as load capacitance, series and shunt resistors.

The ZL40230 has ten LVPECL/HCSL/LVDS outputs which can be powered from 3.3V or 2.5V supply. Each output can be independently enabled/disabled via SPI bus. The type of each output driver can be programmed to be LVPECL, HCSL or LVDS. Hence, the device can be configured to support different signaling formats depending on the application.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40230 inputs.

Figure 3 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each and Ro + Rs should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 8). The source resistors of Rs = 270Ω could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270Ω + 50Ω)) = 5.16mA.
For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

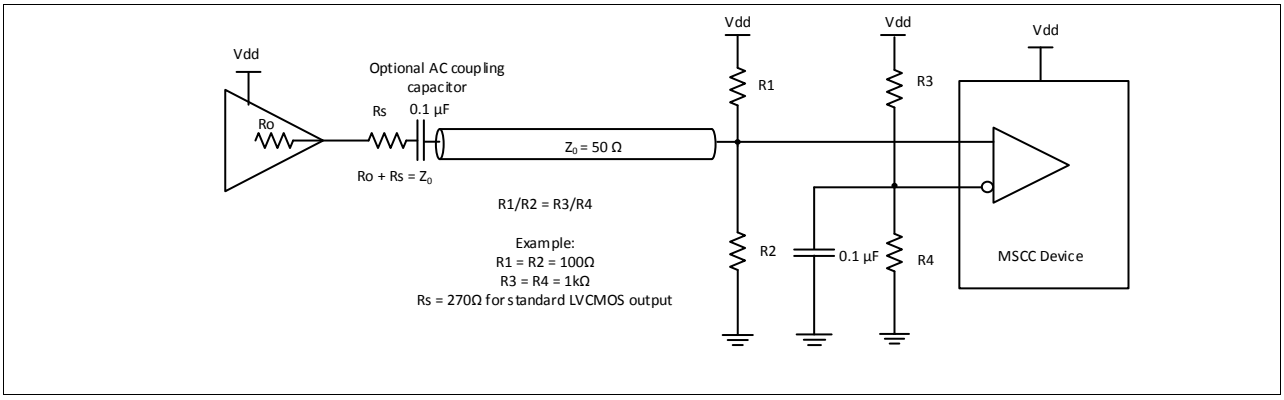

Figure 3. Input driven by a single ended output

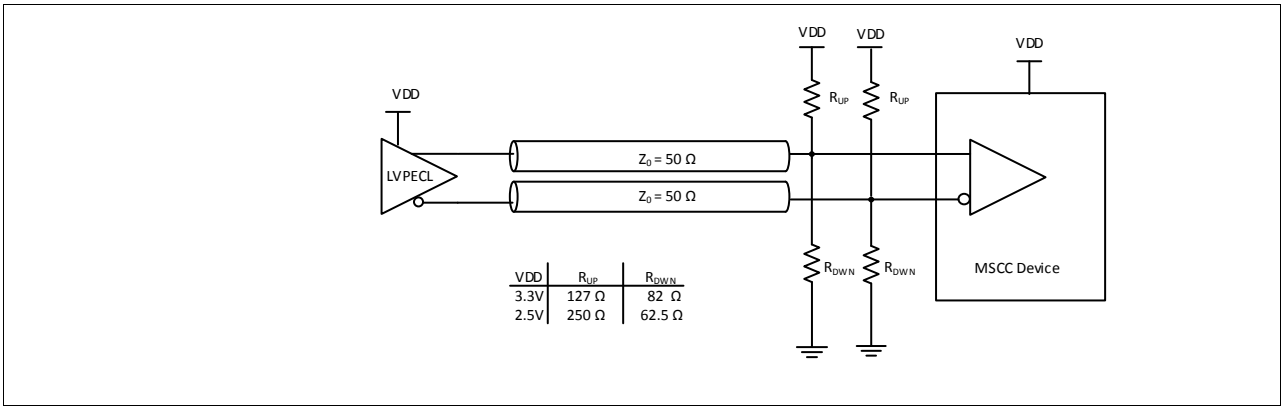

Figure 4. Input driven by DC coupled LVPECL output

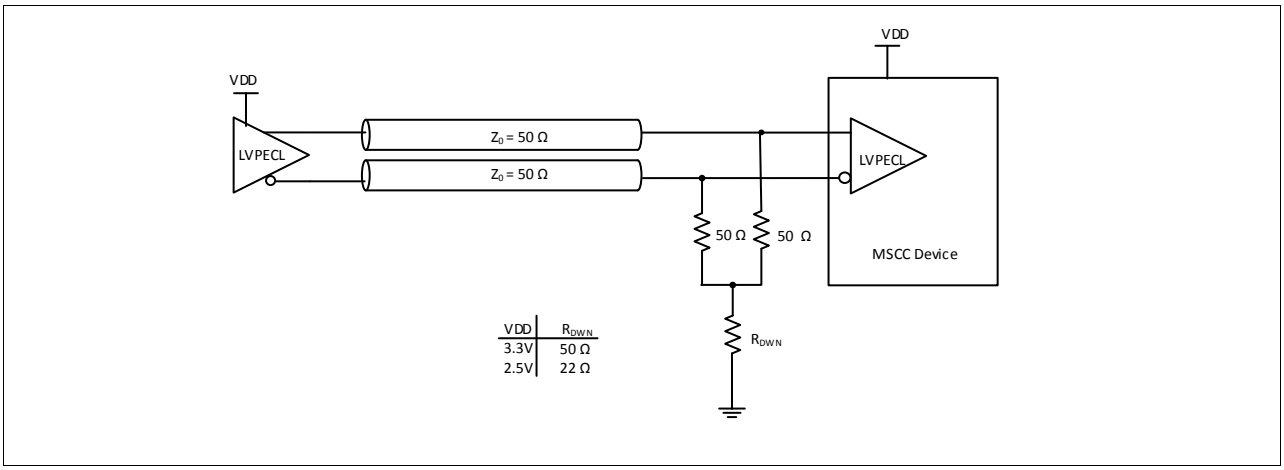

Figure 5. Input driven by DC coupled LVPECL output (alternative termination)

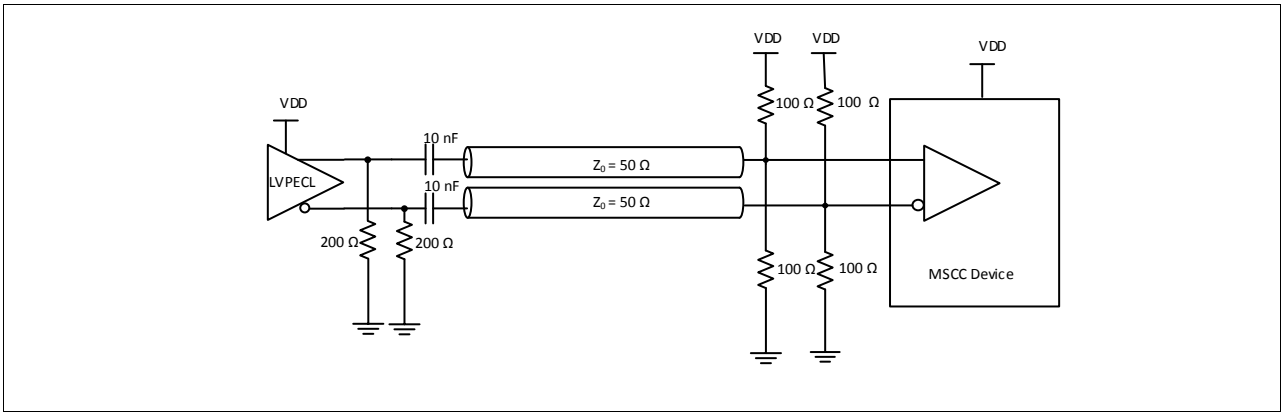

Figure 6. Input driven by AC coupled LVPECL output

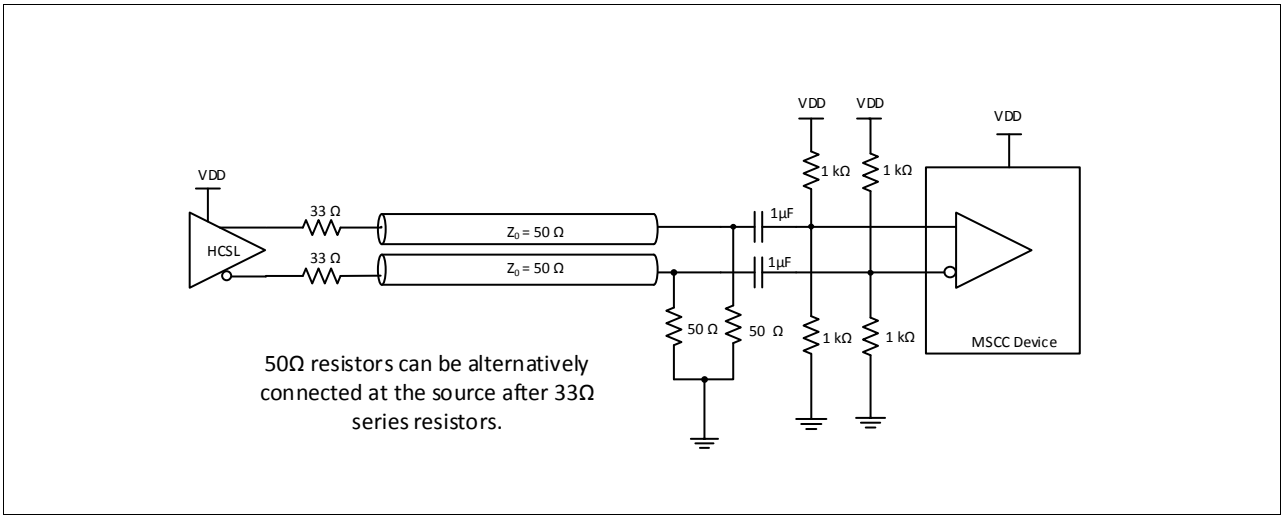

Figure 7. Input driven by HCSL output

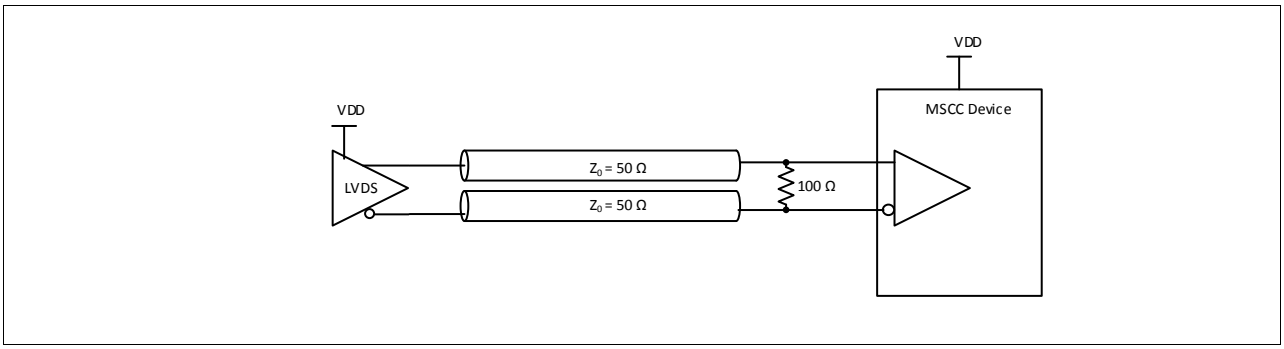

Figure 8. Input driven by LVDS output

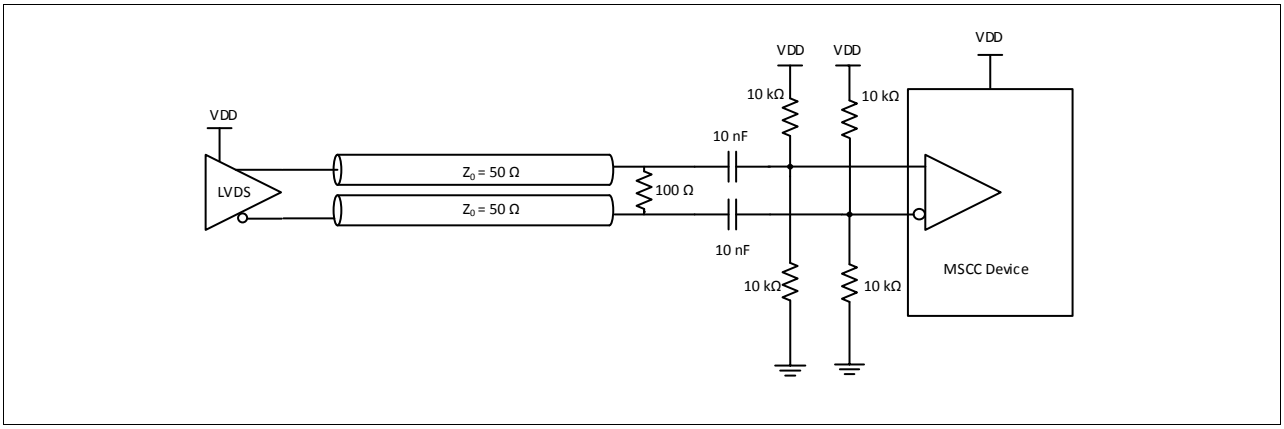

Figure 9. Input driven by AC coupled LVDS

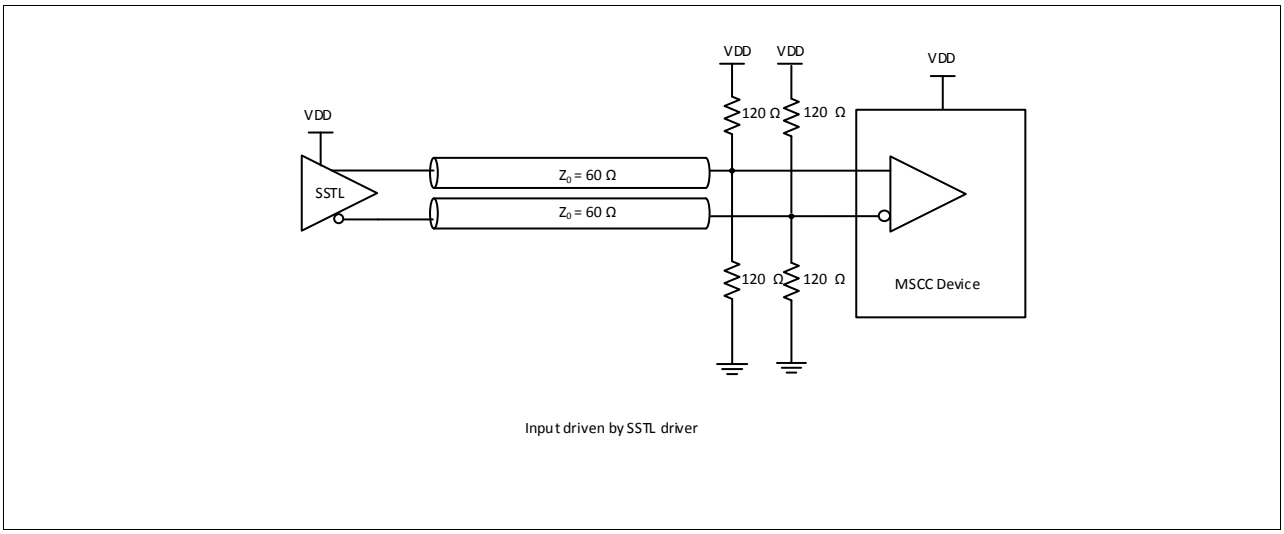

Figure 10. Input driven by an SSTL output

Clock Outputs

LVCMOS output OUT10 require only series termination resistor whose value is depending on LVCMOS output voltage as shown in Figure 11.

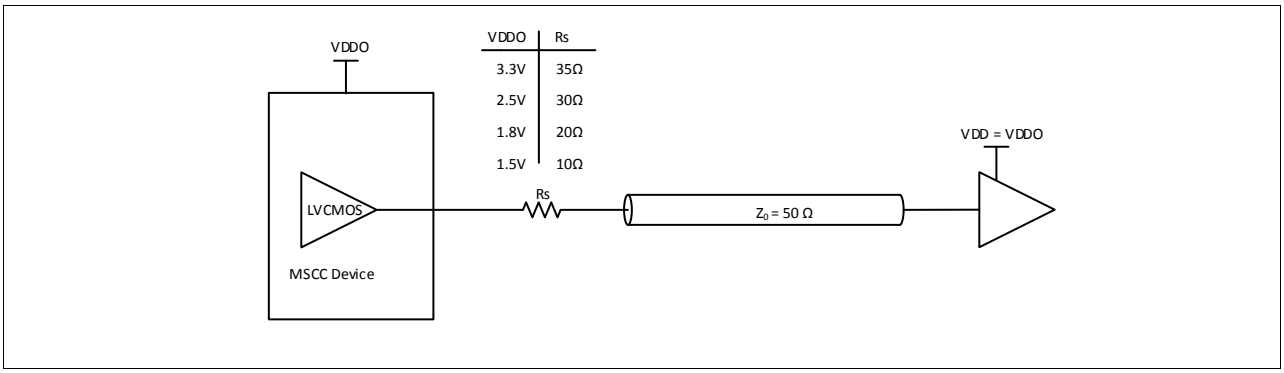

Figure 11. Termination for LVCMOS output

Differential outputs LVPECL and LVDS should have same termination as corresponding outputs described in previous section. HCSL outputs should be terminated with 33Ω series resistors at the source and 50Ω shunt resistors at the source or at the end on the transmission line. AC coupling and re-biasing is not required at the outputs when driving native HCSL receivers.

The device is designed to drive differential input of semiconductor devices. In applications that use a transformer to convert from the differential to the single ended output (for example driving an oscilloscope 50Ω input), a resistor larger than 10Ω should be added at the center tap of the primary winding to achieve optimum jitter performance as shown in Figure 12. This is to provide a nominal common mode impedance of 10Ω or higher which is typical for differential terminations.

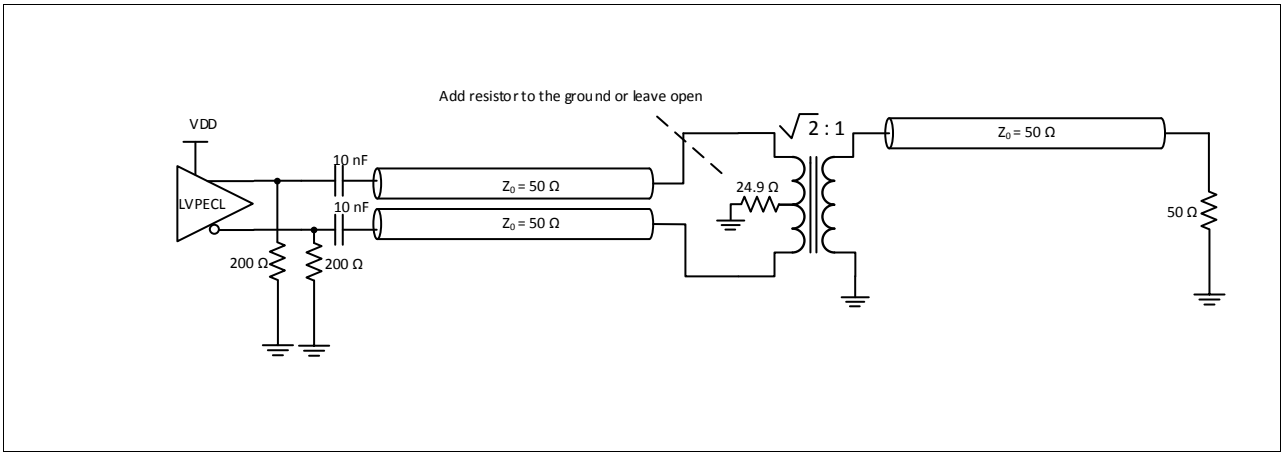

Figure 12. Driving a load via transformer

Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8MHz to 160MHz. As can be seen in the following figure only crystal resonator is required and all the other components are built-in the device. To be able support crystal resonators with different characteristics all internal components are programmable.

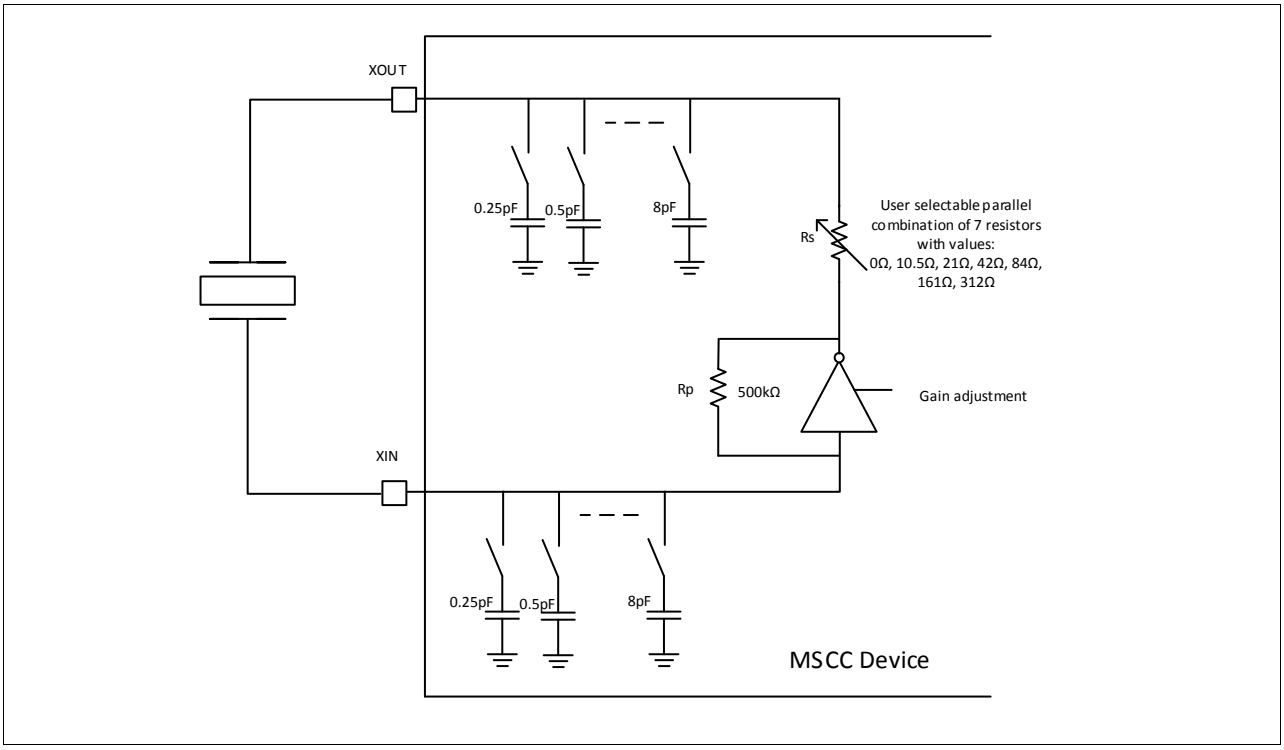

Figure 13. Crystal Oscillator Circuit

The load capacitors can be programmed from 0 to 21.75 pF (4pF default) with resolution of 0.25pF which not only meets load requirement for most crystal resonator but also allows for fine tuning of the crystal resonator frequency. The amplifier gain can be adjusted in five steps and series resistor can be adjusted as parallel combination of seven different resistors: 0Ω, 10.5Ω, 21Ω, 42Ω, 84Ω, 161Ω and 312Ω.(84Ω default) Although the first resistor is 0Ω the series resistance Rs will be slightly higher than 0Ω due to parasitic resistance of the switch which connects resistor. Hence the minimum series resistance is achieved when all seven resistors are connected in parallel. The shunt resistor is fixed and its value is 500kΩ.

In Hardware Controlled mode the capacitive load is set at 4pF, internal series resistance to 84Ω and they cannot be changed. For Crystal requiring higher load or series resistance additional capacitance and/or series resistance can be added externally as shown in the Figure 14.

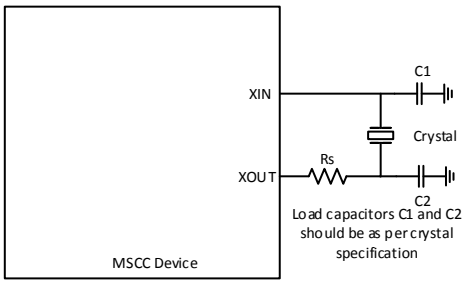

Figure 14. Crystal Oscillator Circuit in Hardware Controlled Mode

Termination of unused inputs and outputs

Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by 1kΩ resistor. Unused outputs should be left unconnected.

Power Consumption

The device total power consumption can be calculated as:

$$P_T = P_S + P_{XTAL} + P_C + P_{O\_DIF} + P_{O\_LVCMOS}$$

Where:

$P_S = V_{DD} \times I_S$ — The core power when XTAL is not used. The current is specified in Table 7. .If XTAL is running this power should be set to zero.

$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$ — The core power when XTAL is used. The current is provided in Table 7. . If XTAL is not used this power should be set to zero.

$P_C = V_{DDO} \times I_{DD\_CM}$ — Common output power shared among all ten outputs. The current I_{DD_CM} is specified Table 7.

$$P_{O\_DIF} = V_{DDO} \times (I_{DD\_LVDS} \times N_1 + I_{DD\_LVPECL} \times N_2 + I_{DD\_HCSL} \times N_3)$$

Output power where the output currents are specified Table 7.
N_1, N_2 and N_3 are number of enabled LVPECL, LVDS and HSCL outputs respectively and $N_1+N_2+N_3$ is less or equal to 10.

$$P_{O\_LVCMOS} = V_{DD\_LVCMOS} \times (I_{DD} \times f / 100MHz + V_{DD\_LVCMOS} \times C_{LOAD} \times f)$$

Dynamic LVCMOS output power. I_{DD} is specified in Table 7. If LVCMOS output is disabled this term is equal to zero.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption.

$$P_D = P_T - N_1 \times P_{LVPECL} - N_2 \times P_{LVDS} - N_3 \times P_{HCSL}$$

Where N_1, N_2 and N_3 are the number of enabled LVPECL, LVDS and HSCL outputs respectively. Since there are ten differential outputs $N_1 + N_2 + N_3$ will be less or equal to 10.

$$P_{LVPECL} = (V_{OH} - V_B)^2 / 50\Omega + (V_{OL} - V_B)^2 / 50\Omega + (V_{OH} - V_B) \times V_B / 50\Omega + (V_{OL} - V_B) \times V_B / 50\Omega$$

V_{OH} and V_{OL} are the output high and low voltages respectively for LVPECL output

V_B is LVPECL bias voltage equal to V_{DD} – 2V

$$P_{LVDS} = V_{SW}^{\ 2} / 100\Omega$$

V_{SW} is voltage swing of LVDS output.

$$P_{HCSL} = (V_{SW} / 50\Omega)^2 \times (33\Omega + 50\Omega)$$

V_{SW} is voltage swing of HCSL output. 50Ω is termination resistance and 33Ω is series resistance of the HCSL output.

Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulated with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling for each power pin.

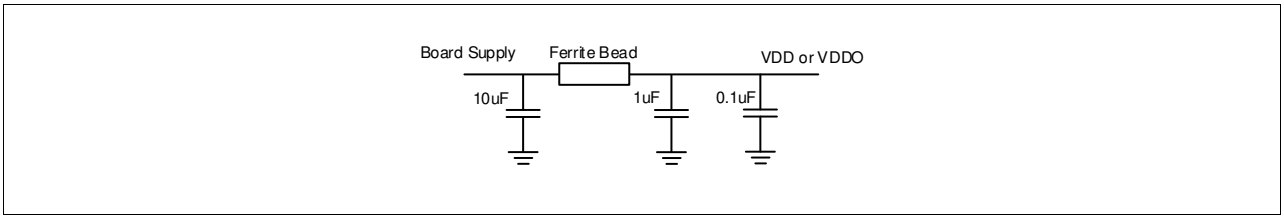

Figure 15. Power Supply Filtering

Power Supplies and Power-up Sequence

The device has four different power supplies: VDD, VDDO_A, VDDO_B and VDD_LVCMOS which are mutually independent. Voltages supported by each of these power supplies are specified in Table 1.

The device is not sensitive to the power-up sequence. For example commonly used sequence where higher voltage comes up before or at the same time as the lower voltages can be used (or any other sequence).

Host Interface

ZL30230 can be controlled via hardware pins (SEL pin tied low) or via SPI port (SEL pin tied high). The mode shall be selected during power up and it cannot be changed on the fly.

Hardware Control Mode

In this mode, ZL40230 is controlled via Input Select (IN_SEL0/1) pins which select which one of three inputs is fed to the output and show in Table 2 and OUTA/B_TYPE_SEL0/1 pins which select signal level (LVPECL, LVDS, HCSL or Hi-Z) for each of two (A and B) output banks as shown in Table 3.
All input control pins have low input threshold voltage so they can be driven from the device with low output voltage (FPGA/CPLD). Supported voltages are between 1.2V and VDD (2.5V or 3.3V).

Table 2 Input clock selection

IN_SEL1	IN_SEL0	Selected Input
0	0	IN0_p, IN0_n
0	1	IN1_p, IN1_n
1	X	XIN

Table 3 Output Type Selection

OUTA/B_TYPE_SEL1	OUTA/B_TYPE_SEL0	Output
0	0	LVPECL
1	1	LVDS
1	0	HCSL
1	1	High-Z (Output Disabled)

Output is disabled synchronously on the falling edge of the input (t_2) as shown in Figure 16.

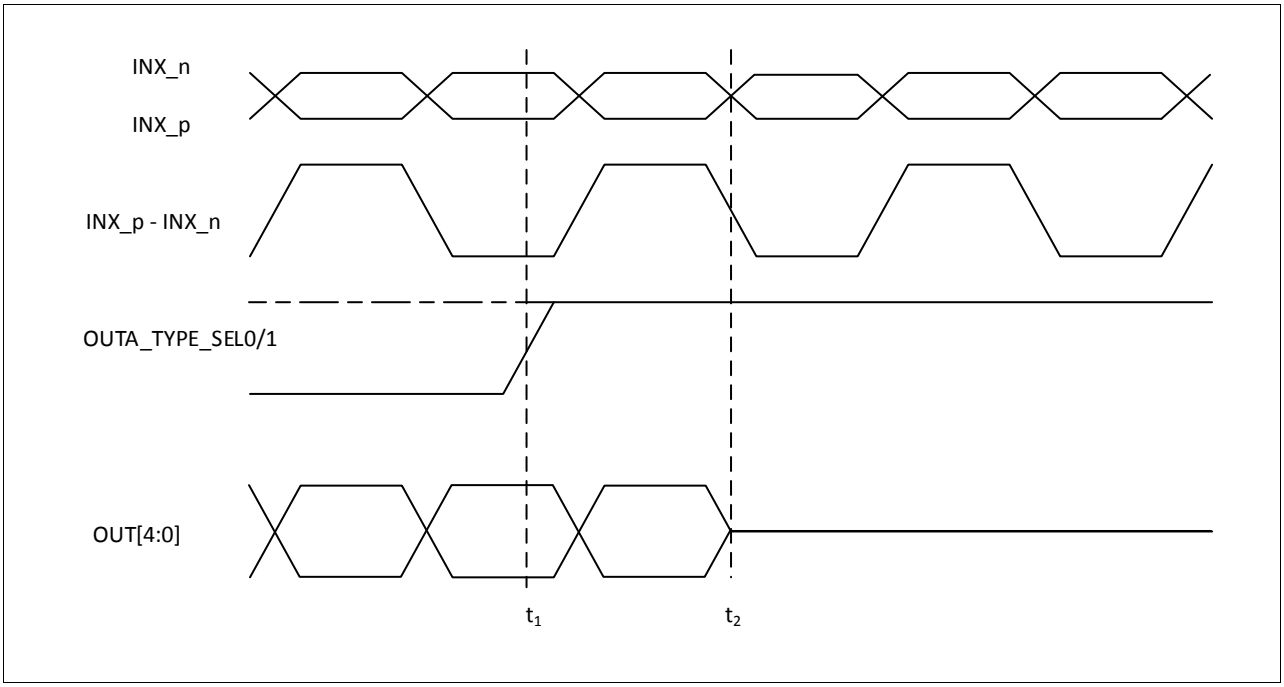

Figure 16. Output Disable

Outputs can be enabled by toggling one or both OUTA/B_TYPE_SEL0/1 pins low depending on which type of interface needs to be enabled for particular bank. As soon as one or both OUTA/B_TYPE_SEL0/1 pins go low (t_1) the outputs will go from high-Z to low (OUTX_p = low, OUTx_n = high) and will start to track the input after the first falling edge (t_2) of the input signal as shown in Figure 17.

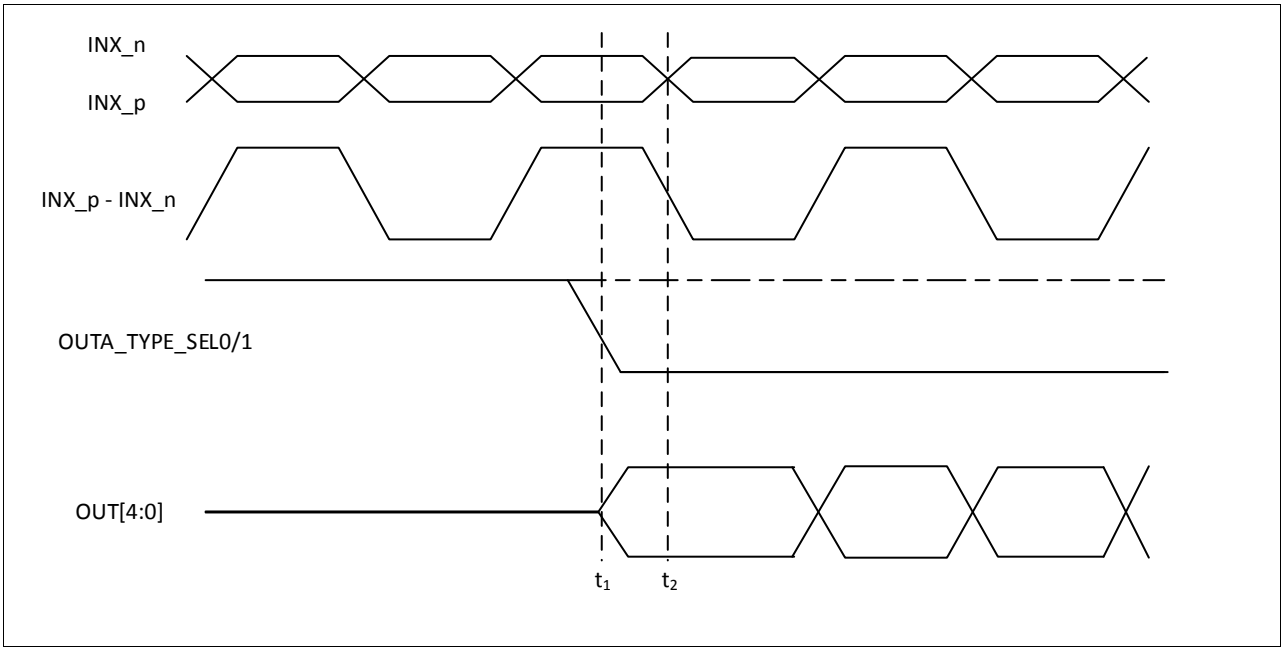

Figure 17. Output Enable

Figures above show enable/disable waveform for the output bank A (OUT[4:0]). The waveforms are equivalent for the output bank B (OUT[9:5]) which is controlled by OUTB_TYPE_SEL0/1 pins.

SPI Control Mode

ZL40230 is controlled via four pin SPI slave interface as shown in the following figure.

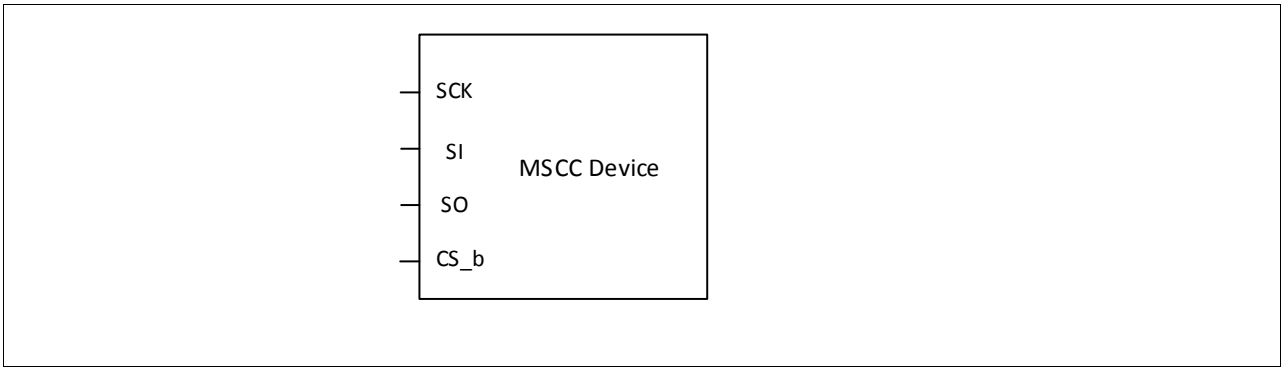

Figure 18. SPI slave interface

All SPI input pins have low threshold voltage so they can be driven from low output voltage SPI master device. Supported voltages are between 1.2V and VDD (2.5V or 3.3V). This allows device to be controlled from an FPGA with low voltage I/O supply.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **SO** pin must be ignored. Similarly, the input data on the **SI** pin is ignored by the device during a read cycle.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission or Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **SCK** pin when the **CS_b** pin is active. If the **SCK** pin is low during **CS_b** activation, then MSb first timing is selected. If the **SCK** pin is high during **CS_b** activation, then LSb first timing is assumed.

The SPI port expects 1-bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **CS_b** pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal **CS_b** is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

Functional waveforms for the LSb and MSb first mode, and burst mode are shown in Figure 19 and Figure 20 respectively. Figure 21 shows an example of burst mode operation which allows user to read or write consecutive location in the register map.

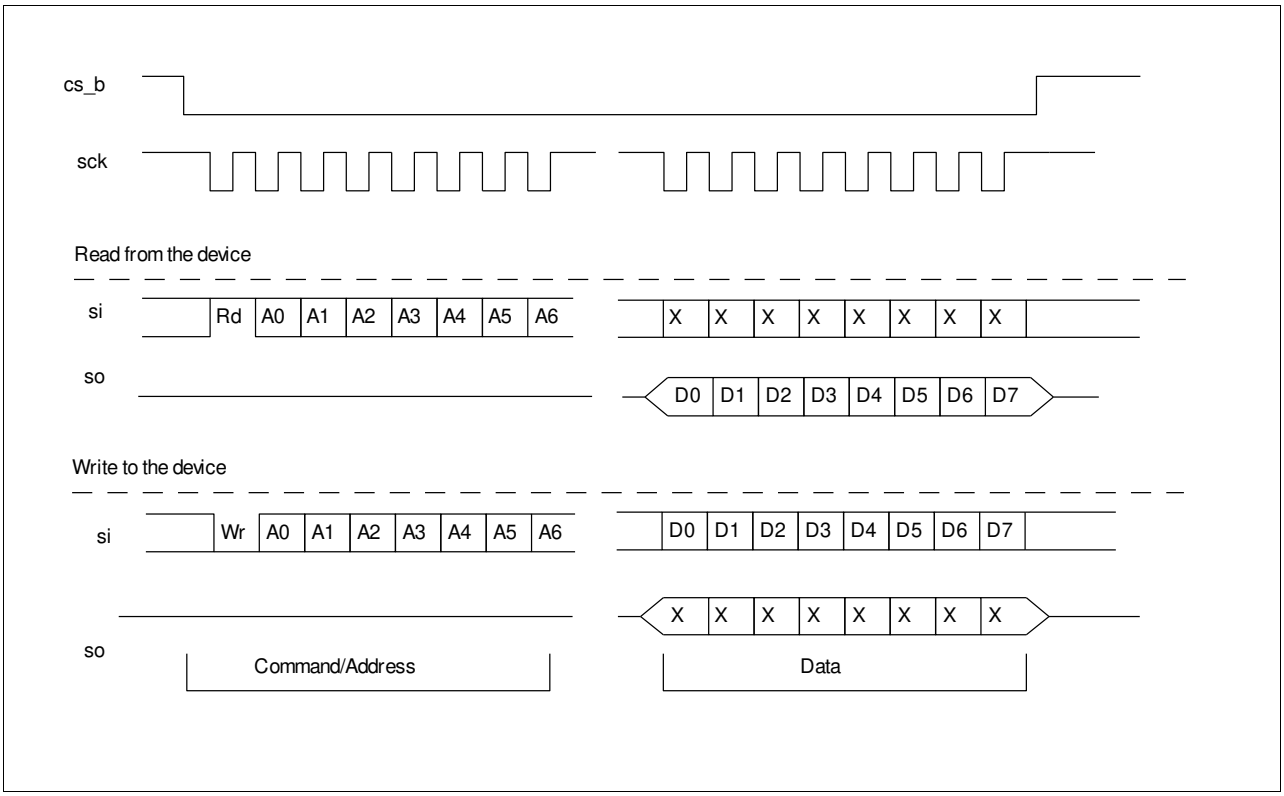

Figure 19. Serial Peripheral Interface Functional Waveform – LSB First Mode

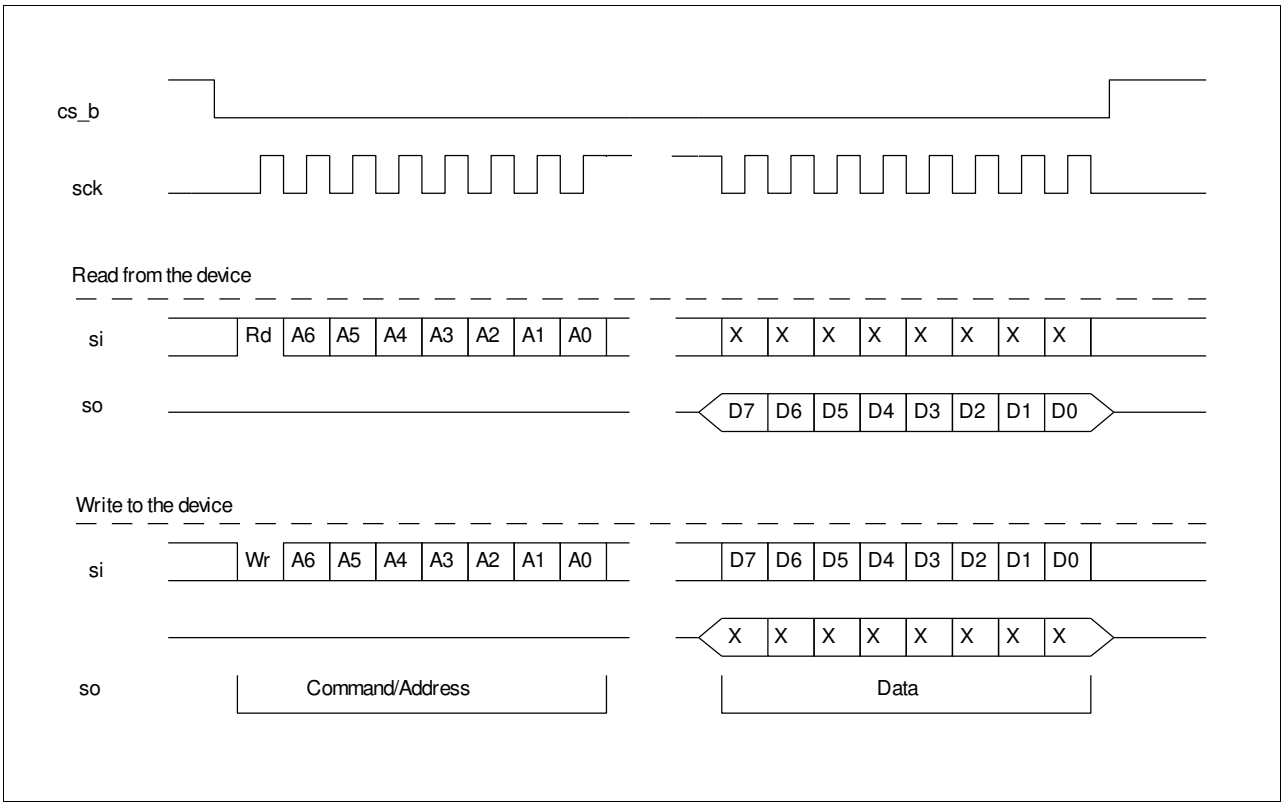

Figure 20. Serial Peripheral Interface Functional Waveform – MSB First Mode

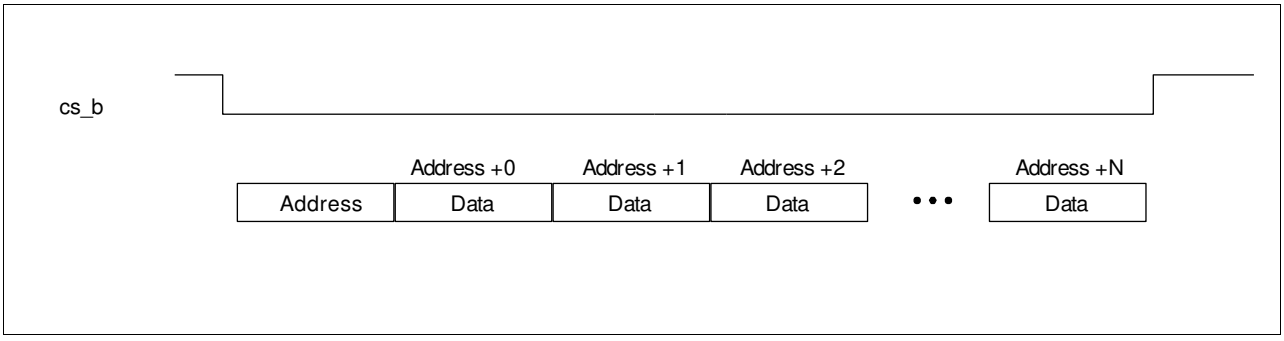

Figure 21. Example of the Burst Mode Operation

Typical device performance

The following plots show typical device performances

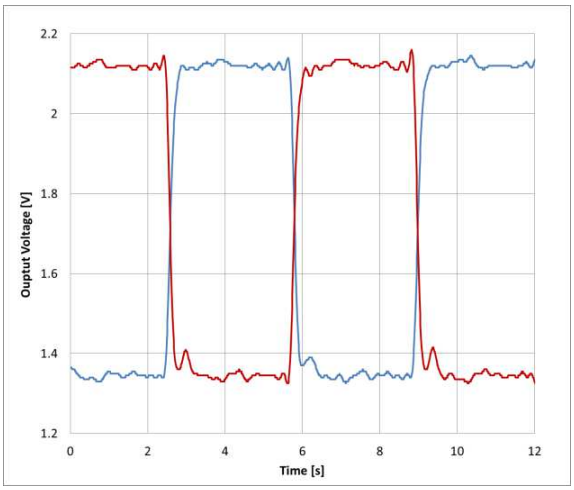

Figure 22. 156.25MHz LVPECL

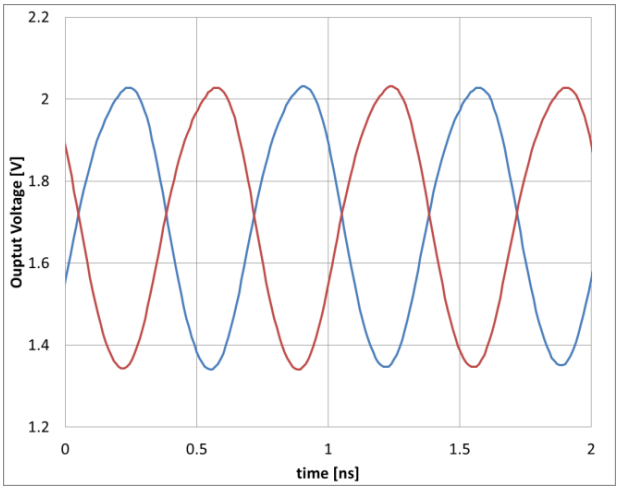

Figure 23. 1.5GHz LVPECL

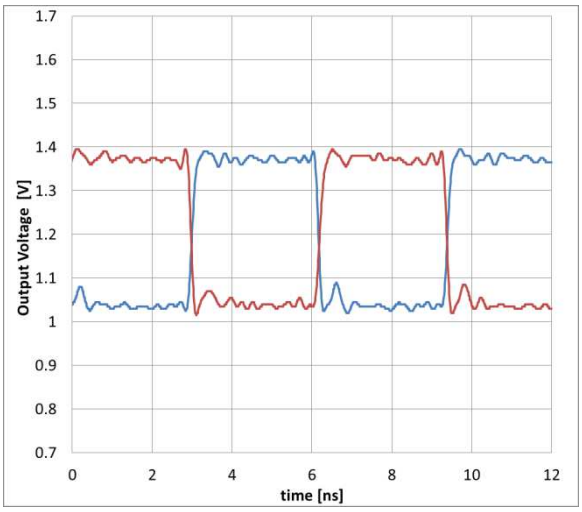

Figure 24. 156.25MHz LVDS

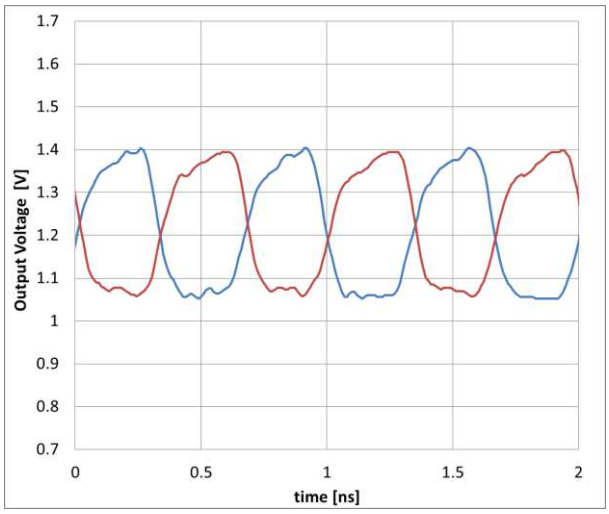

Figure 25. 1.5GHz LVDS

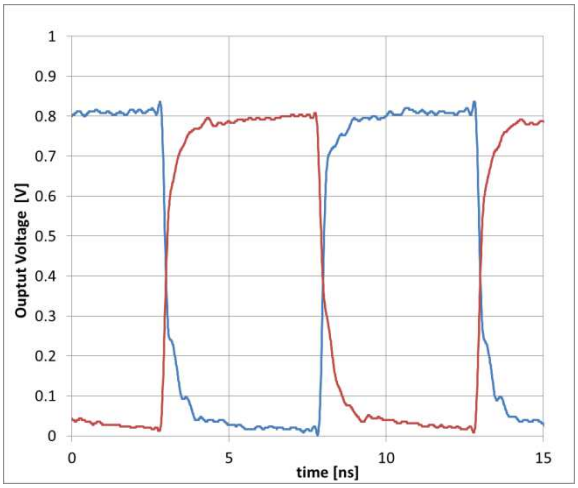

Figure 26. 100MHz HCSL

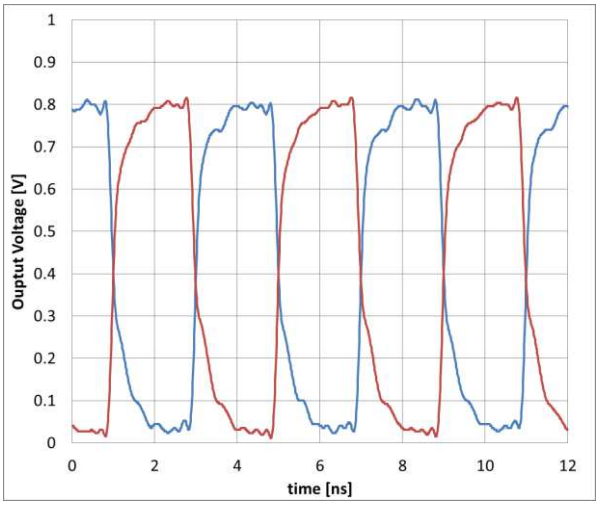

Figure 27. 250MHz HCSL

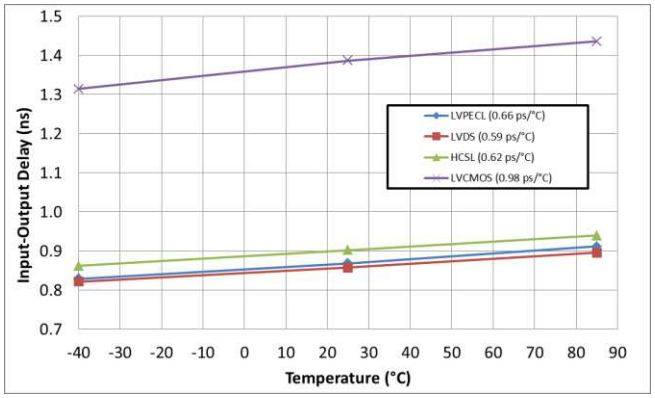

Figure 28. I/O delay vs temperature

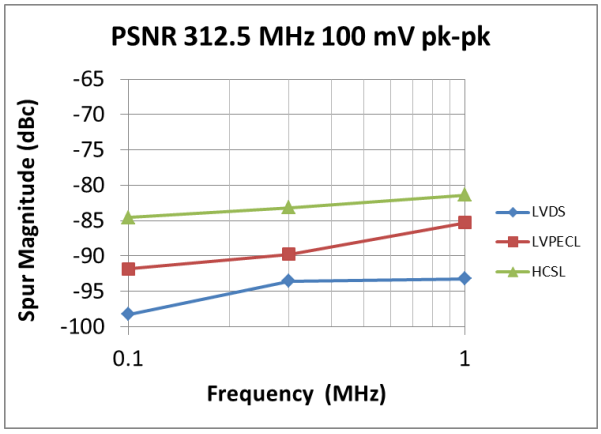

Figure 29. PSNR vs noise frequency

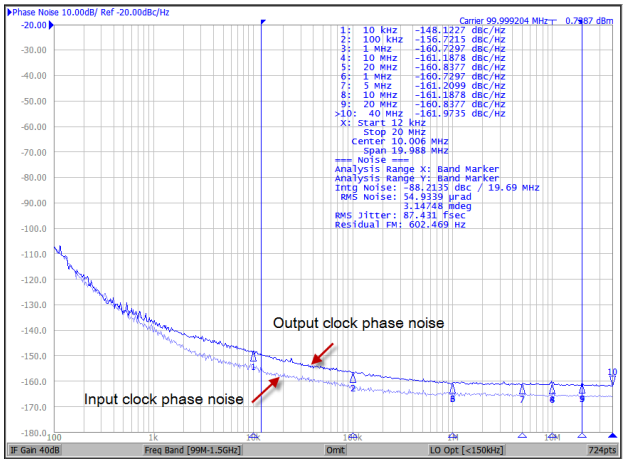

Figure 30. 100MHz LVPECL Phase Noise

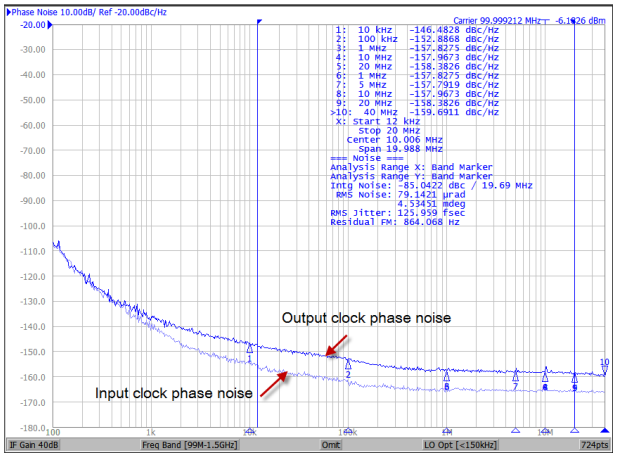

Figure 31. 100MHz LVDS Phase Noise

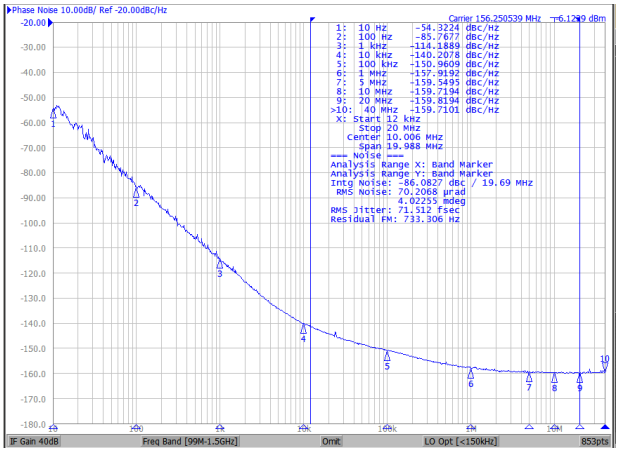

Figure 32. 156.25MHz LVDS Phase Noise in Xtal mode

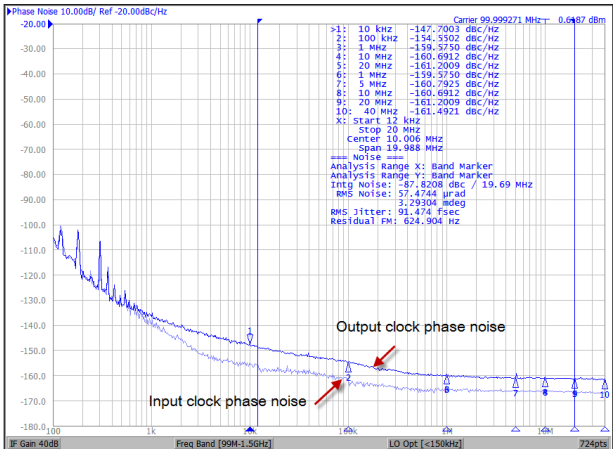

Figure 33. 100MHz HCSL Phase Noise

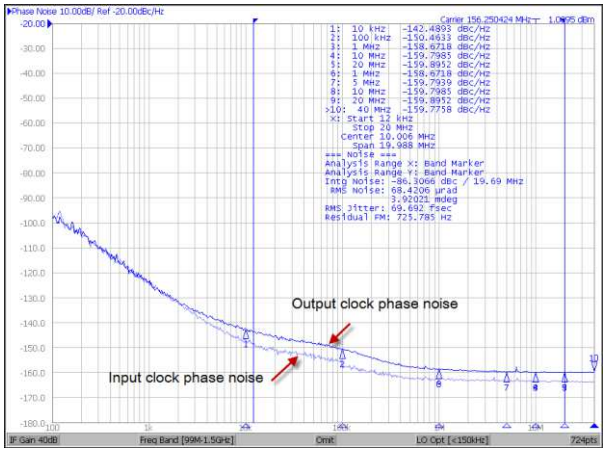

Figure 34. 156.25MHz LVPECL Phase Noise

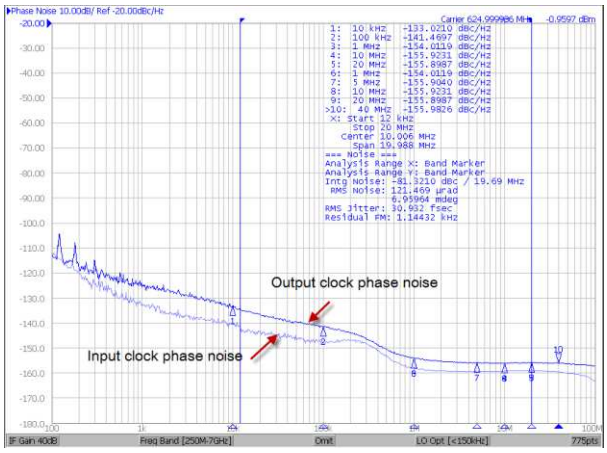

Figure 35. 625MHz LVPECL Phase Noise

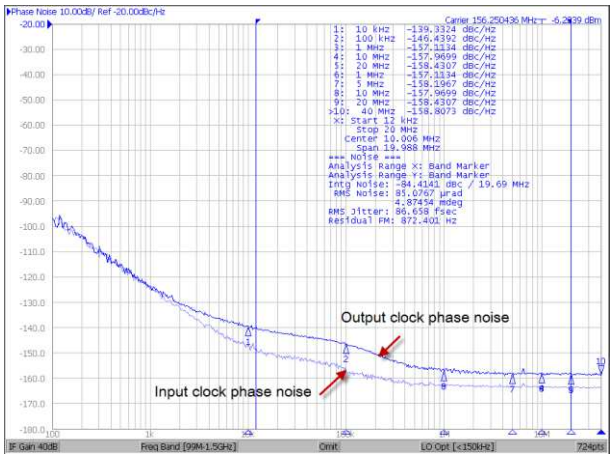

Figure 36. 156.25MHz LVDS Phase Noise

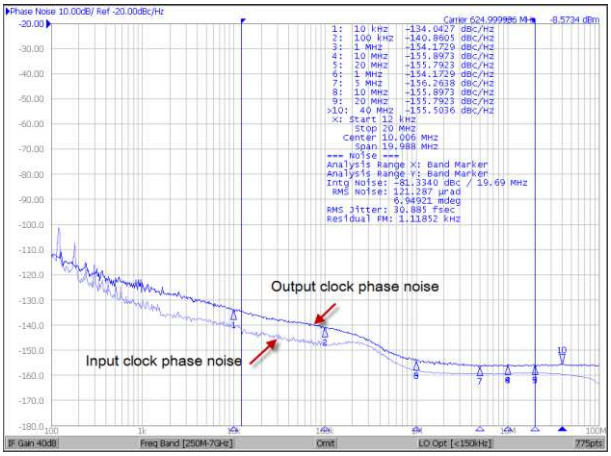

Figure 37. 625MHz LVDS Phase Noise

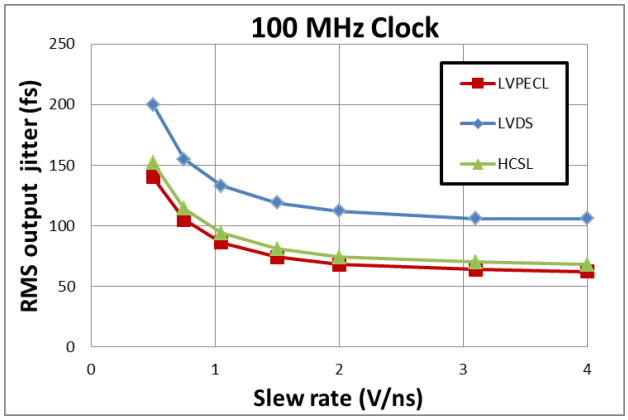

Figure 38. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

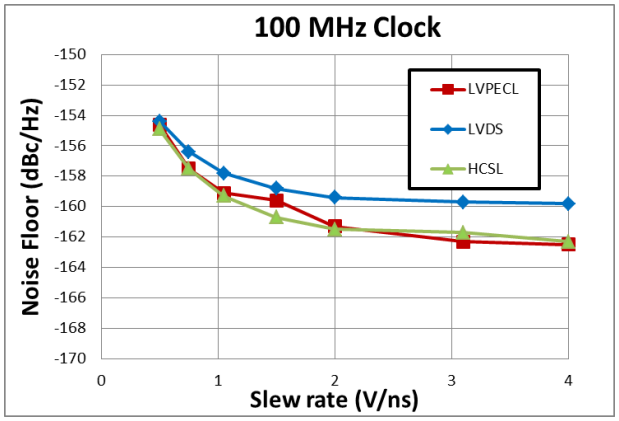

Figure 39. Output clock noise floor vs input clock slew-rate

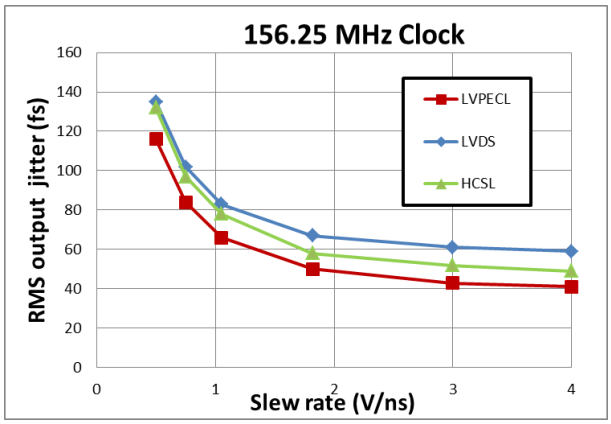

Figure 40. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

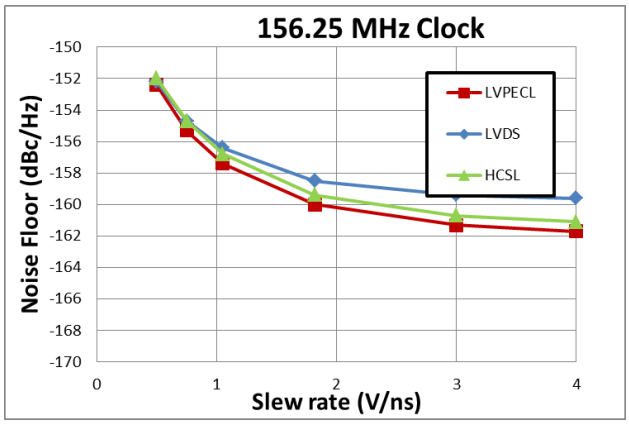

Figure 41. Output clock noise floor vs input clock slew-rate

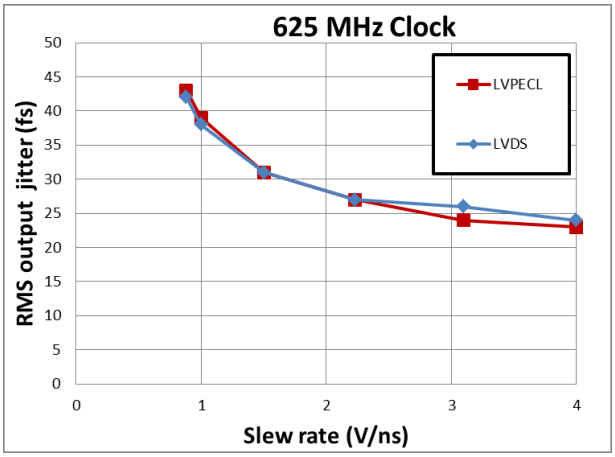

Figure 42. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

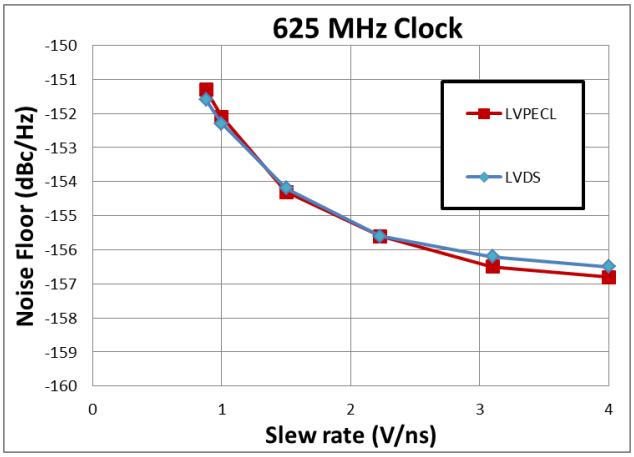

Figure 43. Output clock noise floor vs input clock slew-rate

Register Map

The device is controlled by accessing registers through the serial interface. The following table provides a summary of the registers available for the configuration of the device.

Table 4 Register Map

Address SPI A[6:0] Hex (0x)	Name	Data D[7:0]
00	XTALBG	xtal_buf_gain[7:0]
01	XTALDL	xtal_drive_level[7:0]
02	XTALLC	xtal_load_cap[7:0]
03	XTALNR	xtal_normal_run
04	-	Not used
05	INSEL	input_select[1:0]
06	OUTLOW	output_drive_low
07	DRVTYPEA0	driver_type[7:0] (differential output OUT3, OUT2, OUT1, OUT0)
08	DRVTYPEA1	driver_type[9:8] (differential output OUT4)
09	DRVTYPEB0	driver_type[17:10] (differential output OUT8, OUT7, OUT6, OUT5)
0A	DRVTYPEB1	driver_type[19:18] (differential output OUT9)
0B	CMOSDIV	cmos_div[2:0] (cmos)
0C	CMOSOUTEN	output_enable (cmos)
0D	CMOSDRVSTR	driver_strength (cmos)
0E	-	Not used
0F and 10	Reserved	Leave as default
11	DEVID	Device ID
12 to 1F	Reserved	Leave as default