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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# Low Skew, Low Additive Jitter, 10 output LVPECL/LVDS/HCSL Fanout Buffer with one LVCMOS output

## Features

- 3 to 1 input Multiplexer: Two inputs accept any differential (LVPECL, HCSL, LVDS, SSTL, CML, LVCMOS) or a single ended signal and the third input accepts a crystal or a single ended signal
- Ten differential LVPECL/LVDS/HCSL outputs
- One LVCMOS output
- Ultra-low additive jitter: 24fs (integration band: 12kHz to 20MHz at 625MHz clock frequency)
- Supports clock frequencies from 0 to 1.6GHz
- Supports 2.5V or 3.3V power supplies on LVPECL, LVDS or HCSL outputs
- Supports 1.5V, 1.8V, 2.5V or 3.3V on LVCMOS outputs
- Embedded Low Drop Out (LDO) Voltage regulator provides superior Power Supply Noise Rejection
- Maximum output to output skew of 40ps
- Device controlled via control pins

## Ordering Information

ZL40231LDG1	48 Pin QFN	Trays
ZL40231LDF1	48 pin QFN	Tape and Reel
Package size: 7 x 7 mm		
<b>-40°C to +85°C</b>		

## Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3/4 clock distribution
- Wireless communications
- High performance microprocessor clock distribution
- Test Equipment

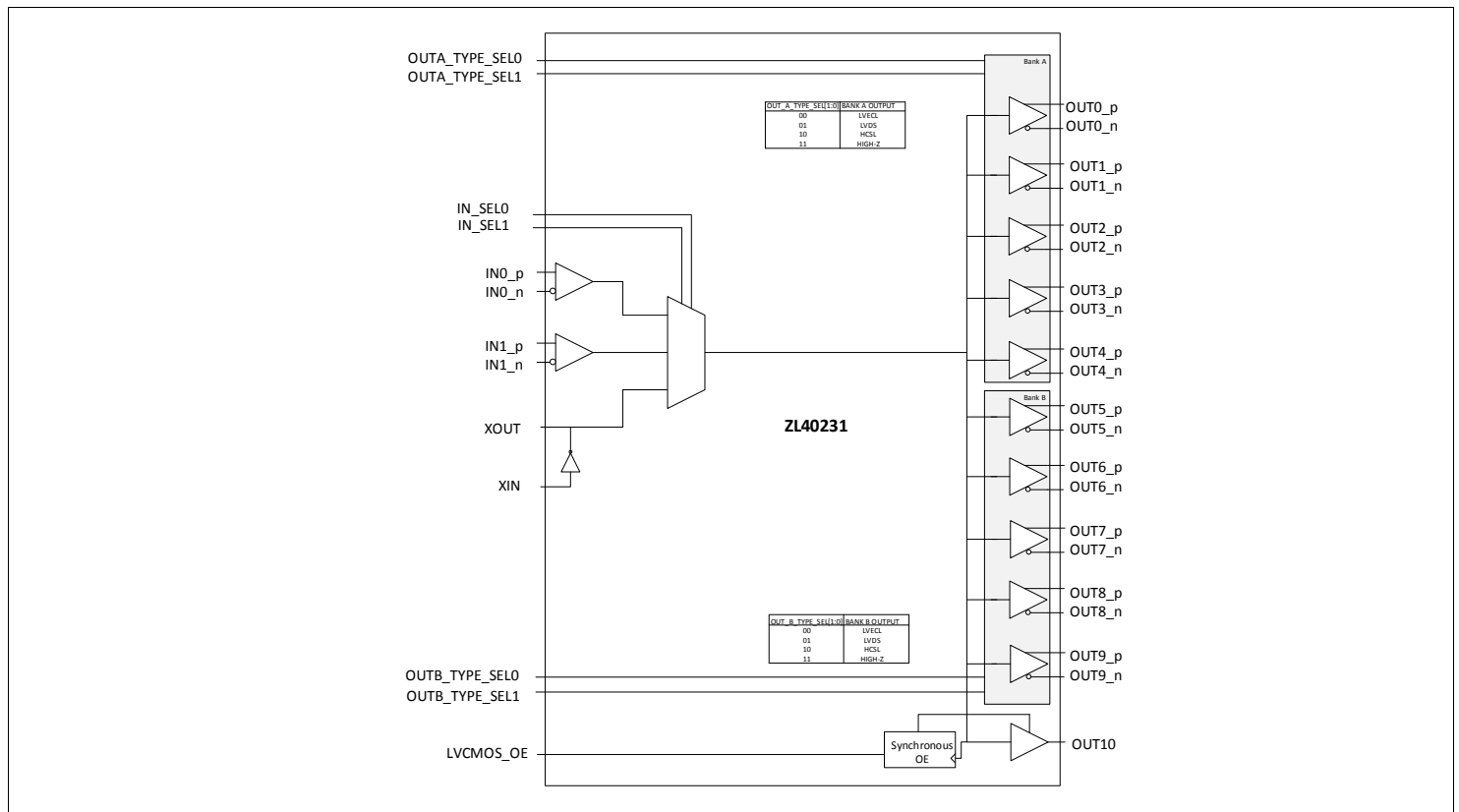


Figure 1. Functional Block Diagram

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# Table of Contents

Features .....	1
Applications .....	1
Table of Contents.....	2
Pin Diagram.....	5
Pin Descriptions.....	6
Functional Description.....	9
Clock Inputs.....	9
Clock Outputs .....	12
Crystal Oscillator Input.....	13
Termination of unused inputs and outputs .....	13
Power Consumption.....	13
Power Supply Filtering .....	14
Power Supplies and Power-up Sequence.....	14
Host Interface .....	15
Typical device performance .....	17
AC and DC Electrical Characteristics .....	21
Absolute Maximum Ratings.....	21
Recommended Operating Conditions.....	21
Change History .....	35
Package Outline .....	36

**List of Figures**

Figure 1.	Functional Block Diagram .....	1
Figure 2.	Pin Diagram .....	5
Figure 3.	Input driven by a single ended output .....	9
Figure 4.	Input driven by DC coupled LVPECL output.....	9
Figure 5.	Input driven by DC coupled LVPECL output (alternative termination) .....	10
Figure 6.	Input driven by AC coupled LVPECL output.....	10
Figure 7.	Input driven by HCSL output .....	10
Figure 8.	Input driven by LVDS output .....	11
Figure 9.	Input driven by AC coupled LVDS .....	11
Figure 10.	Input driven by an SSTL output .....	11
Figure 11.	Termination for LVCMOS output .....	12
Figure 12.	Driving a load via transformer .....	12
Figure 13.	Crystal Oscillator Circuit.....	13
Figure 15.	Output Disable .....	15
Figure 16.	Output Enable .....	16
Figure 17.	156.25MHz LVPECL.....	17
Figure 18.	1.5GHz LVPECL.....	17
Figure 19.	156.25MHz LVDS .....	17
Figure 20.	1.5GHz LVDS .....	17
Figure 21.	100MHz HCSL.....	17
Figure 22.	250MHz HCSL.....	17
Figure 23.	I/O delay vs temperature .....	18
Figure 24.	PSNR vs noise frequency .....	18
Figure 25.	100MHz LVPECL Phase Noise .....	18
Figure 26.	100MHz LVDS Phase Noise .....	18
Figure 27.	25MHz LVDS Phase Noise in Xtal mode .....	18
Figure 28.	100MHz HCSL Phase Noise .....	18
Figure 29.	156.25MHz LVPECL Phase Noise.....	19
Figure 30.	625MHz LVPECL Phase Noise.....	19
Figure 31.	156.25MHz LVDS Phase Noise .....	19
Figure 32.	625MHz LVDS Phase Noise .....	19
Figure 33.	Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate.....	20
Figure 34.	Output clock noise floor vs input clock slew-rate.....	20
Figure 35.	Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate.....	20
Figure 36.	Output clock noise floor vs input clock slew-rate.....	20
Figure 37.	Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate.....	20
Figure 38.	Output clock noise floor vs input clock slew-rate .....	20
Figure 39.	Differential Input Voltage Levels.....	22
Figure 40.	Differential Output Voltage Levels.....	26

**List of Tables**

<i>Table 1 Pin Descriptions</i> .....	6
<i>Table 2 Input clock selection</i> .....	15
<i>Table 3 Output Type Selection</i> .....	15
<i>Table 4 Absolute Maximum Ratings*</i> .....	21
<i>Table 5 Recommended Operating Conditions*</i> .....	21
<i>Table 6 Current consumption</i> .....	21
<i>Table 7 Input Characteristics*</i> .....	22
<i>Table 8 Crystal Oscillator Characteristics*</i> .....	23
<i>Table 9 Power Supply Rejection Ratio for VDD = VDDO = 3.3V*</i> .....	23
<i>Table 10 Power Supply Rejection Ratio for VDD = VDDO = 2.5V*</i> .....	24
<i>Table 11 LVCMOS Output Characteristics for VDDO = 3.3V*</i> .....	24
<i>Table 12 LVCMOS Output Characteristics for VDDO = 2.5V*</i> .....	25
<i>Table 13 LVPECL Output Characteristics for VDDO = 3.3V*</i> .....	26
<i>Table 14 LVPECL Output Characteristics for VDDO = 2.5V*</i> .....	27
<i>Table 15 LVDS Outputs for VDDO = 3.3V*</i> .....	28
<i>Table 16 LVDS Outputs for VDDO = 2.5V*</i> .....	29
<i>Table 17 HCSL Outputs for VDDO = 3.3V*</i> .....	30
<i>Table 18 HCSL Outputs for VDDO = 2.5V*</i> .....	31
<i>Table 24 7x7mm QFN Package Thermal Properties</i> .....	34

## Pin Diagram

The device is packaged in a 7x7mm 48-pin QFN.

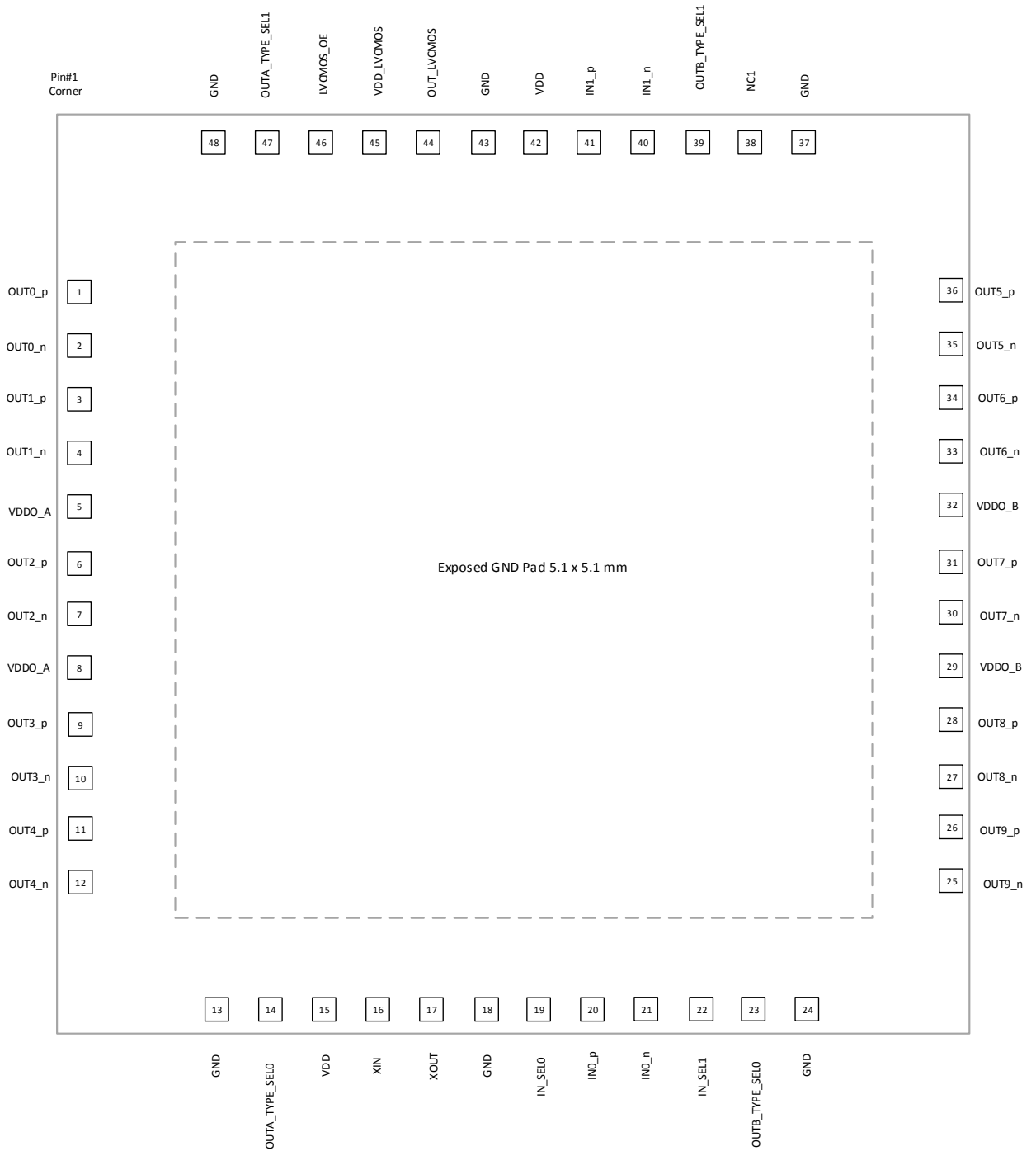


Figure 2. Pin Diagram

## Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I<sub>PU</sub> – input with 300kΩ internal pull-up resistor, I<sub>PD</sub> – input with 300kΩ internal pull-down resistor, I<sub>APU</sub> – input with 31kΩ internal pull-up resistor, I<sub>APD</sub> – input with 30kΩ internal pull-down resistor, I<sub>APU/APD</sub> – input biased to VDD/2 with 60kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/O – Input/Output pin, NC-No connect pin, P – power supply pin.

**Table 1 Pin Descriptions**

#	Name	I/O	Description
<b>Input Reference</b>			
20 21 41 40	IN0_p IN0_n IN1_p IN1_n	I <sub>APD</sub> I <sub>APU/APD</sub> I <sub>APD</sub> I <sub>APU/APD</sub>	<p><b>Input Differential or Single Ended References 0 and 1</b></p> <p>Input frequency range 0Hz to 1.6GHz.</p> <p>Non inverting inputs (_p) are pulled down with internal 30kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60kΩ internal resistors (30kΩ equivalent) to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).</p>
<b>Output Clocks</b>			
1 2 3 4 6 7 9 10 11 12 36 35 34 33 31 30 28 27 26 25	OUT0_p OUT0_n OUT1_p OUT1_n OUT2_p OUT2_n OUT3_p OUT3_n OUT4_p OUT4_n OUT5_p OUT5_n OUT6_p OUT6_n OUT7_p OUT7_n OUT8_p OUT8_n OUT9_p OUT9_n	O	<p><b>Ultra Low Additive Jitter Differential LVPECL/HCSL/LVDS Outputs 0 to 9</b></p> <p>Output frequency range 0 to 1.6GHz</p> <p>Type (LVPECL/HCSL/LVDS/High-Z) of each output bank is controlled via OUTA/B_TYPE_SEL0/1 pins.</p>
44	OUT_LVCMOS	O	<p><b>Ultra Low Additive Jitter LVCMOS Output 0 to 9</b></p> <p>Output frequency range 0 to 250MHz</p>

<b>Control</b>																		
19 22	IN_SELO IN_SEL1	I <sub>PD</sub>	<p><b>Input select pins.</b> Logic level on these pins selects which input will be passed to the output.</p> <table border="1"> <thead> <tr> <th>IN_SEL1</th> <th>IN_SELO</th> <th>OUTN</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Input 0 (IN0)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Input 1 (IN1)</td> </tr> <tr> <td>1</td> <td>X</td> <td>Crystal Oscillator</td> </tr> </tbody> </table>	IN_SEL1	IN_SELO	OUTN	0	0	Input 0 (IN0)	0	1	Input 1 (IN1)	1	X	Crystal Oscillator			
IN_SEL1	IN_SELO	OUTN																
0	0	Input 0 (IN0)																
0	1	Input 1 (IN1)																
1	X	Crystal Oscillator																
14 47	OUTA_TYPE_SELO OUTA_TYPE_SEL1	I <sub>PD</sub>	<p><b>Output Signal for Bank A:</b> Selects Type of the output for Bank A (Outputs 0 to 4)</p> <table border="1"> <thead> <tr> <th>OUTA_TYPE_SEL1</th> <th>OUTA_TYPE_SELO</th> <th>Output 0 to 4</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>LVPECL</td> </tr> <tr> <td>0</td> <td>1</td> <td>LVDS</td> </tr> <tr> <td>1</td> <td>0</td> <td>HCSL</td> </tr> <tr> <td>1</td> <td>1</td> <td>High-Z (Disabled)</td> </tr> </tbody> </table>	OUTA_TYPE_SEL1	OUTA_TYPE_SELO	Output 0 to 4	0	0	LVPECL	0	1	LVDS	1	0	HCSL	1	1	High-Z (Disabled)
OUTA_TYPE_SEL1	OUTA_TYPE_SELO	Output 0 to 4																
0	0	LVPECL																
0	1	LVDS																
1	0	HCSL																
1	1	High-Z (Disabled)																
23 39	OUTB_TYPE_SELO OUTB_TYPE_SEL1	I/O	<p><b>Output Signal for Bank B:</b> Selects Type of the output for Bank B (Outputs 5 to 9)</p> <table border="1"> <thead> <tr> <th>OUTB_TYPE_SEL1</th> <th>OUTB_TYPE_SELO</th> <th>Output 5 to 9</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>LVPECL</td> </tr> <tr> <td>0</td> <td>1</td> <td>LVDS</td> </tr> <tr> <td>1</td> <td>0</td> <td>HCSL</td> </tr> <tr> <td>1</td> <td>1</td> <td>High-Z (Disabled)</td> </tr> </tbody> </table>	OUTB_TYPE_SEL1	OUTB_TYPE_SELO	Output 5 to 9	0	0	LVPECL	0	1	LVDS	1	0	HCSL	1	1	High-Z (Disabled)
OUTB_TYPE_SEL1	OUTB_TYPE_SELO	Output 5 to 9																
0	0	LVPECL																
0	1	LVDS																
1	0	HCSL																
1	1	High-Z (Disabled)																
46	LVC MOS_OE	I	<p><b>Output enable for LVC MOS outputs:</b> When high LVC MOS output is enabled. When low LVC MOS output is High-Z</p>															
<b>Crystal Oscillator</b>																		
16	XIN	I	<b>Crystal Oscillator Input or crystal bypass mode or crystal overdrive mode</b>															
17	XOUT	O	<b>Crystal Oscillator Output</b>															



<b>No Connect</b>			
38	NC1	NC	<b>No Connects (not connected to the die)</b> Leave unconnected or connect to GND for mechanical support
<b>Power and Ground</b>			
15 42	VDD	P	<b>Positive Supply Voltage.</b> Connect to 3.3V or 2.5V supply.
5 8	VDDO_A	P	<b>Positive Supply Voltage for Differential Outputs Bank A</b> Connect 3.3V or 2.5V power supply. VDDO_A does not have to be connected to the same voltage level as VDD or VDDO_B. These pins power up differential outputs OUT[0:4]_p/n.
29 32	VDDO_B		<b>Positive Supply Voltage for Differential Outputs Bank B</b> Connect 3.3V or 2.5V power supply. VDDO_B does not have to be connected to the same voltage level as VDD or VDDO_A. These pins power up differential outputs OUT[5:9]_p/n.
45	VDD_LVCMOS	P	<b>Power Supply Voltage for LVCMOS Output</b> Connect to 3.3V, 2.5V, 1.8V or 1.5V power supply
13 18 24 43 37 48	GND	P	<b>Ground</b> Connect to the ground
E-Pad	GND	P	<b>Ground.</b> Connect to the ground

### Functional Description

The ZL40231 is a low additive jitter, low power 3 x 10 LVPECL/HCSL/LVDS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML ) or single ended ( LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins.

The ZL40231 has ten LVPECL/HCSL/LVDS outputs which can be powered from 3.3V or 2.5V supply. Each output bank (A and B) can be independently set to be LVPECL, LVDS, HCSL or Hi-Z via control OUTA/B\_TYPE\_SEL0/1 pins.

The control inputs: OUTA/B\_TYPE\_SEL0/1 and IN\_SEL0/1 have low input threshold voltage so they can be driven from a device with low I/O voltage (down to 1.2V).

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

### Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40231 inputs.

Figure 3 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each and  $R_o + R_s$  should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor  $R_s$  should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 7). The source resistors of  $R_s = 270\Omega$  could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of  $(3.3V/2) * (1/(270\Omega + 50\Omega)) = 5.16mA$ .

For optimum performance both differential input pins ( $\_p$  and  $\_n$ ) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

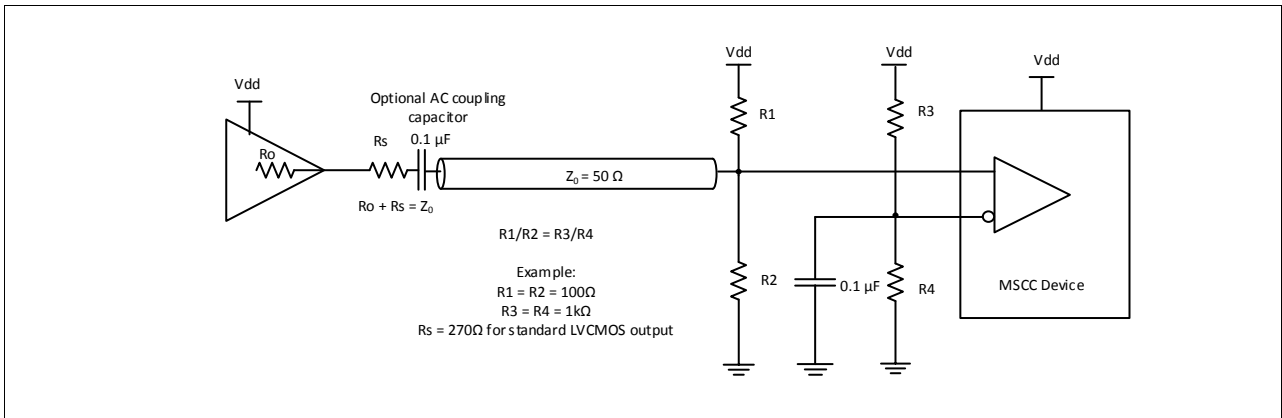


Figure 3. Input driven by a single ended output

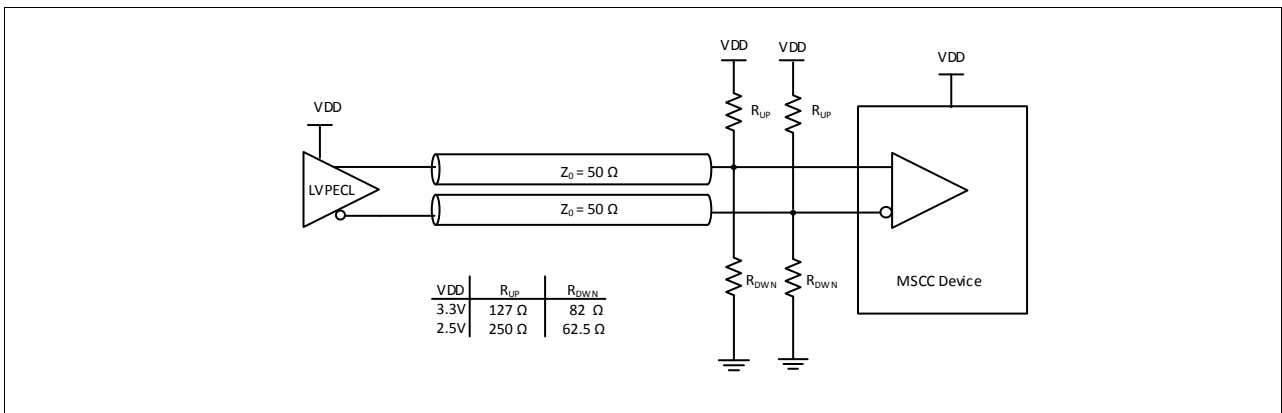


Figure 4. Input driven by DC coupled LVPECL output

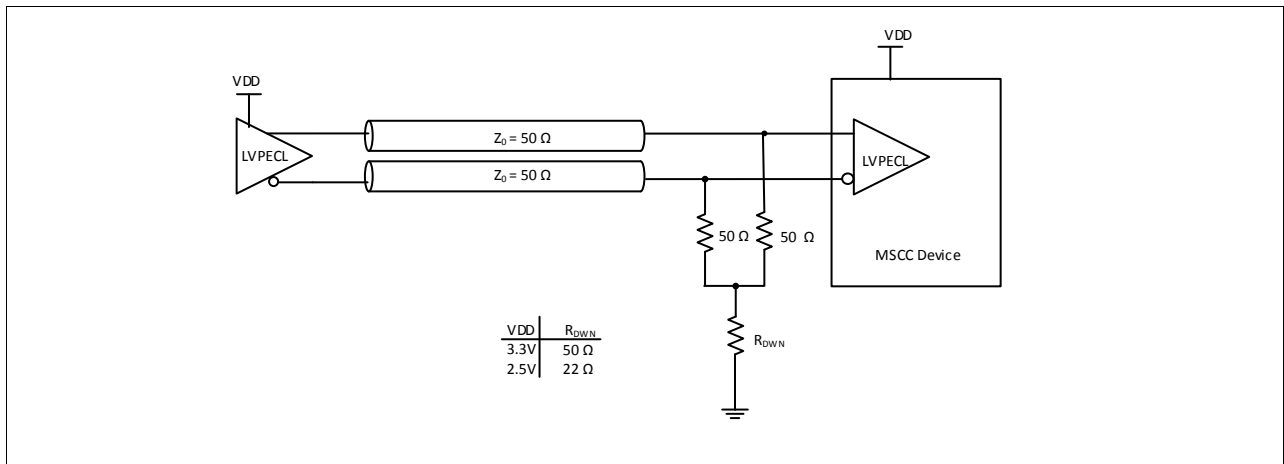


Figure 5. Input driven by DC coupled LVPECL output (alternative termination)

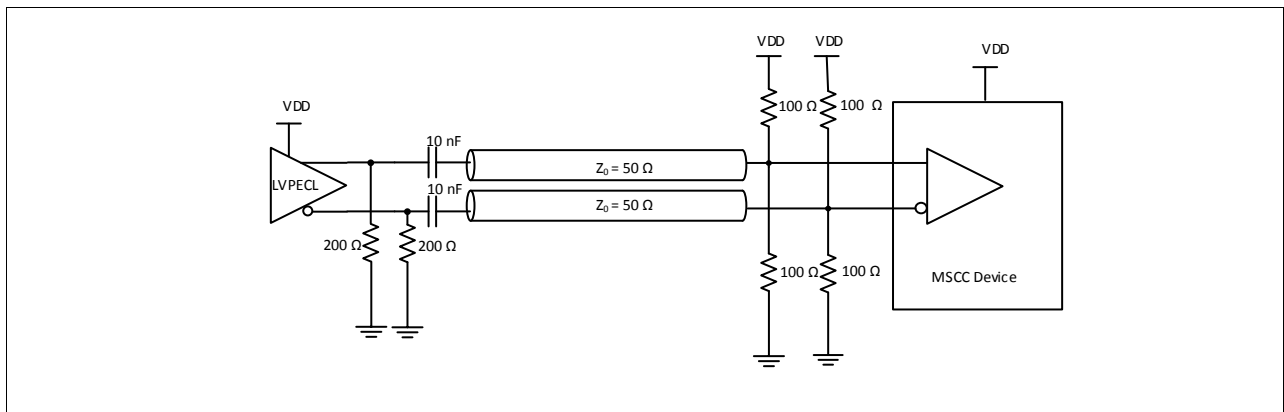


Figure 6. Input driven by AC coupled LVPECL output

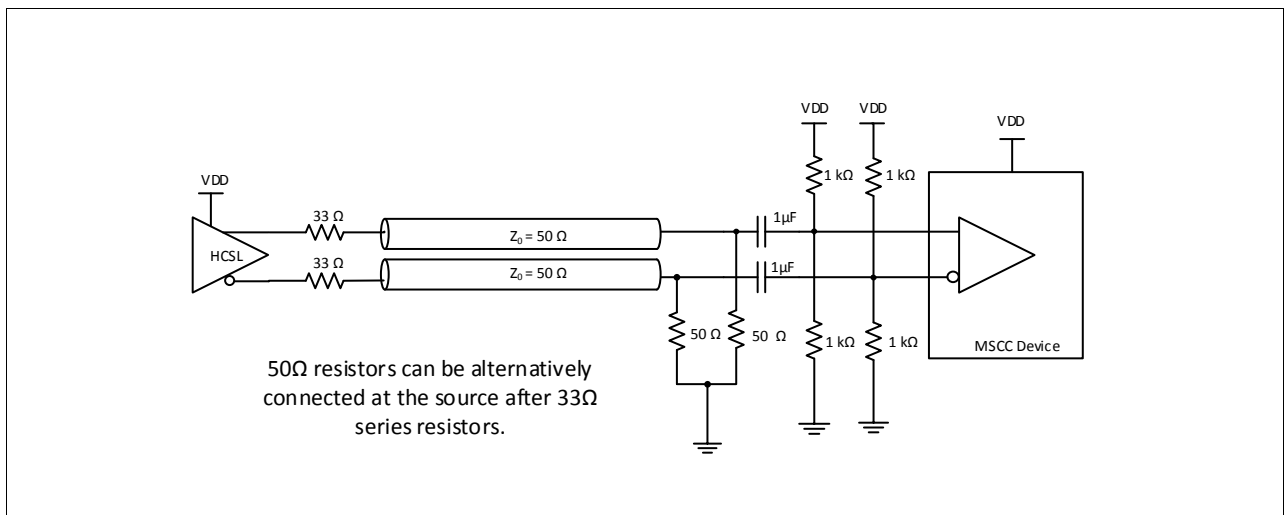


Figure 7. Input driven by HCSL output

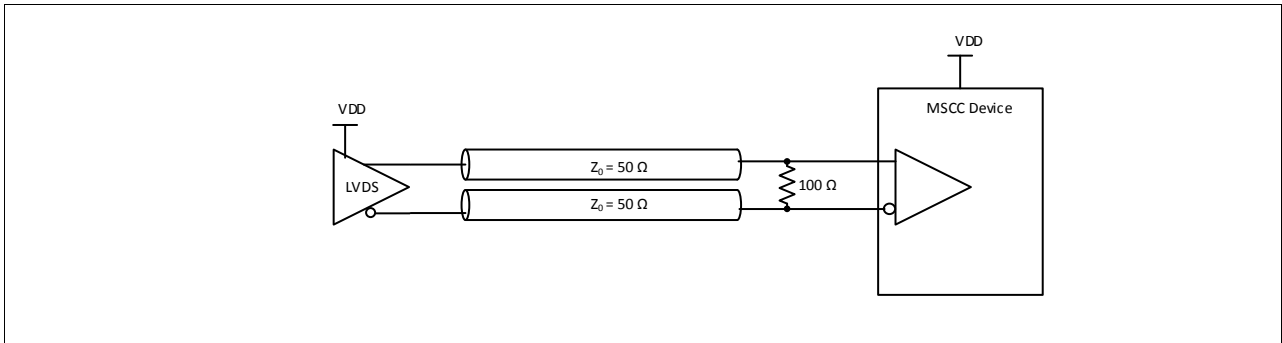


Figure 8. Input driven by LVDS output

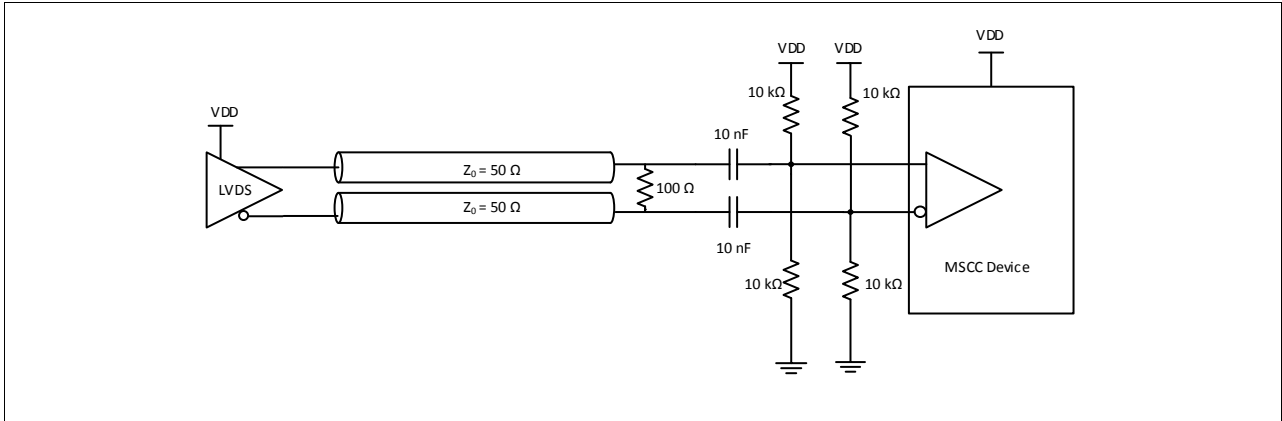


Figure 9. Input driven by AC coupled LVDS

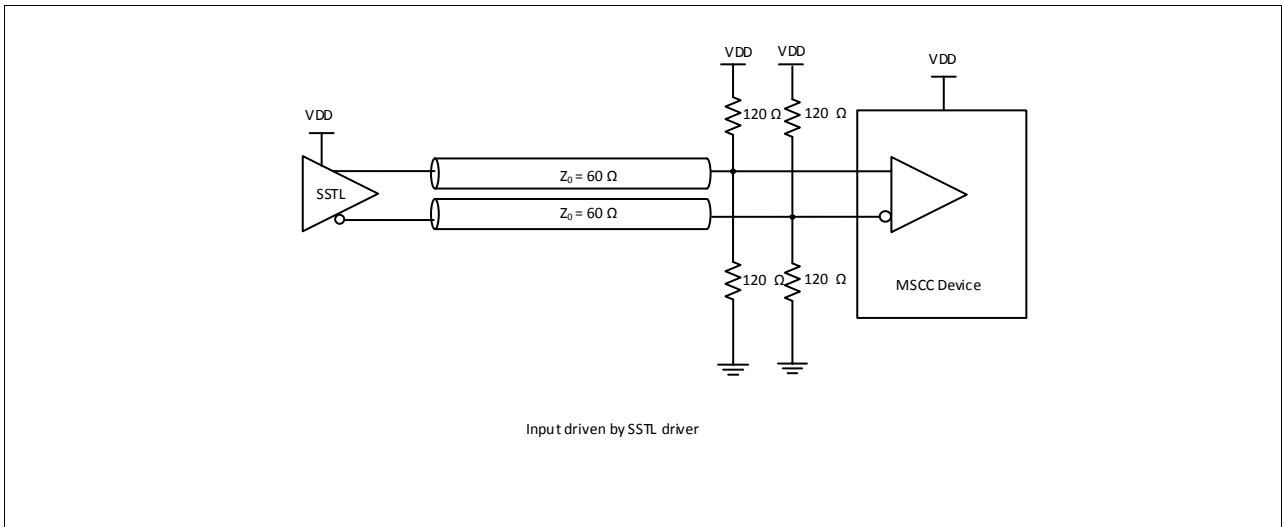
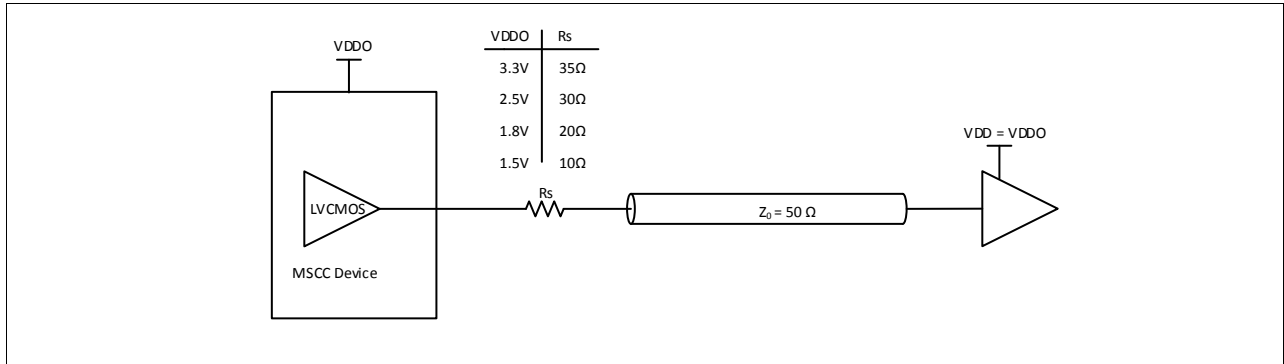


Figure 10. Input driven by an SSTL output

## Clock Outputs

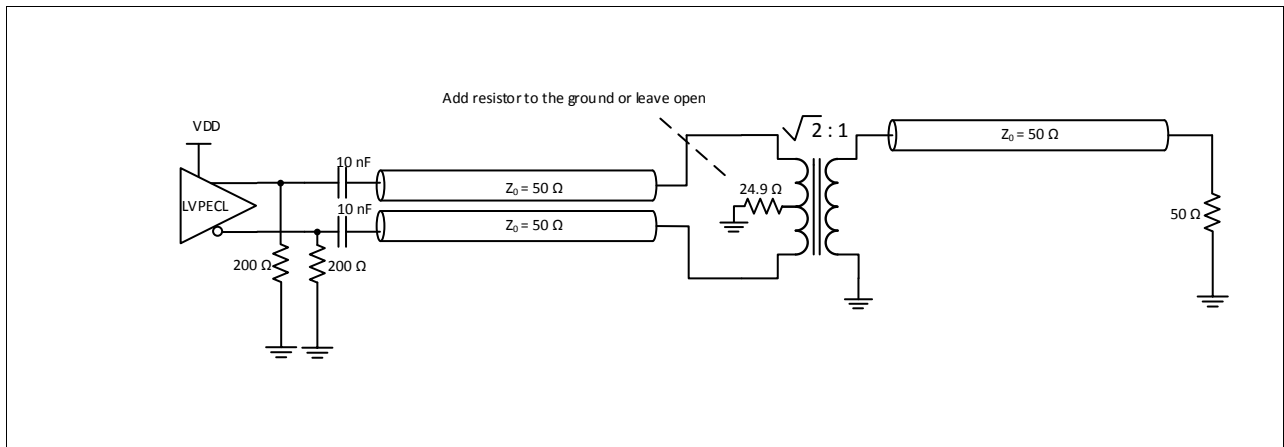
LVC MOS output OUT10 require only series termination resistor whose value is depending on LVC MOS output voltage as shown in Figure 11.



**Figure 11. Termination for LVC MOS output**

Differential outputs LVPECL and LVDS should have same termination as corresponding outputs described in previous section. HCSL outputs should be terminated with 33Ω series resistors at the source and 50Ω shunt resistors at the source or at the end on the transmission line. AC coupling and re-biasing is not required at the outputs when driving native HCSL receivers.

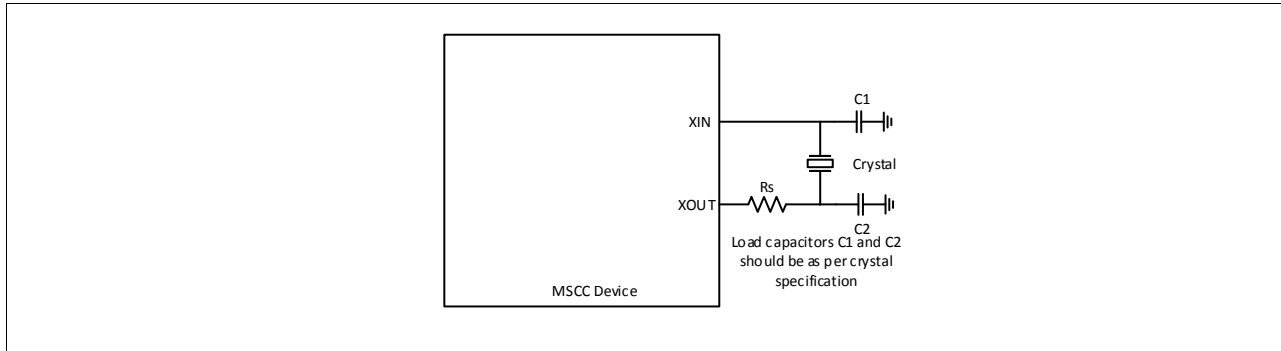
The device is designed to drive differential input of semiconductor devices. In applications that use a transformer to convert from the differential to the single ended output (for example driving an oscilloscope 50Ω input), a resistor larger than 10Ω should be added at the center tap of the primary winding to achieve optimum jitter performance as shown in Figure 12. This is to provide a nominal common mode impedance of 10Ω or higher which is typical for differential terminations.



**Figure 12. Driving a load via transformer**

## Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8MHz to 60MHz. Load capacitors C1, C2 and series resistor Rs shall be selected as per crystal vendor recommendation. Shunt resistor is implemented inside the device.



**Figure 13. Crystal Oscillator Circuit**

## Termination of unused inputs and outputs

Unused inputs can be left unconnected or alternatively IN\_0/1 can be pulled-down by 1kΩ resistor. Unused outputs should be left unconnected.

## Power Consumption

The device total power consumption can be calculated as:

$$P_T = P_S + P_{XTAL} + P_C + P_{O\_DIF} + P_{O\_LVCMOS}$$

Where:

$$P_S = V_{DD} \times I_S$$

The core power when XTAL is not used. The current is specified in Table 6. If XTAL is running this power should be set to zero.

$$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$$

The core power when XTAL is used. The current is provided in Table 6. If XTAL is not used this power should be set to zero.

$$P_C = V_{DDO} \times I_{DD\_CM}$$

Common output power shared among all ten outputs. The current  $I_{DD\_CM}$  is specified Table 6.

$$P_{O\_DIF} = V_{DDO} \times I_{DD\_LVDS} \times N$$

Output power where output current ( $I_{DD\_LVDS}$ ) is specified in Table 6. For LVPECL or HCSL just replace  $I_{DD\_LVDS}$  with  $I_{DD\_LVPECL}$  or  $I_{DD\_HCSL}$ . N is the number of enabled differential outputs and it can be either: 0, 5 or 10.

$$P_{O\_LVCMOS} = V_{DD\_LVCMOS} \times (I_{DD} \times f / 100MHz) + V_{DD\_LVCMOS} \times C_{LOAD} \times f)$$

Dynamic LVCMOS output power.  $I_{DD}$  is specified in Table 6. If LVCMOS output is disabled this term is equal to zero.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption.

$$P_D = P_T - N_1 \times P_{LVPECL} - N_2 \times P_{LVDS} - N_3 \times P_{HCSL}$$

Where  $N_1$ ,  $N_2$  and  $N_3$  are the number of enabled LVPECL, LVDS and HCSL outputs respectively. When both banks are enabled  $N_1 + N_2 + N_3 = 10$  and one or two of  $N_1$ ,  $N_2$  and  $N_3$  will equal to 0.

$$P_{LVPECL} = (V_{OH} - V_B)^2 / 50\Omega + (V_{OL} - V_B)^2 / 50\Omega + (V_{OH} - V_B) \times V_B / 50\Omega + (V_{OL} - V_B) \times V_B / 50\Omega$$

$V_{OH}$  and  $V_{OL}$  are the output high and low voltages respectively for LVPECL output

$V_B$  is LVPECL bias voltage equal to  $V_{DD} - 2V$

$$P_{LVDS} = V_{SW}^2 / 100\Omega$$

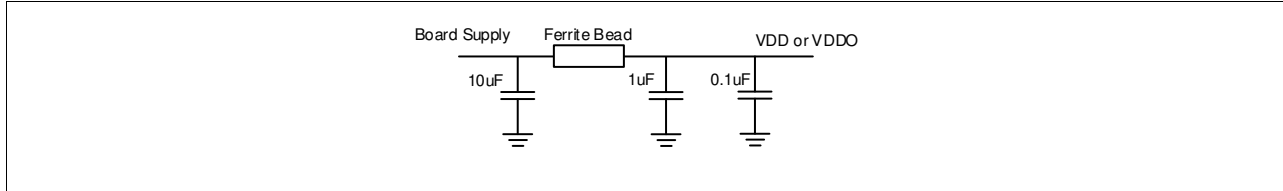
$V_{sw}$  is voltage swing of LVDS output.

$$P_{HCSL} = (V_{SW} / 50\Omega)^2 \times (33\Omega + 50\Omega)$$

$V_{sw}$  is voltage swing of HCSL output.  $50\Omega$  is termination resistance and  $33\Omega$  is series resistance of the HCSL output.

### Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with  $0.1\mu F$  capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulated with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling for each power pin.



**Figure 14. Power Supply Filtering**

### Power Supplies and Power-up Sequence

The device has four different power supplies: VDD, VDDO\_A, VDDO\_B and VDD\_LVCMOS which are mutually independent. Voltages supported by each of these power supplies are specified in Table 1.

The device is not sensitive to the power-up sequence. For example commonly used sequence where higher voltage comes up before or at the same time as the lower voltages can be used (or any other sequence).

## Host Interface

ZL40231 is controlled via Input Select (IN\_SEL0/1) pins which select which one of three inputs is fed to the output and show in Table 2 and OUTA/B\_TYPE\_SEL0/1 pins which select signal level (LVPECL, LVDS, HCSL or Hi-Z) for each of two (A and B) output banks as shown in Table 3.

All input control pins have low input threshold voltage so they can be driven from the device with low output voltage (FPGA/CPLD). Supported voltages are between 1.2V and VDD (2.5V or 3.3V).

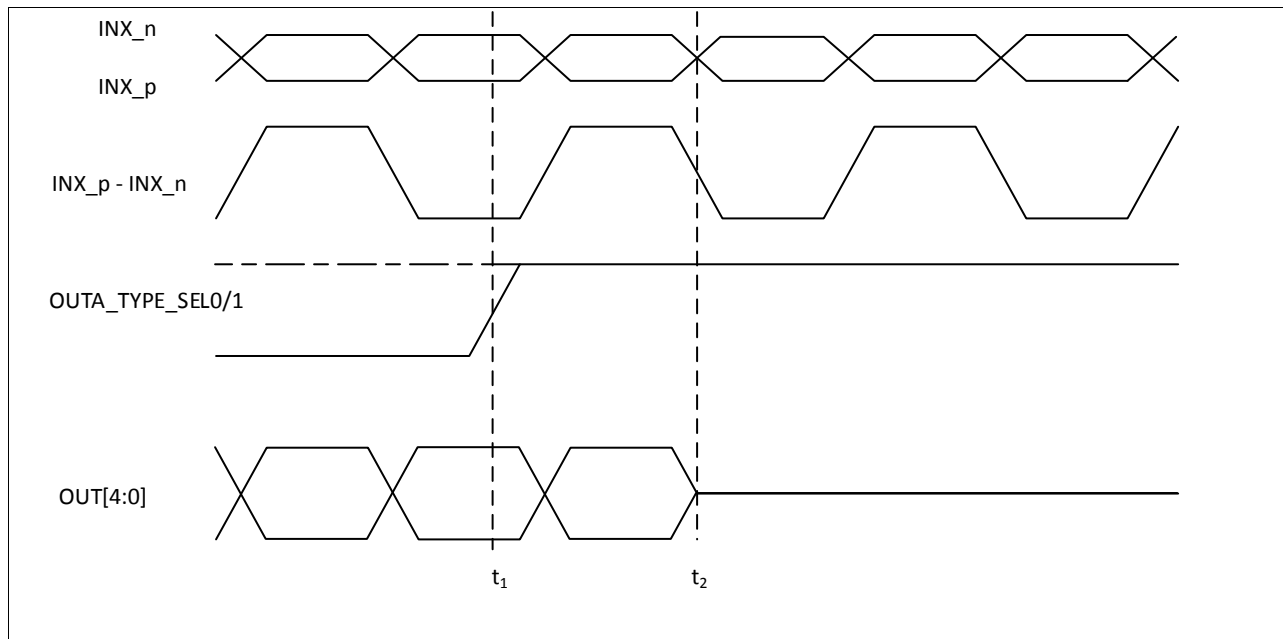
**Table 2 Input clock selection**

IN_SEL1	IN_SEL0	Selected Input
0	0	IN0_p, IN0_n
0	1	IN1_p, IN1_n
1	X	XIN

**Table 3 Output Type Selection**

OUTA/B_TYPE_SEL1	OUTA/B_TYPE_SEL0	Output
0	0	LVPECL
1	1	LVDS
1	0	HCSL
1	1	High-Z (Output Disabled)

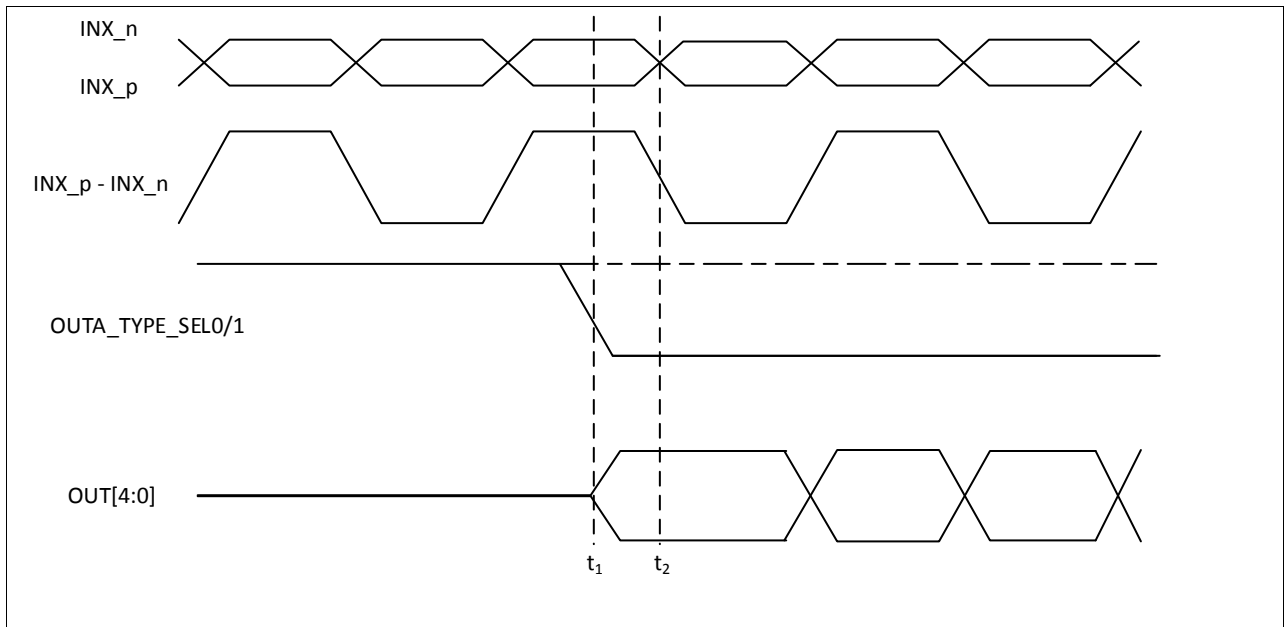
Output is disabled synchronously on the falling edge of the input ( $t_2$ ) as shown in Figure 15.



**Figure 15. Output Disable**

Outputs can be enabled by toggling one or both OUTA/B\_TYPE\_SEL0/1 pins low depending on which type of interface needs to be enabled for particular bank. As soon as one or both OUTA/B\_TYPE\_SEL0/1 pins go low ( $t_1$ ) the outputs will go from high-Z to low (OUTX\_p = low, OUTx\_n = high) and will start to track the input after the first falling edge ( $t_2$ ) of the input signal as shown in Figure 16.



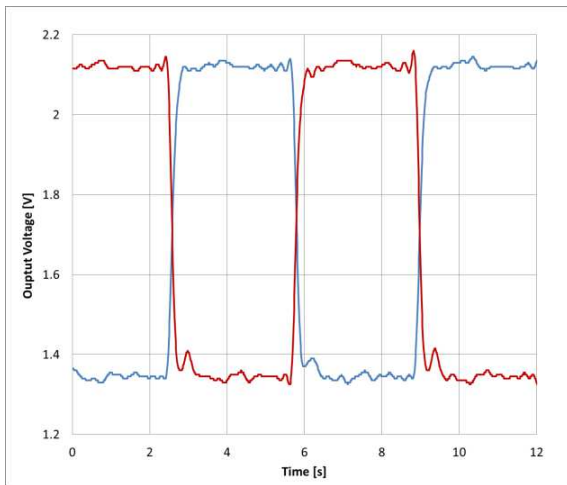


**Figure 16. Output Enable**

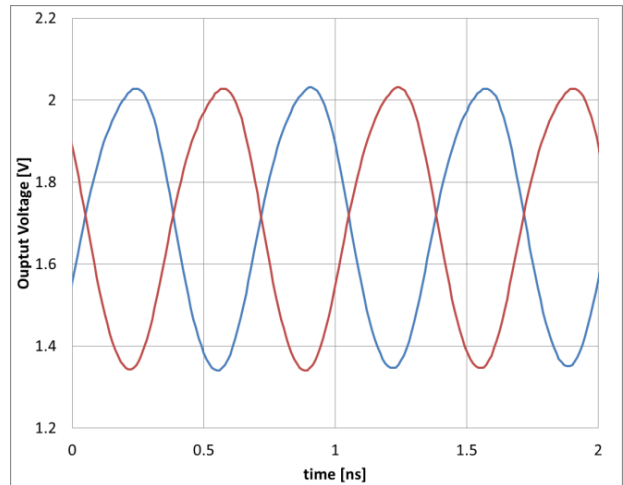
Figures above show enable/disable waveform for the output bank A (OUT[4:0]). The waveforms are equivalent for the output bank B (OUT[9:5]) which is controlled by OUTB\_TYPE\_SEL0/1 pins.

## Typical device performance

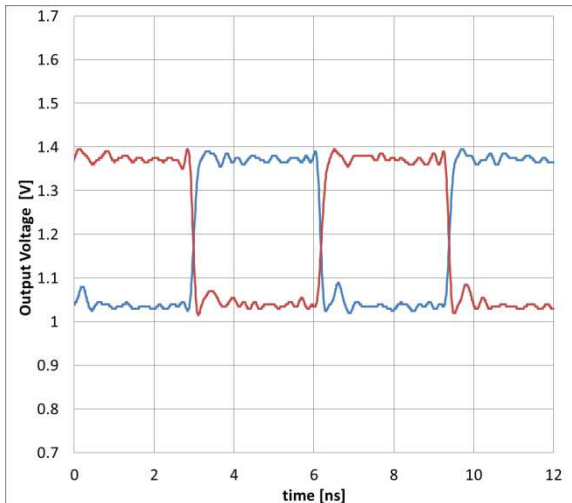
The following plots show typical device performances



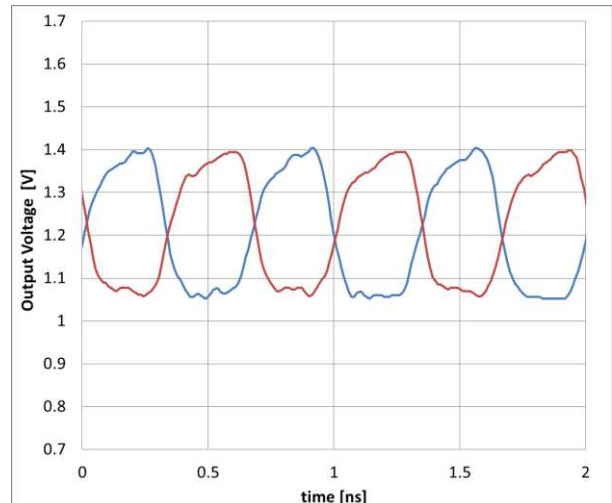
**Figure 17. 156.25MHz LVPECL**



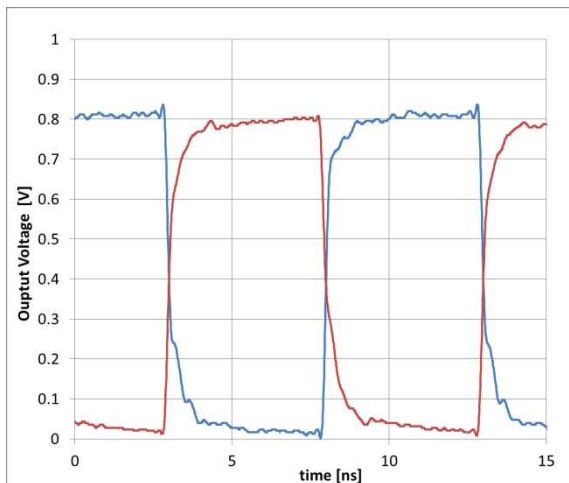
**Figure 18. 1.5GHz LVPECL**



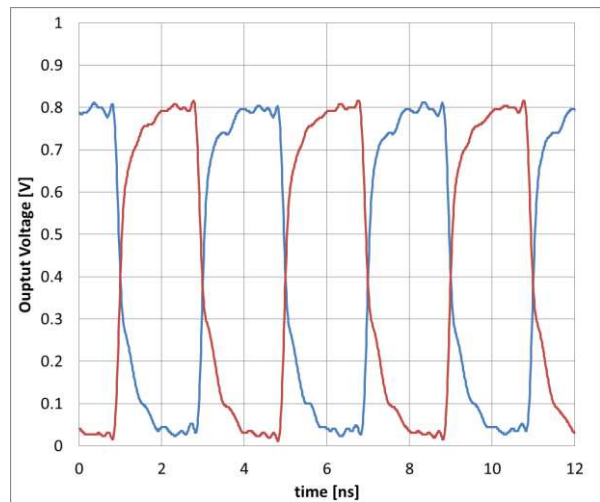
**Figure 19. 156.25MHz LVDS**



**Figure 20. 1.5GHz LVDS**



**Figure 21. 100MHz HCSSL**



**Figure 22. 250MHz HCSSL**

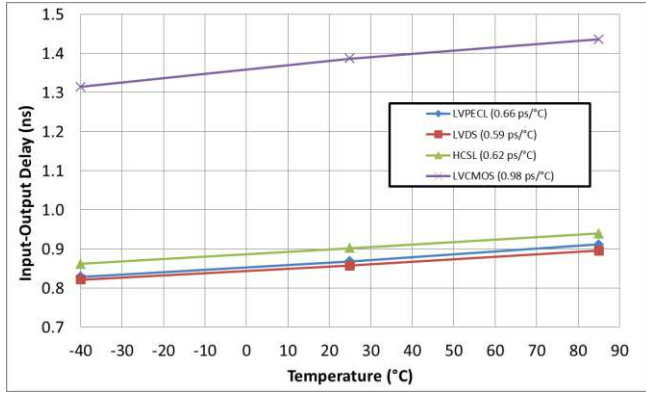


Figure 23. I/O delay vs temperature

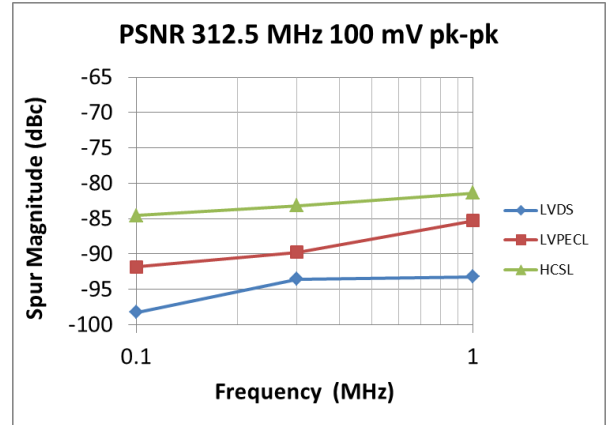


Figure 24. PSNR vs noise frequency

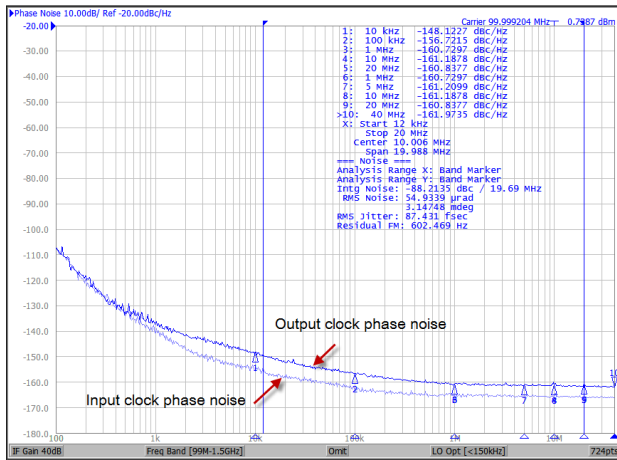


Figure 25. 100MHz LVPECL Phase Noise

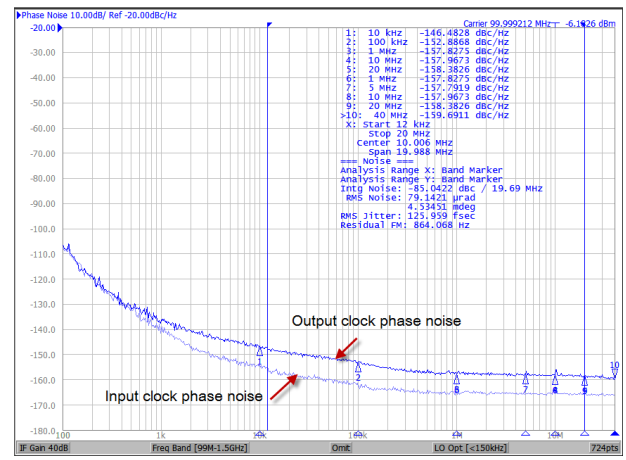


Figure 26. 100MHz LVDS Phase Noise

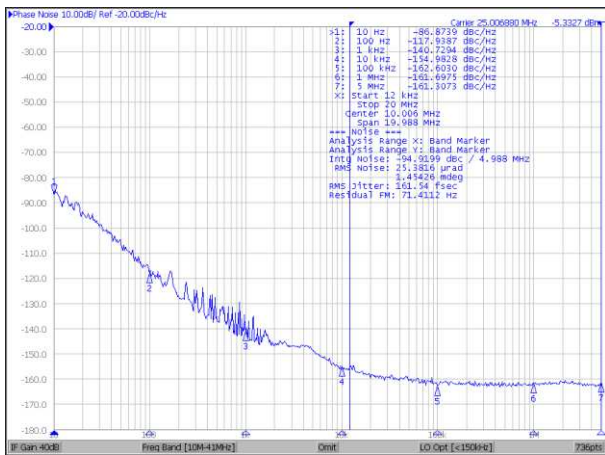


Figure 27. 25MHz LVDS Phase Noise in Xtal mode

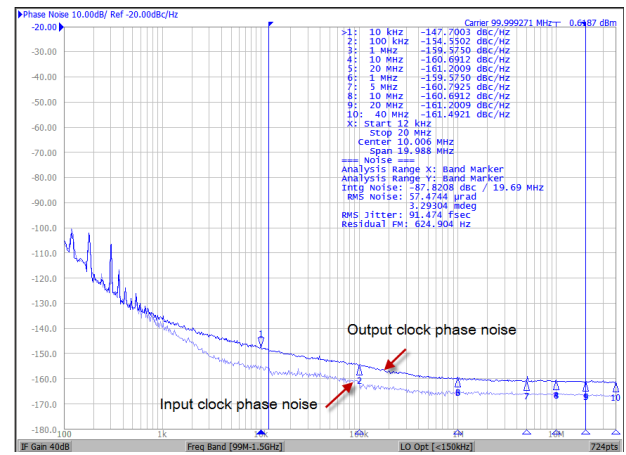


Figure 28. 100MHz HCSL Phase Noise

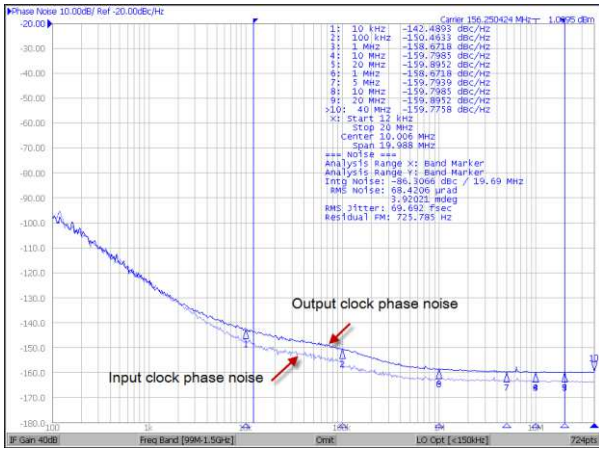


Figure 29. 156.25MHz LVPECL Phase Noise

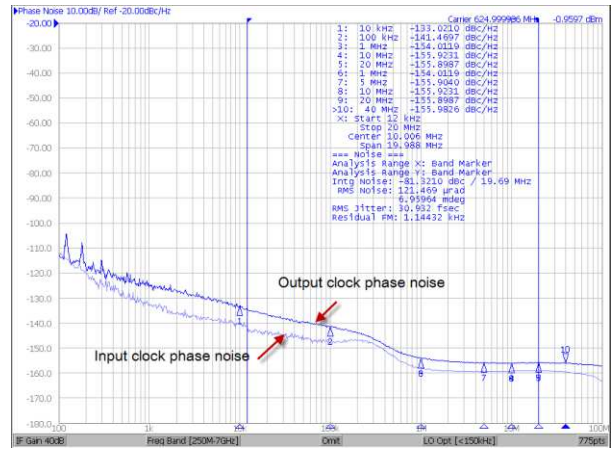


Figure 30. 625MHz LVPECL Phase Noise

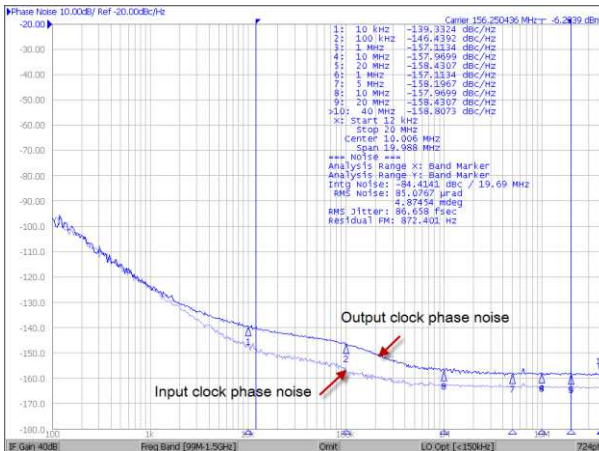


Figure 31. 156.25MHz LVDS Phase Noise

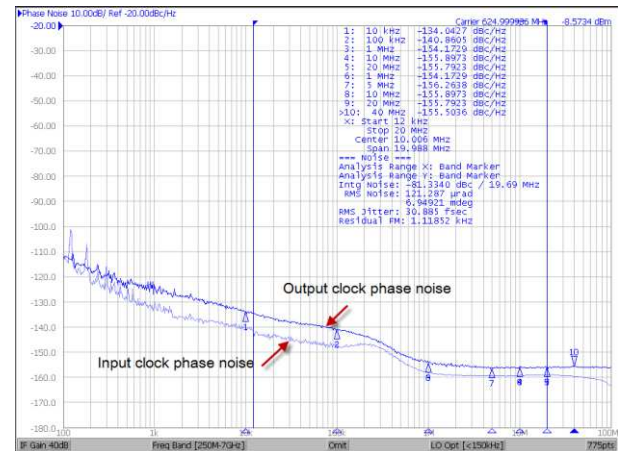


Figure 32. 625MHz LVDS Phase Noise

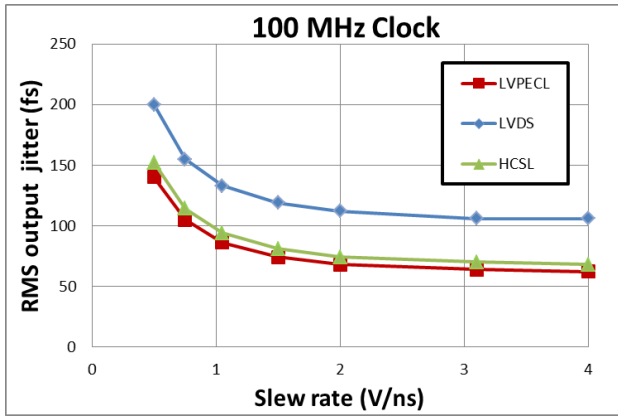


Figure 33. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

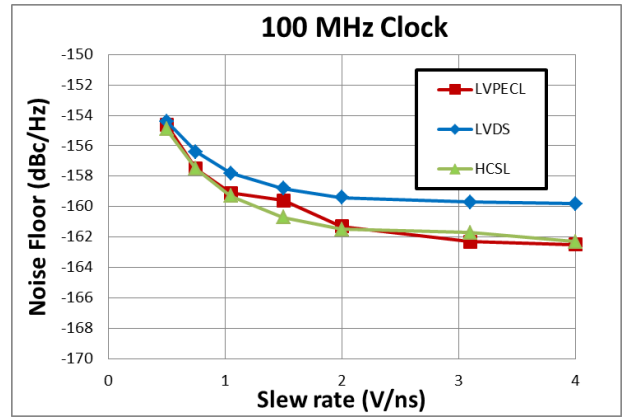


Figure 34. Output clock noise floor vs input clock slew-rate

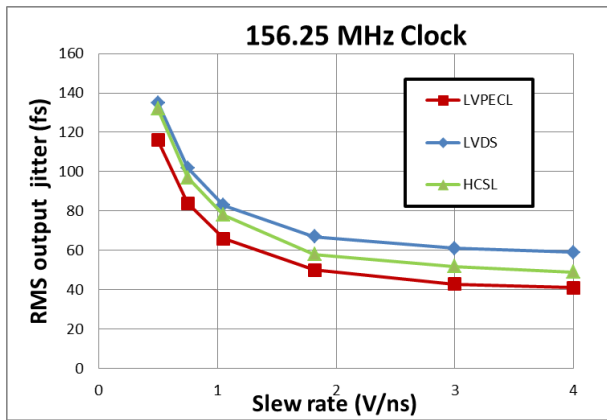


Figure 35. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

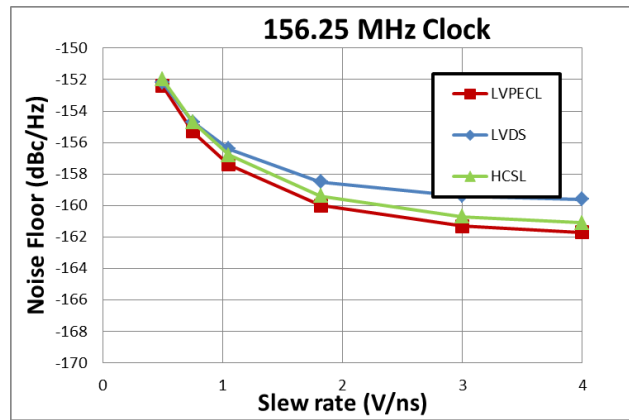


Figure 36. Output clock noise floor vs input clock slew-rate

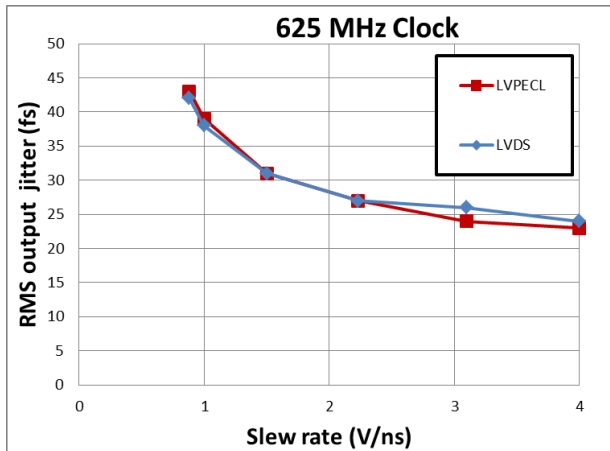


Figure 37. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

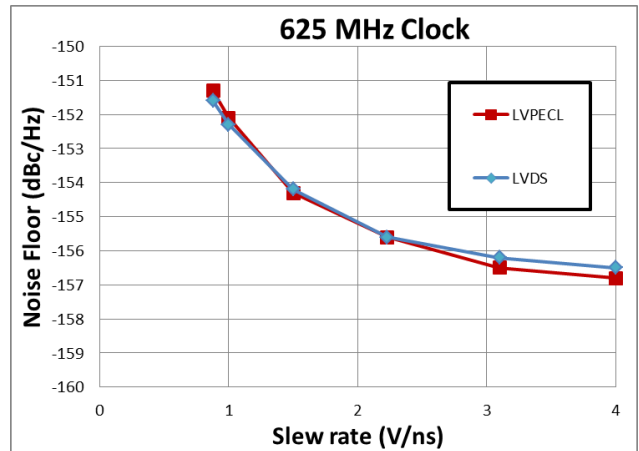


Figure 38. Output clock noise floor vs input clock slew-rate

## AC and DC Electrical Characteristics

### Absolute Maximum Ratings

**Table 4 Absolute Maximum Ratings\***

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage (3.3V)	V <sub>DD</sub> /V <sub>DDO</sub>	-0.5		4.6	V	
2	Supply voltage (2.5V)	V <sub>DD</sub> /V <sub>DDO</sub>	-0.5		3.5	V	
3	Storage temperature	T <sub>ST</sub>	-55		125	°C	

\* Exceeding these values may cause permanent damage

\* Functional operation under these conditions is not implied

\* Voltages are with respect to ground (GND) unless otherwise stated

### Recommended Operating Conditions

**Table 5 Recommended Operating Conditions\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	V <sub>DD</sub> /V <sub>DDO</sub> /V <sub>DD,LVCMOS</sub>	3.135	3.30	3.465	V	
2	Supply voltage 2.5V	V <sub>DD</sub> /V <sub>DDO</sub> /V <sub>DD,LVCMOS</sub>	2.375	2.50	2.625	V	
3	Supply voltage 1.8V	V <sub>DD,LVCMOS</sub>	1.6	1.8V	2	V	
4	Supply voltage 1.5V	V <sub>DD,LVCMOS</sub>	1.35	1.5	1.65	V	
5	Operating temperature	T <sub>A</sub>	-40	25	85	°C	
6	Input voltage	V <sub>DD-IN</sub>	- 0.3		V <sub>DD</sub> + 0.3	V	

\* Voltages are with respect to ground (GND) unless otherwise stated

\* The device core supports two power supply modes (3.3V and 2.5V)

**Table 6 Current consumption**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Core device current (all outputs and XTAL disabled)	I <sub>s,3.3V</sub>		163	197	mA	VDD= 3.3V+5%
		I <sub>s,2.5V</sub>		153	187	mA	VDD = 2.5V+5%
2	Core device current (all outputs disabled) XTAL circuit enabled with 25MHz Crystal connected between XIN and XOUT	I <sub>DD,XTAL_3.3V</sub>		128	154	mA	VDD= 3.3V+5%
		I <sub>DD,XTAL_2.5V</sub>		124	150	mA	VDD= 2.5V+5%
3	Common output current	I <sub>DD,CM_3.3V</sub>		13.44	15.05	mA	VDDO= 3.3V+5%
		I <sub>DD,CM_2.5V</sub>		12.18	13.65	mA	VDDO= 2.5V+5%
4	Dynamic LVCMOS output current (f = 100MHz) Needs to be scaled for different frequencies by f/100MHz	I <sub>DD,3.3V</sub>		2.38	2.68	mA	VDDO= 3.3V+5%
		I <sub>DD,2.5V</sub>		1.74	1.96	mA	VDDO= 2.5V+5%
5	Current dissipation per LVEPCL output	I <sub>DD,LVPECL_3.3V</sub>		19.36	23.26	mA	VDDO= 3.3V+5%
		I <sub>DD,LVPECL_2.5V</sub>		19.38	22.17	mA	VDDO= 2.5V+5%
6	Current dissipation per LVDS output	I <sub>DD,LVDSL_3.3V</sub>		6.73	8.00	mA	VDDO= 3.3V+5%
		I <sub>DD,LVDS_2.5V</sub>		6.87	7.83	mA	VDDO= 2.5V+5%
7	Current dissipation per HCSL output	I <sub>DD,HCSL_3.3V</sub>		16.43	19.87	mA	VDDO= 3.3V+5%
		I <sub>DD,HCSL_2.5V</sub>		17.14	19.18	mA	VDDO= 2.5V+5%

**Table 7 Input Characteristics\***

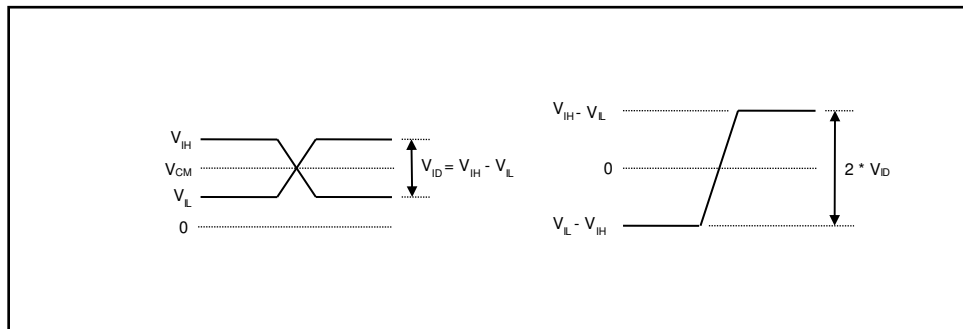
	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage for control inputs	$V_{CIH}$	1.05			V	
2	CMOS low-level input voltage for control inputs	$V_{CIL}$			0.45	V	
3	CMOS input leakage current for control inputs (includes current due to pull down resistors)	$I_L$	-25		50	$\mu A$	$V_i = V_{DD}$ or 0 V
4	Differential input common mode voltage for IN0_p/n and IN1_p/n	$V_{CM}$	1		2	V	
5	Differential input voltage difference for IN0_p/n and IN1_p/n $f \leq 1GHz$ **	$V_{ID}$	0.15		1.3	V	
6	Differential input voltage difference for IN0_p/n and IN1_p/n for $1GHz < f \leq 1.6GHz$ **	$V_{ID}$	0.35		1.3	V	
7	Differential input leakage current for IN0_p/n and IN1_p/n (includes current due to pull-up and pull-down resistors)	$I_L$	-150		150	$\mu A$	$V_i = 2V$ or 0V
8	Single ended input voltage for IN0_p and IN1_p	$V_{SI}$	-0.3		2.7	V	$V_{DD} = 3.3V$ or $2.5V$
9	Single ended input common mode voltage (IN0_p/n and IN1_p/n)	$V_{SIC}$	1		2	V	$V_{DD} = 3.3V$ or $2.5V$
10	Single ended input voltage swing for IN0_p and IN1_p	$V_{SID}$	0.3		1.3	V	$V_{DD} = 3.3V$ or $2.5V$
11	Input frequency (differential)	$f_{IN}$	0		1600	MHz	
12	Input frequency (LVCMOS)	$f_{IN\_CMOS}$	0		250	MHz	
13	Input duty cycle	dc	35%		65%		
14	Input slew rate	slew		2		V/ns	
15	Input pull-up/ pull-down resistance	$R_{PU}/R_{PD}$		60k $\Omega$			
16	Input pull-down resistance for INx_p	$R_{PD}$		30k $\Omega$			
17	Input multiplexer isolation IN0_p/n to IN1_p/n and vice versa Power on both inputs 0dBm, $f_{OFFSET} > 50kHz$	Iso		-84		dBc	$f_{IN} = 100$ MHz
				-82			$f_{IN} = 200$ MHz
				-71			$f_{IN} = 400$ MHz
				-67			$f_{IN} = 800$ MHz

\* Values are over Recommended Operating Conditions

\* Values are over all two power supply modes ( $V_{DD} = 3.3V$  and  $V_{DD} = 2.5V$ )

\* Input mux isolation is measured as amplitude of  $f_{OFFSET}$  spur in dBc on the output clock phase noise plot

\*\*Input differential voltage is calculated as  $V_{ID} = V_{IH} - V_{IL}$  where  $V_{IH}$  and  $V_{IL}$  are input voltage high and low respectively. It should not be confused with  $V_{ID} = 2 * (V_{IH} - V_{IL})$  used in some datasheets. Please refer to Figure 39.



**Figure 39. Differential Input Voltage Levels**

**Table 8 Crystal Oscillator Characteristics\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Mode of oscillation	mode	Fundamental				
2	Frequency	f	8		60	MHz	
3	On chip load capacitance			1		pF	
4	On chip series resistor			0		$\Omega$	
5	On chip shunt resistor	R		500		k $\Omega$	
6	Frequency in overdrive mode <sup>(1)</sup>	f <sub>ov</sub>	0.1		250	MHz	Functional but may not meet AC parameters Minimum depends on AC coupling Capacitor (0.1 $\mu$ F assumed)
7	Frequency in bypass mode <sup>(2)</sup>	f <sub>BP</sub>	0		250	MHz	Functional but may not meet AC parameters

\* Values are over Recommended Operating Conditions

\* Values are over all two power supply modes ( $V_{DD} = 3.3V$  and  $V_{DD} = 2.5V$ )

(1) Maximum input level is 2V

(2) Maximum output level is VDD

**Table 9 Power Supply Rejection Ratio for  $V_{DD} = V_{DDO} = 3.3V^*$**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	PSRR for LVPECL output	PSRR <sub>LVPECL</sub>		-71.75		dBc	f <sub>IN</sub> = 156.25 MHz
				-84.45			f <sub>IN</sub> = 312.5 MHz
				-82.11			f <sub>IN</sub> = 625 MHz
2	PSRR for LVDS output	PSRR <sub>LVDS</sub>		-95.16		dBc	f <sub>IN</sub> = 156.25 MHz
				-97.77			f <sub>IN</sub> = 312.5 MHz
				-79.23			f <sub>IN</sub> = 625 MHz
3	PSRR for HCSSL output	PSRR <sub>HCSSL</sub>		-77.15		dBc	f <sub>IN</sub> = 100 MHz
				-76.75			f <sub>IN</sub> = 156.25 MHz
				-80.44			f <sub>IN</sub> = 312.5 MHz

\* Values are over Recommended Operating Conditions

\* Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp

\* PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot



**Table 10 Power Supply Rejection Ratio for VDD = VDDO = 2.5V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	PSRR for LVPECL output	PSRR <sub>LVPECL</sub>		-73.68		dBc	f <sub>IN</sub> = 156.25 MHz
				-78.88			f <sub>IN</sub> = 312.5 MHz
				-71.82			f <sub>IN</sub> = 625 MHz
2	PSRR for LVDS output	PSRR <sub>LVDS</sub>		-90.04		dBc	f <sub>IN</sub> = 156.25 MHz
				-79.99			f <sub>IN</sub> = 312.5 MHz
				-73.45			f <sub>IN</sub> = 625 MHz
3	PSRR for HCSSL output	PSRR <sub>HCSSL</sub>		-92.16		dBc	f <sub>IN</sub> = 100 MHz
				-74.08			f <sub>IN</sub> = 156.25 MHz
				-91.88			f <sub>IN</sub> = 312.5 MHz

\* Values are over Recommended Operating Conditions

\* Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp

\* PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot

**Table 11 LVCMOS Output Characteristics for VDDO = 3.3V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage (1 mA load)	V <sub>OH</sub>	VDDO-0.1			V	DC Measurement
2	Output low voltage (1 mA load)	V <sub>OL</sub>			0.1	V	DC Measurement
3	Output High Current (Load adjusted to V <sub>out</sub> = VDDO/2)	I <sub>OH</sub>		30		mA	DC Measurement
4	Output Low Current (Load adjusted to V <sub>out</sub> = VDDO/2)	I <sub>OL</sub>		34		mA	DC Measurement
5	Output impedance	R <sub>O</sub>		15		Ω	DC Measurement
6	Rise time (20% to 80%)	t <sub>r</sub>		220	310	ps	
7	Fall time (20% to 80%)	t <sub>f</sub>		320	365	ps	
8	Output frequency	F <sub>O</sub>	0		250	MHz	
9	Input to output delay	t <sub>iOD</sub>	1.07	1.28	2.07	ns	
10	Output enable time	t <sub>EN</sub>			3	cycles	
11	Output disable time	T <sub>DIS</sub>			3	cycles	
12	Additive RMS jitter in 1MHz to 5MHz band	T <sub>L1M,5M</sub>		46	80	fs	Input Clock 25MHz
13	Additive RMS jitter in 12kHz to 5MHz band	T <sub>L12K,5M</sub>		56	90	fs	Input Clock 25MHz
14	Additive RMS jitter in 1MHz to 20MHz band	T <sub>L1M,20M</sub>		60	79	fs	Input Clock 125MHz
15	Additive RMS jitter in 12kHz to 20MHz band	T <sub>L12K,20M</sub>		65	86	fs	Input Clock 125MHz
16	Additive RMS jitter in 1MHz to 20MHz band	T <sub>L1M,20M</sub>		61	94	fs	Input Clock 156.25MHz
17	Additive RMS jitter in 12kHz to 20MHz band	T <sub>L12K,20M</sub>		66	100	fs	Input Clock 156.25MHz
18	Noise floor	N <sub>F</sub>		-165	-162	dBc/Hz	Input clock: 25 MHz
19				-160	-156	dBc/Hz	Input clock: 125 MHz
20				-158	-153	dBc/Hz	Input clock: 156.25 MHz

\* Values are over Recommended Operating Conditions

**Table 12 LVCMOS Output Characteristics for VDDO = 2.5V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage (1 mA load)	$V_{OH}$	VDDO-0.1			V	DC Measurement
2	Output low voltage (1 mA load)	$V_{OL}$			0.1	V	DC Measurement
3	Output High Current (Load adjusted to $V_{out} = VDDO/2$ )	$I_{OH}$		21		mA	DC Measurement
4	Output Low Current (Load adjusted to $V_{out} = VDDO/2$ )	$I_{OL}$		25		mA	DC Measurement
5	Output impedance	$R_o$		15		$\Omega$	DC Measurement
6	Rise time (20% to 80%)	$t_r$		225	310	ps	
7	Fall time (20% to 80%)	$t_f$		320	365	ps	
8	Output frequency	$F_o$	0		250	MHz	
9	Input to output delay	$t_{IOD}$	1.10	1.41	2.30	ns	
10	Output enable time	$t_{EN}$			3	cycles	
11	Output disable time	$T_{DIS}$			3	cycles	
12	Additive RMS jitter in 1MHz to 5MHz band	$T_{L1M,5M}$		51	104	fs	Input Clock 25MHz
13	Additive RMS jitter in 12kHz to 5MHz band	$T_{L12k,5M}$		62	111	fs	Input Clock 25MHz
14	Additive RMS jitter in 1MHz to 20MHz band	$T_{L1M,20M}$		64	81	fs	Input Clock 125MHz
15	Additive RMS jitter in 12kHz to 20MHz band	$T_{L12k,20M}$		70	88	fs	Input Clock 125MHz
16	Additive RMS jitter in 1MHz to 20MHz band	$T_{L1M,20M}$		62	94	fs	Input Clock 156.25MHz
17	Additive RMS jitter in 12kHz to 20MHz band	$T_{L12k,20M}$		68	100	fs	Input Clock 156.25MHz
18	Noise floor	$N_F$		-164	-161	dBc/Hz	Input clock: 25 MHz
19				-159	-155	dBc/Hz	Input clock: 125 MHz
20				-158	-153	dBc/Hz	Input clock: 156.25 MHz

\* Values are over Recommended Operating Conditions