



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# Low Skew, Low Additive Jitter 3 x 5 LVPECL/LVDS/HCSL Fanout Buffer with one LVCMOS output

## Features

- 3 to 1 input Multiplexer: Two inputs accept any differential (LVPECL, HCSL, LVDS, SSTL, CML, LVCMOS) or a single ended signal and the third input accepts a crystal or a single ended signal
- Five differential LVPECL/LVDS/HCSL outputs
- One LVCMOS output
- Ultra-low additive jitter: 24fs (integration band 12kHz to 20MHz at 625MHz clock frequency)
- Supports clock frequencies from 0 to 1.6GHz
- Supports 2.5V or 3.3V power supplies for LVPECL, LVDS or HCSL outputs
- Supports 1.5V, 1.8V, 2.5V or 3.3V power supplies for LVCMOS output
- Embedded Low Drop Out (LDO) Voltage regulator provides superior Power Supply Noise Rejection
- Maximum output to output skew of 40ps
- Device controlled via SPI

## Ordering Information

ZL40235LDG1	40 pin QFN	Trays
ZL40235LDF1	40 pin QFN	Tape and Reel
Package size: 6 x 6 mm		
<b>-40°C to +85°C</b>		

## Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3/4 clock distribution
- Wireless communications
- High performance microprocessor clock distribution
- Test Equipment

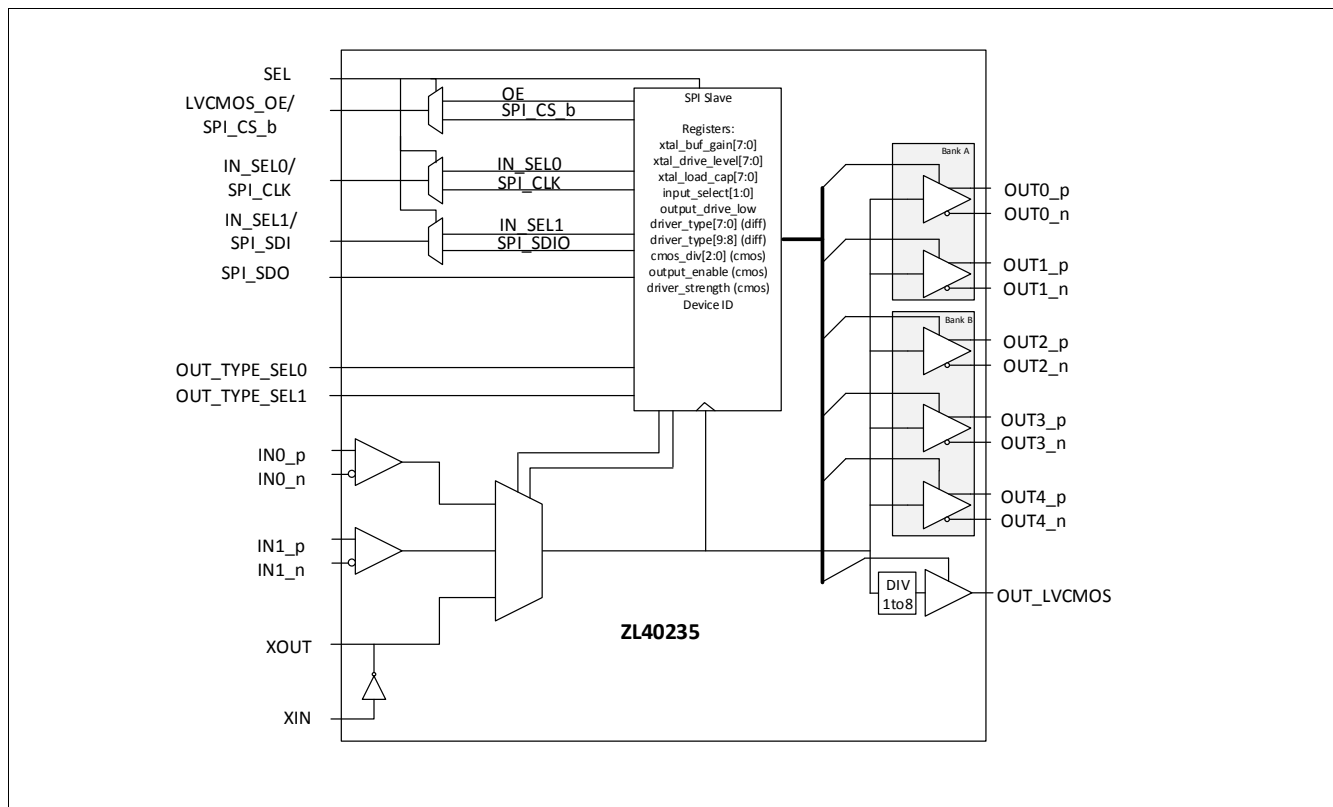


Figure 1. Functional Block Diagram

---

# Table of Contents

Features .....	1
Applications .....	1
Table of Contents.....	2
Pin Diagram.....	5
Pin Descriptions.....	6
Functional Description.....	9
Clock Inputs.....	9
Clock Outputs .....	12
Crystal Oscillator Input .....	13
Termination of unused inputs and outputs .....	13
Power Consumption.....	14
Power Supply Filtering .....	14
Power Supplies and Power-up Sequence.....	15
Host Interface .....	15
Typical device performance .....	20
Register Map .....	24
AC and DC Electrical Characteristics .....	30
Absolute Maximum Ratings.....	30
Recommended Operating Conditions.....	30
Change History .....	49
Package Outline .....	50

## List of Figures

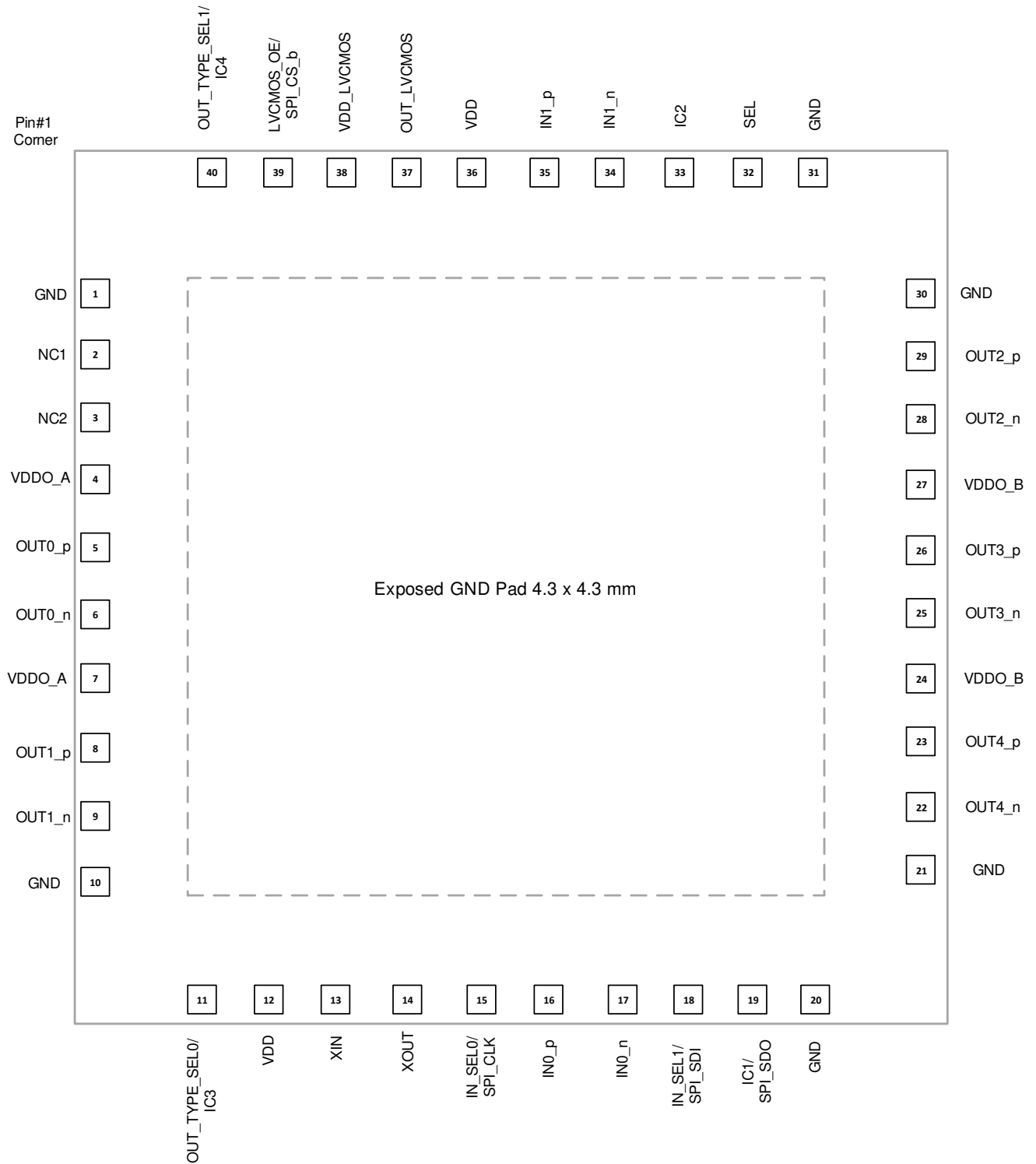
Figure 1.	Functional Block Diagram .....	1
Figure 2.	Pin Diagram .....	5
Figure 3.	Input driven by a single ended output .....	9
Figure 4.	Input driven by DC coupled LVPECL output.....	9
Figure 5.	Input driven by DC coupled LVPECL output (alternative termination).....	10
Figure 6.	Input driven by AC coupled LVPECL output.....	10
Figure 7.	Input driven by HCSL output .....	10
Figure 8.	Input driven by LVDS output .....	11
Figure 9.	Input driven by AC coupled LVDS .....	11
Figure 10.	Input driven by an SSTL output .....	11
Figure 11.	Termination for LVCMOS outputs .....	12
Figure 12.	Driving a load via transformer.....	12
Figure 13.	Crystal Oscillator Circuit.....	13
Figure 14.	Crystal Oscillator Circuit in Hardware Controlled Mode .....	13
Figure 15.	Power Supply Filtering .....	15
Figure 16.	Output Disable .....	16
Figure 17.	Output Enable.....	16
Figure 18.	SPI slave interface.....	17
Figure 19.	Serial Peripheral Interface Functional Waveform – LSB First Mode .....	18
Figure 20.	Serial Peripheral Interface Functional Waveform – MSB First Mode.....	18
Figure 21.	Example of the Burst Mode Operation .....	19
Figure 22.	156.25MHz LVPECL.....	20
Figure 23.	1.5GHz LVPECL.....	20
Figure 24.	156.25MHz LVDS .....	20
Figure 25.	1.5GHz LVDS .....	20
Figure 26.	100MHz HCSL.....	20
Figure 27.	250MHz HCSL.....	20
Figure 28.	I/O delay vs temperature .....	21
Figure 29.	PSNR vs noise frequency .....	21
Figure 30.	100MHz LVPECL Phase Noise .....	21
Figure 31.	100MHz LVDS Phase Noise .....	21
Figure 32.	156.25MHz LVDS Phase Noise in Xtal mode .....	21
Figure 33.	100MHz HCSL Phase Noise .....	21
Figure 34.	156.25MHz LVPECL Phase Noise.....	22
Figure 35.	625MHz LVPECL Phase Noise.....	22
Figure 36.	156.25MHz LVDS Phase Noise .....	22
Figure 37.	625MHz LVDS Phase Noise .....	22
Figure 38.	Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate.....	23
Figure 39.	Output clock noise floor vs input clock slew-rate.....	23
Figure 40.	Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate.....	23
Figure 41.	Output clock noise floor vs input clock slew-rate.....	23
Figure 42.	Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate.....	23
Figure 43.	Output clock noise floor vs input clock slew-rate .....	23
Figure 44.	Differential Input Voltage Levels.....	31
Figure 45.	Differential Output Voltage Levels.....	35
Figure 46.	SPI (Serial Peripheral Interface) Timing - LSB First Mode.....	47
Figure 47.	SPI (Serial Peripheral Interface) Timing - MSB First Mode.....	47

**List of Tables**

Table 1 Pin Description.....	6
Table 2 Input clock selection.....	15
Table 3 Output Type Selection.....	15
Table 4 Register Map.....	24
Table 5 Absolute Maximum Ratings*.....	30
Table 6 Recommended Operating Conditions*.....	30
Table 7 Current consumption.....	30
Table 8 Input Characteristics*.....	31
Table 9 Crystal Oscillator Characteristics*.....	32
Table 10 Power Supply Rejection Ratio for $VDD = VDDO = 3.3V^*$ .....	32
Table 11 Power Supply Rejection Ratio for $VDD = VDDO = 2.5V^*$ .....	33
Table 12 LVCMOS Output Characteristics for $VDDO = 3.3V^*$ .....	33
Table 13 LVCMOS Output Characteristics for $VDDO = 2.5V^*$ .....	34
Table 14 LVPECL Output Characteristics for $VDDO = 3.3V^*$ .....	35
Table 15 LVPECL Output Characteristics for $VDDO = 2.5V^*$ .....	36
Table 16 LVDS Outputs for $VDDO = 3.3V^*$ .....	37
Table 17 LVDS Outputs for $VDDO = 2.5V^*$ .....	38
Table 18 HCSL Outputs for $VDDO = 3.3V^*$ .....	39
Table 19 HCSL Outputs for $VDDO = 2.5V^*$ .....	40
Table 20 LVCMOS Output Phase Noise with 25 MHz XTAL*.....	41
Table 21 LVPECL Output Phase Noise with 25 MHz XTAL*.....	41
Table 22 LVDS Output Phase Noise with 25 MHz XTAL.....	42
Table 23 HCSL Output Phase Noise with 25 MHz XTAL.....	42
Table 24 LVCMOS Output Phase Noise with 125 MHz XTAL*.....	43
Table 32 AC Electrical Characteristics* - SPI (Serial Peripheral Interface) Timing.....	47
Table 33 6x6mm QFN Package Thermal Properties.....	48

## Pin Diagram

The device is packaged in a 6 x 6 mm 40-pin QFN.



**Figure 2. Pin Diagram**

## Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I<sub>PU</sub> – input with 300kΩ internal pull-up resistor, I<sub>PD</sub> – input with 300kΩ internal pull-down resistor, I<sub>APU</sub> – input with 31kΩ internal pull-up resistor, I<sub>APD</sub> – input with 30kΩ internal pull-down resistor, I<sub>APU/APD</sub> – input with 60kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/O – Input/Output pin, NC – No connect, P – power supply pin.

**Table 1 Pin Description**

#	Name	I/O	Description
<b>Input Reference</b>			
16 17 35 34	IN0_p IN0_n IN1_p IN1_n	I <sub>APD</sub> I <sub>APU/APD</sub> I <sub>APD</sub> I <sub>APU/APD</sub>	<p><b>Input Differential or Single Ended References 0 and 1</b></p> <p>Input frequency range 0Hz to 1.6GHz.</p> <p>Non inverting inputs (_p) are pulled down with internal 30kΩ pull-down resistors. Inverting inputs (_n) are biased at VDD/2 with 60kΩ pull-up and pull-down resistors to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).</p>
<b>Output Clocks</b>			
5 6 8 9 29 28 26 25 23 22	OUT0_p OUT0_n OUT1_p OUT1_n OUT2_p OUT2_n OUT3_p OUT3_n OUT4_p OUT4_n	O	<p><b>Ultra Low Additive Jitter Differential LVPECL/HCSL/LVDS Outputs 0 to 4</b></p> <p>Output frequency range 0 to 1.6GHz</p> <p>In SPI bus controlled mode (SEL pin pulled high on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output is programmable via SPI bus</p> <p>In Hardware control mode (SEL pin pulled low on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output bank is controlled via OUTA/B_TYPE_SEL0/1 pins</p>
37	OUT_LVCMOS	O	<p><b>Ultra Low Additive Jitter LVCMOS Output</b></p> <p>Output frequency range 0 to 250MHz</p>
<b>Control</b>			
32	SEL	I <sub>PD</sub>	<p><b>Select control.</b></p> <p>When this pin is low, the device is controlled via hardware pins, IN_SEL0/1 and OE. When this pin is high, the device is controlled via SPI port.</p> <p>Any change of SEL pin value requires power cycle. Hence, SEL pin cannot be changed on the fly.</p>

15	IN_SEL0/SPI_CLK	$I_{PD}$ or $I_{PU}$	<p><b>Input Select 0 or Clock for Serial Interface.</b> When SEL pin is low this pin is Input Select 0 hardware control input pin and it is pulled-down with 300 k<math>\Omega</math> resistor. When SEL pin is high this pin provides clock for serial micro-port interface and it is pulled-up with 300 k<math>\Omega</math> resistor.</p> <table border="1" data-bbox="621 331 1508 562"> <thead> <tr> <th>IN_SEL1</th> <th>IN_SEL0</th> <th>OUTN</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Input 0 (IN0)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Input 1 (IN1)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Crystal Oscillator or overdrive</td> </tr> <tr> <td>1</td> <td>1</td> <td>Crystal Bypass</td> </tr> </tbody> </table>	IN_SEL1	IN_SEL0	OUTN	0	0	Input 0 (IN0)	0	1	Input 1 (IN1)	1	0	Crystal Oscillator or overdrive	1	1	Crystal Bypass
IN_SEL1	IN_SEL0	OUTN																
0	0	Input 0 (IN0)																
0	1	Input 1 (IN1)																
1	0	Crystal Oscillator or overdrive																
1	1	Crystal Bypass																
18	IN_SEL1/SPI_SDI	$I_{PD}$ or $I_{PU}$	<p><b>Input Select 1 or Serial Interface Input.</b> When SEL pin is low this pin is Input Select 1 hardware control pin and it is pulled-down with 300 k<math>\Omega</math> resistor. When SEL pin is high this pin is serial interface input stream and it is pulled-up with 300 k<math>\Omega</math> resistor. The serial data stream holds the access command, the address and the write data bits.</p>															
19	IC1/SPI_SDO	I/O	<p><b>Internal Connection 1 or Serial Interface Output.</b></p> <p>When SEL pin is low this pin in an internal connection. Leave open.</p> <p>When SEL pin is high this pin is Serial interface output stream. As an output the serial stream holds the read data bits.</p>															
33	IC2	$I_{PD}$	<p><b>Internal Connection 2.</b> This pin should be left open.</p>															
39	LVCMOS_OE/ SPI_CS_b	$I_{PD}$ or $I_{PU}$	<p><b>LVCMOS Output Enable or Chip Select for Serial Interface.</b></p> <p>When SEL pin is low this pin is LVCMOS Output Enable hardware control input and it is pulled-down with 300 k<math>\Omega</math> resistor.</p> <p>When SEL pin is high this pin is serial interface chip select and it is pulled-up with 300 k<math>\Omega</math> resistor--this is an active low signal.</p>															
11 40	OUT_TYPE_SEL0/ IC3 OUT_TYPE_SEL1/ IC4	$I_{PD}$	<p><b>Output Signal Type:</b></p> <p>When SEL pin is low these two pins Selects Type for all outputs</p> <table border="1" data-bbox="621 1593 1508 1824"> <thead> <tr> <th>OUT_TYPE_SEL1</th> <th>OUT_TYPE_SEL0</th> <th>Output 0 to 4</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>LVPECL</td> </tr> <tr> <td>0</td> <td>1</td> <td>LVDS</td> </tr> <tr> <td>1</td> <td>0</td> <td>HCSL</td> </tr> <tr> <td>1</td> <td>1</td> <td>High-Z (Disabled)</td> </tr> </tbody> </table> <p>When SEL pin is high these two pins are unused and should be left unconnected.</p>	OUT_TYPE_SEL1	OUT_TYPE_SEL0	Output 0 to 4	0	0	LVPECL	0	1	LVDS	1	0	HCSL	1	1	High-Z (Disabled)
OUT_TYPE_SEL1	OUT_TYPE_SEL0	Output 0 to 4																
0	0	LVPECL																
0	1	LVDS																
1	0	HCSL																
1	1	High-Z (Disabled)																



<b>Crystal Oscillator</b>			
13	XIN	I	<b>Crystal Oscillator Input or crystal bypass mode or crystal overdrive mode</b>
14	XOUT	O	<b>Crystal Oscillator Output</b>
<b>No Connect</b>			
2 3	NC1 NC2	NC	<b>No Connect (not connected to the die)</b> Leave unconnected or connect to GND for mechanical support
<b>Power and Ground</b>			
12 36	VDD	P	<b>Positive Supply Voltage.</b> Connect to 3.3V or 2.5V supply.
4 7	VDDO_A	P	<b>Positive Supply Voltage for Differential Outputs Bank A</b> Connect 3.3V or 2.5V power supply. VDDO_A does not have to be connected to the same voltage level as VDD or VDDO_B. These pins power up differential outputs OUT0_p/n and OUT1_p/n.
24 27	VDDO_B	P	<b>Positive Supply Voltage for Differential Outputs Bank B</b> Connect 3.3V or 2.5V power supply. VDDO_B does not have to be connected to the same voltage level as VDD or VDDO_A. These pins power up differential outputs OUT2_p/n, OUT3_p/n and OUT4_p/n.
38	VDD_LVCMOS	P	<b>Positive Supply Voltage for LVCMOS Output</b> Connect 3.3V, 2.5V, 1.8V or 1.5V power supply
1 10 20 21 30 31	GND	P	<b>Ground</b> Connect to the ground
E-Pad	GND	P	<b>Ground.</b> Connect to the ground

### Functional Description

The ZL40235 is a programmable or hardware pin controlled low additive jitter, low power 3 x 5 LVPECL/HCSL/LVDS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML ) or single ended (LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins. All the other components for building crystal oscillator are built in device such as load capacitance, series and shunt resistors.

The ZL40235 has five LVPECL/HCSL/LVDS outputs which can be powered from 3.3V or 2.5V supply. Each output can be independently enabled/disabled via SPI bus. The type of each output driver can be programmed to be LVPECL, HCSL or LVDS. Hence, the device can be configured to support application where different signal formats are needed.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

### Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40235 inputs.

Figure 3 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each and  $R_o + R_s$  should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor  $R_s$  should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 8). The source resistors of  $R_s = 270\Omega$  could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of  $(3.3V/2) * (1/(270\Omega + 50\Omega)) = 5.16mA$ .

For optimum performance both differential input pins ( $\_p$  and  $\_n$ ) need to be DC biased to the same voltage. Hence, the ratio  $R1/R2$  should be equal to the ratio  $R3/R4$ .

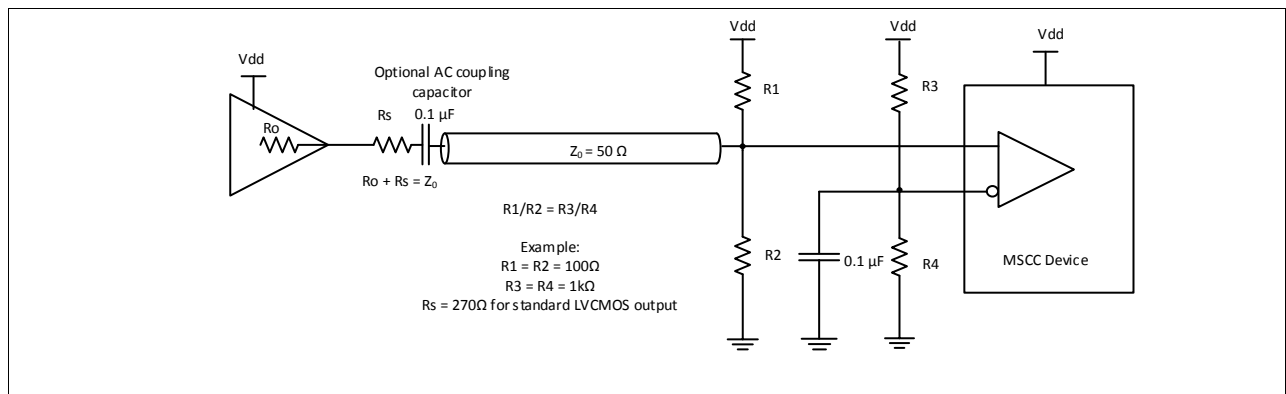


Figure 3. Input driven by a single ended output

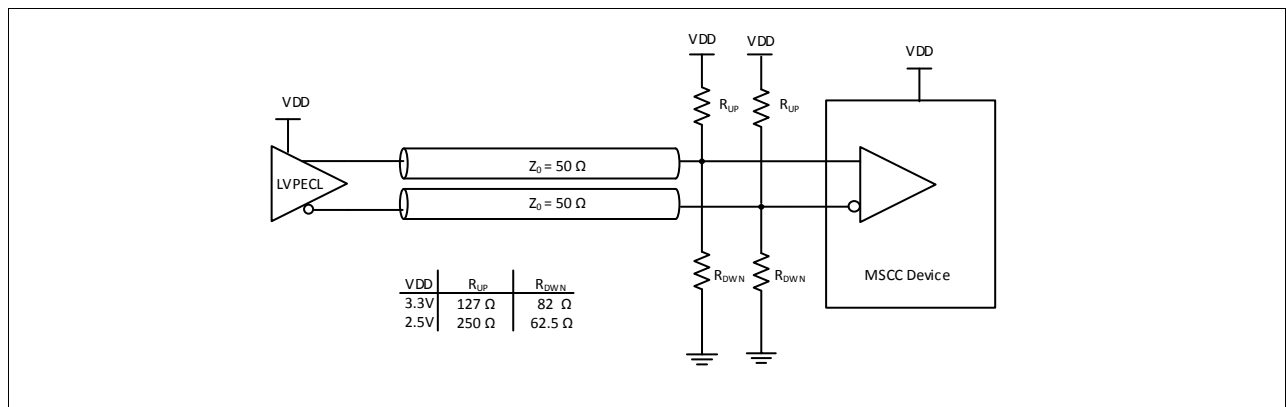


Figure 4. Input driven by DC coupled LVPECL output

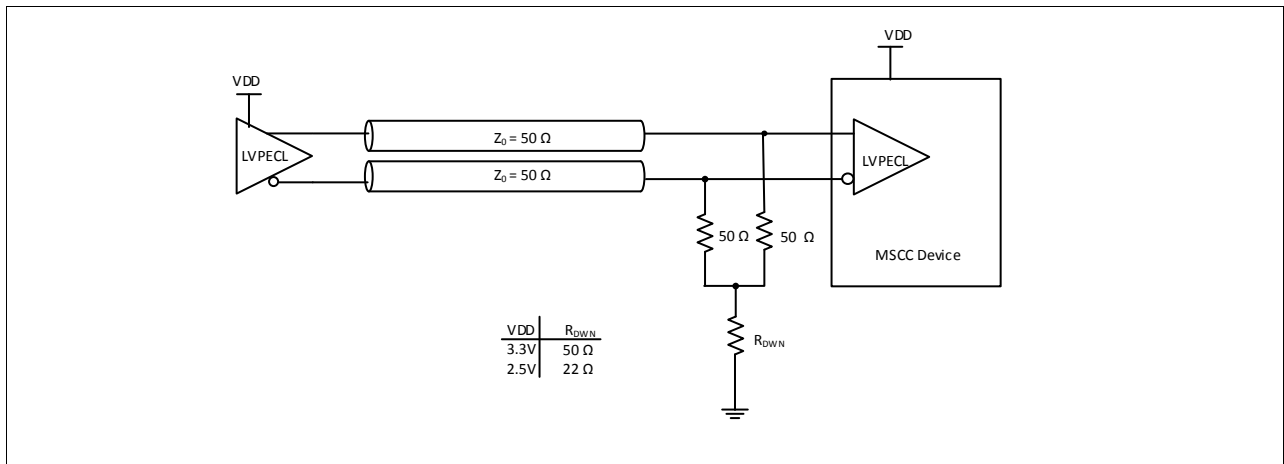


Figure 5. Input driven by DC coupled LVPECL output (alternative termination)

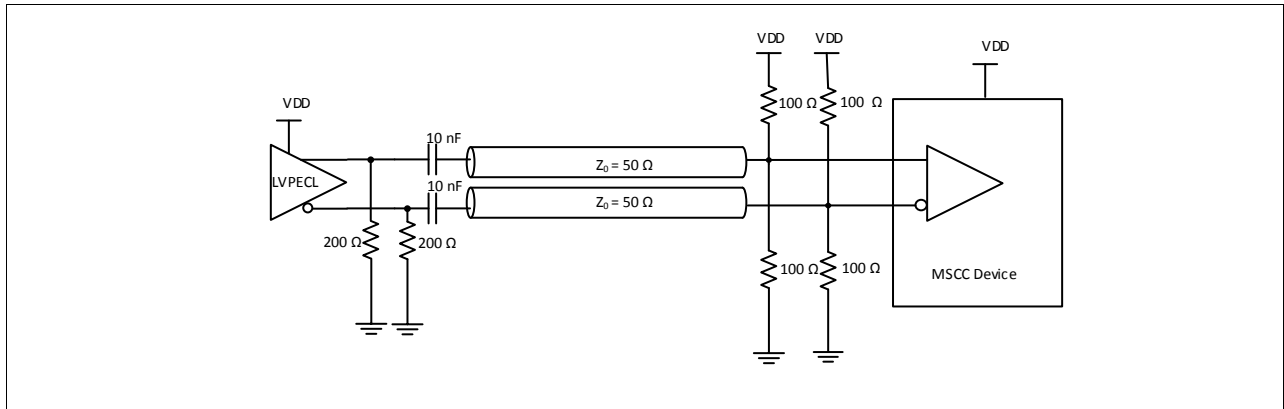


Figure 6. Input driven by AC coupled LVPECL output

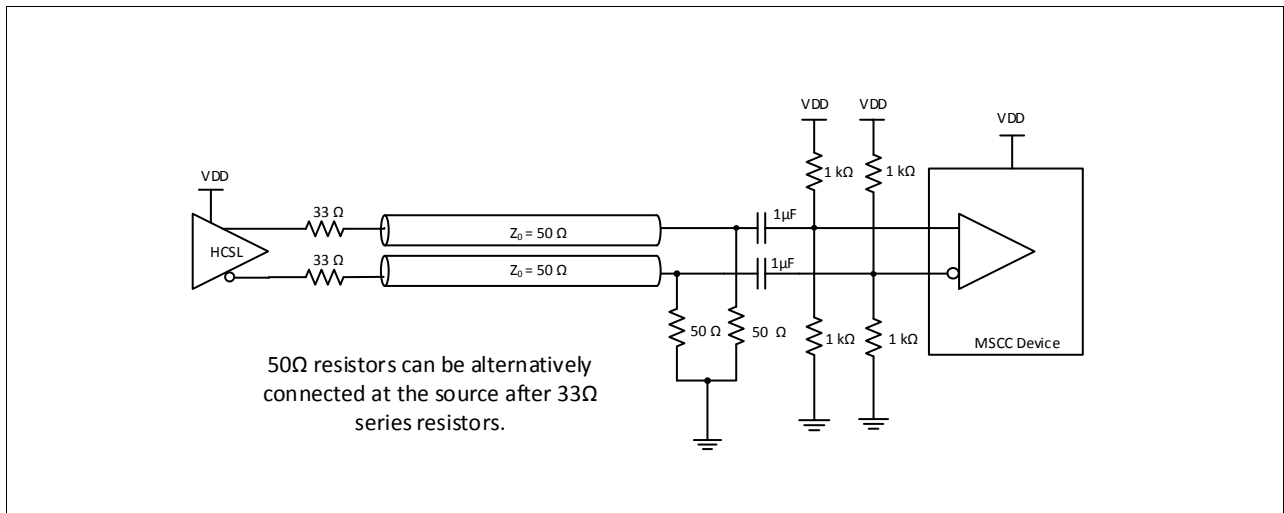


Figure 7. Input driven by HCSL output

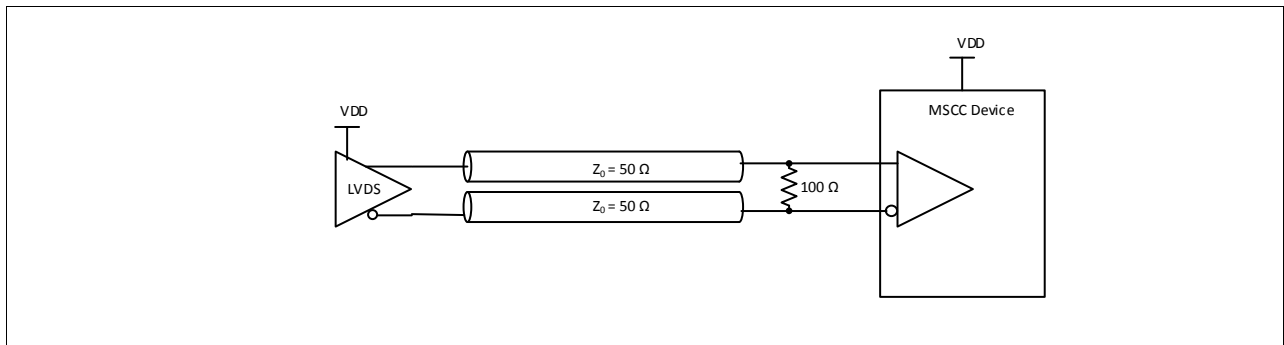


Figure 8. Input driven by LVDS output

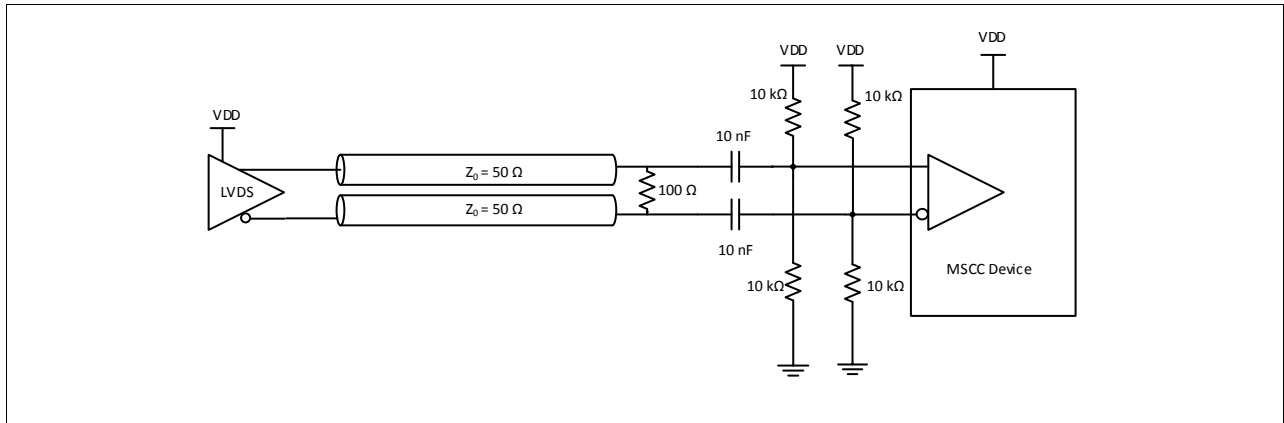


Figure 9. Input driven by AC coupled LVDS

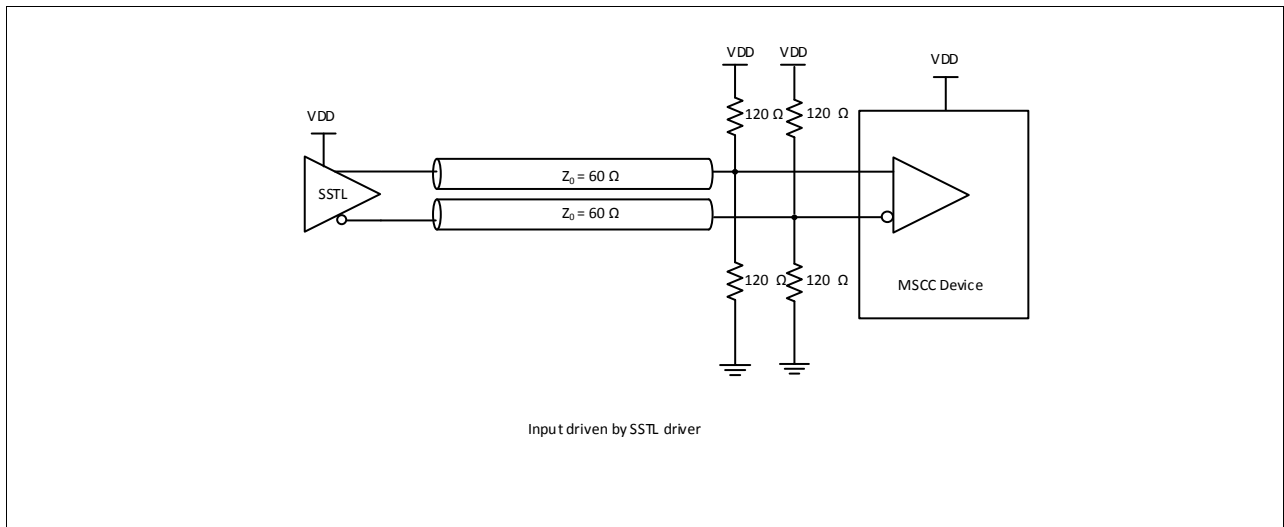
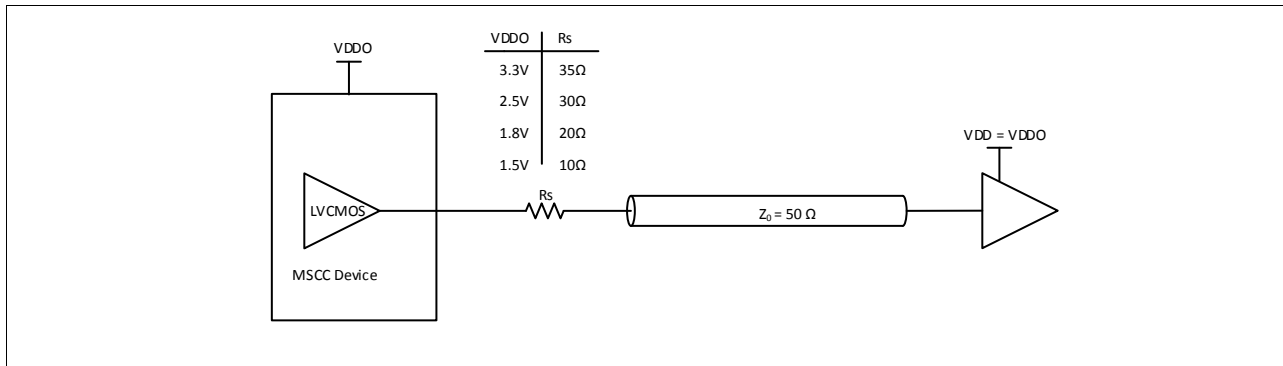


Figure 10. Input driven by an SSTL output

## Clock Outputs

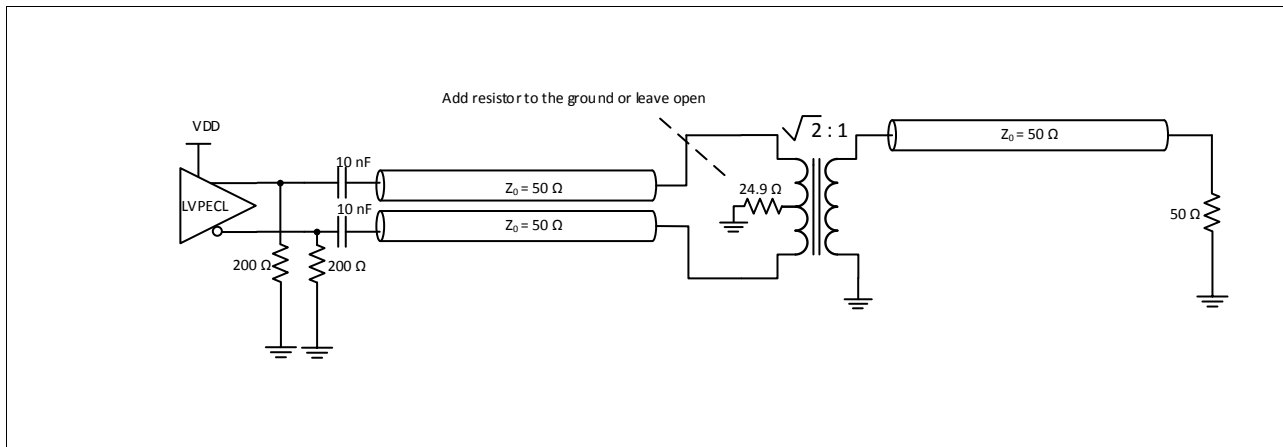
LVC MOS output OUT10 require only series termination resistor whose value is depending on LVC MOS output voltage as shown in Figure 11.



**Figure 11. Termination for LVC MOS outputs**

Differential outputs LVPECL and LVDS should have same termination as corresponding outputs described in previous section. HCSL outputs should be terminated with 33Ω series resistors at the source and 50Ω shunt resistors at the source or at the end on the transmission line. AC coupling and re-biasing is not required at the outputs when driving native HCSL receivers.

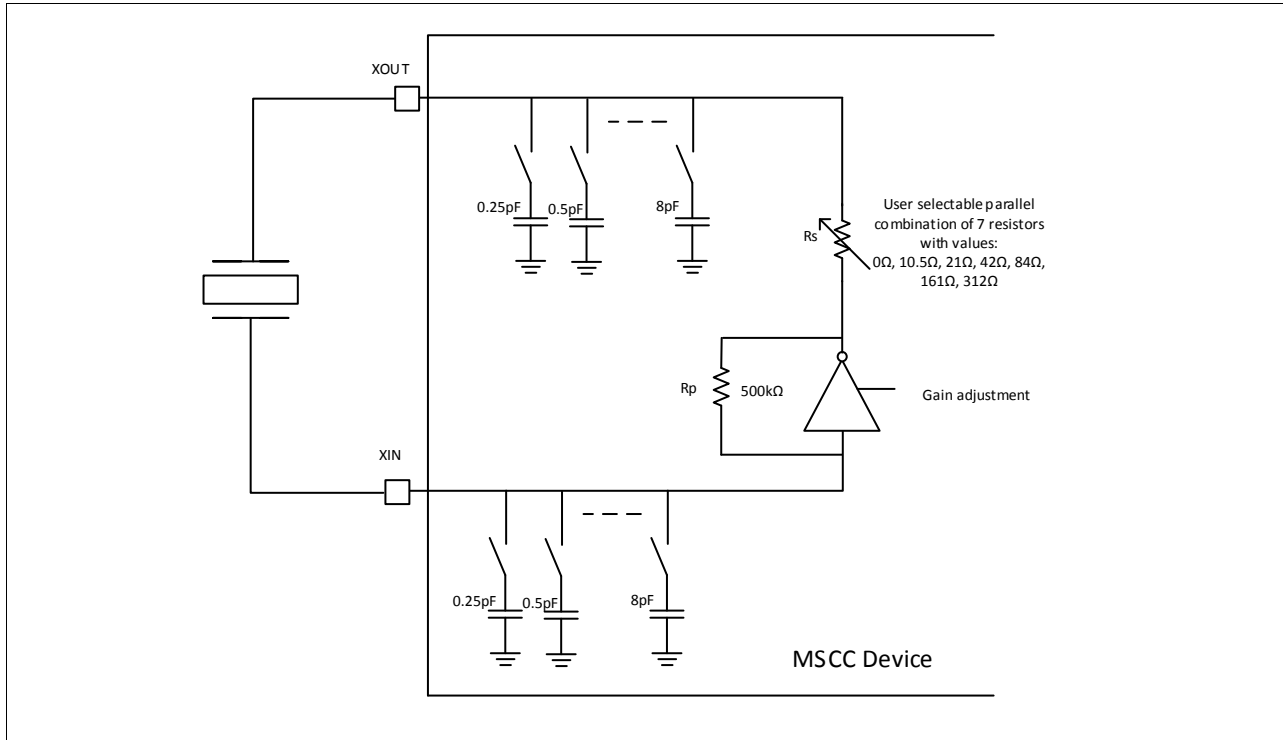
The device is designed to drive differential input of semiconductor devices. In applications that use a transformer to convert from the differential to the single ended output (for example driving an oscilloscope 50Ω input), a resistor larger than 10Ω should be added at the center tap of the primary winding to achieve optimum jitter performance as shown in Figure 12. This is to provide a nominal common mode impedance of 10Ω or higher which is typical for differential terminations.



**Figure 12. Driving a load via transformer**

### Crystal Oscillator Input

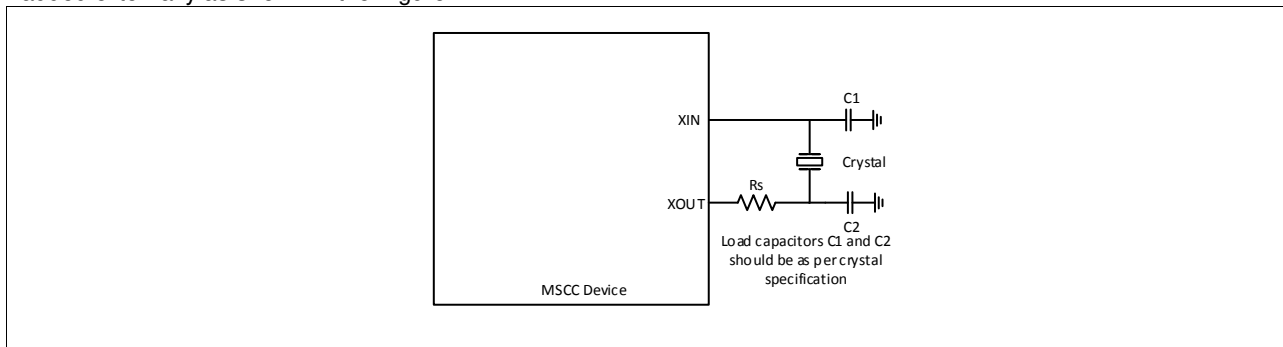
The crystal oscillator circuit can work with crystal resonators from 8MHz to 160MHz. As can be seen in the following figure only crystal resonator is required and all the other components are built-in the device. To be able support crystal resonators with different characteristics all internal components are programmable.



**Figure 13. Crystal Oscillator Circuit**

The load capacitors can be programmed from 0 to 21.75 pF (4pF default) with resolution of 0.25pF which not only meets load requirement for most crystal resonator but also allows for fine tuning of the crystal resonator frequency. The amplifier gain can be adjusted in five steps and series resistor can be adjusted as parallel combination of seven different resistors: 0Ω, 10.5Ω, 21Ω, 42Ω, 84Ω, 161Ω and 312Ω (84Ω default). Although the first resistor is 0Ω the series resistance  $R_s$  will be slightly higher than 0Ω due to parasitic resistance of the switch which connects resistor. Hence the minimum series resistance is achieved when all seven resistors are connected in parallel. The shunt resistor is fixed and its value is 500kΩ.

In Hardware Controlled mode the capacitive load is set at 4pF, internal series resistance to 84Ω and they cannot be changed. For Crystal requiring higher load or series resistance additional capacitance and/or series resistance can be added externally as shown in the Figure 14.



**Figure 14. Crystal Oscillator Circuit in Hardware Controlled Mode**

### Termination of unused inputs and outputs

Unused inputs can be left unconnected or alternatively IN\_0/1 can be pulled-down by 1kΩ resistor. Unused outputs should be left unconnected.

## Power Consumption

The device total power consumption can be calculated as:

$$P_T = P_S + P_{XTAL} + P_C + P_{O\_DIF} + P_{O\_LVCMOS}$$

Where:

$$P_S = V_{DD} \times I_S$$

The core power when XTAL is not used. The current is specified in Table 7. If XTAL is running this power should be set to zero.

$$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$$

The core power when XTAL is used. The current is provided in Table 7. If XTAL is not used this power should be set to zero.

$$P_C = V_{DDO} \times I_{DD\_CM}$$

Common output power shared among all ten outputs. The current  $I_{DD\_CM}$  is specified in Table 7.

$$P_{O\_DIF} = V_{DDO} \times (I_{DD\_LVDS} \times N_1 + I_{DD\_LVPECL} \times N_2 + I_{DD\_HCSL} \times N_3)$$

Output power where output currents are specified in Table 7.

$N_1$ ,  $N_2$  and  $N_3$  are number of enabled LVPECL, LVDS and HCSL outputs respectively and  $N_1+N_2+N_3$  is less or equal to 5.

$$P_{O\_LVCMOS} = V_{DD\_LVCMOS} \times (I_{DD} \times f / 100MHz + V_{DD\_LVCMOS} \times C_{LOAD} \times f)$$

Dynamic LVCMOS output power.  $I_{DD}$  is specified in Table 7. If LVCMOS output is disabled this term is equal to zero.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption.

$$P_D = P_T - N_1 \times P_{LVPECL} - N_2 \times P_{LVDS} - N_3 \times P_{HCSL}$$

Where  $N_1$ ,  $N_2$  and  $N_3$  are number of enabled LVPECL, LVDS and HCSL outputs respectively. Since there are five differential outputs  $N_1 + N_2 + N_3$  is less or equal to 5.

$$P_{LVPECL} = (V_{OH} - V_B)^2 / 50\Omega + (V_{OL} - V_B)^2 / 50\Omega + (V_{OH} - V_B) \times V_B / 50\Omega + (V_{OL} - V_B) \times V_B / 50\Omega$$

$V_{OH}$  and  $V_{OL}$  are the output high and low voltages respectively for LVPECL output

$V_B$  is LVPECL bias voltage equal to  $V_{DD} - 2V$

$$P_{LVDS} = V_{SW}^2 / 100\Omega$$

$V_{SW}$  is voltage swing of LVDS output.

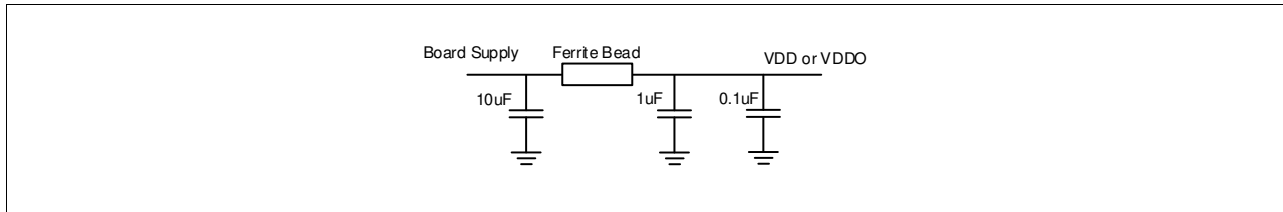
$$P_{HCSL} = (V_{SW} / 50\Omega)^2 \times (33\Omega + 50\Omega)$$

$V_{SW}$  is voltage swing of HCSL output.  $50\Omega$  is termination resistance and  $33\Omega$  is series resistance of the HCSL output.

## Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1 $\mu$ F capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce

the power noise from adjacent digital components on the board each power supply could be further insulated with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling for each power pin.



**Figure 15. Power Supply Filtering**

### Power Supplies and Power-up Sequence

The device has four different power supplies: VDD, VDDO\_A, VDDO\_B and VDD\_LVCMOS which are mutually independent. Voltages supported by each of these power supplies are specified in Table 1.

The device is not sensitive to the power-up sequence. For example commonly used sequence where higher voltage comes up before or at the same time as the lower voltages can be used (or any other sequence)

### Host Interface

ZL30235 can be controlled via hardware pins (SEL pin tied low) or via SPI port (SEL pin tied high). The mode shall be selected during power up and it cannot be changed on the fly.

### Hardware Control Mode

In this mode, ZL40235 is controlled via Input Select (IN\_SEL0/1) pins which select which one of three inputs is fed to the output and show in Table 2 and OUT\_TYPE\_SEL0/1 pins which select signal level (LVPECL, LVDS, HCSL or Hi-Z) as shown in Table 3.

All input control pins have low input threshold voltage so they can be driven from the device with low output voltage (FPGA/CPLD). Supported voltages are between 1.2V and VDD (2.5V or 3.3V).

**Table 2 Input clock selection**

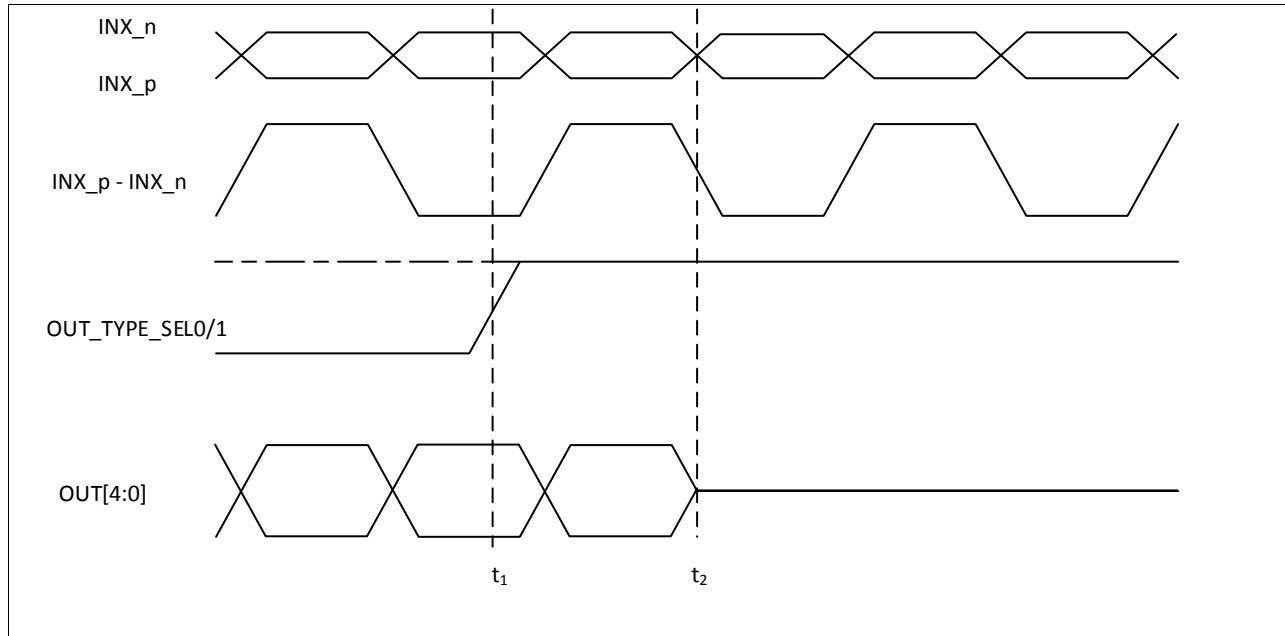
IN_SEL1	IN_SEL0	Selected Input
0	0	IN0_p, IN0_n
0	1	IN1_p, IN1_n
1	X	XIN

**Table 3 Output Type Selection**

OUT_TYPE_SEL1	OUT_TYPE_SEL0	Output
0	0	LVPECL
1	1	LVDS
1	0	HCSL
1	1	High-Z (Output Disabled)

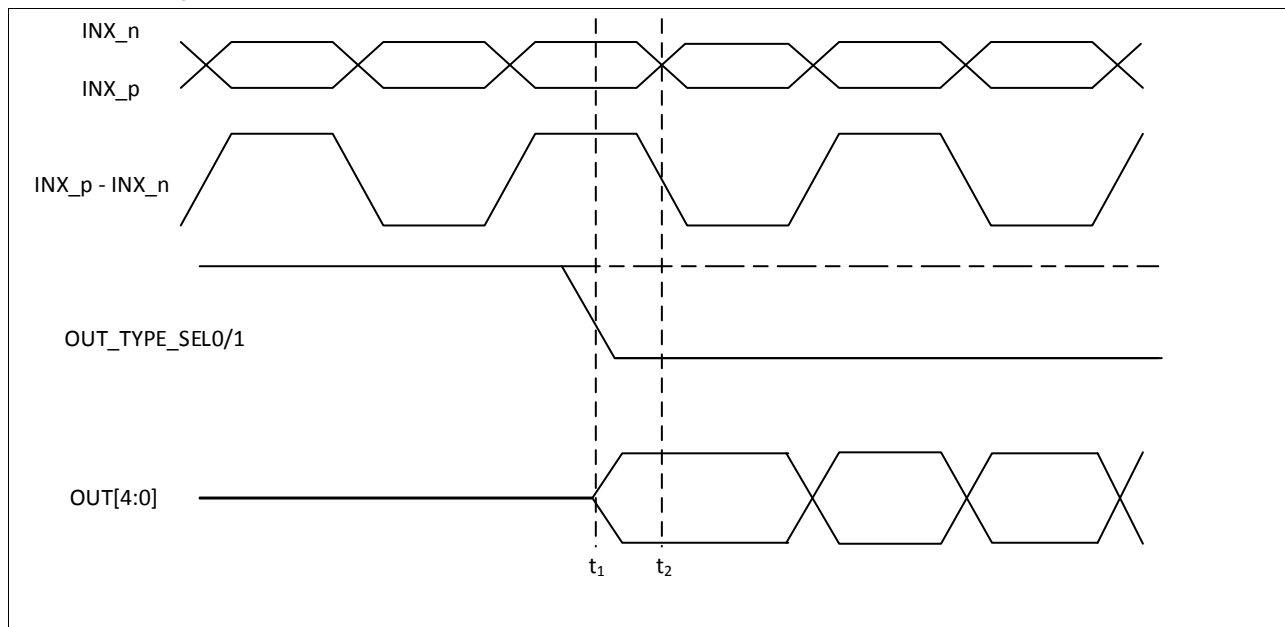


Output is disabled synchronously on the falling edge of the input ( $t_2$ ) as shown in Figure 16.



**Figure 16. Output Disable**

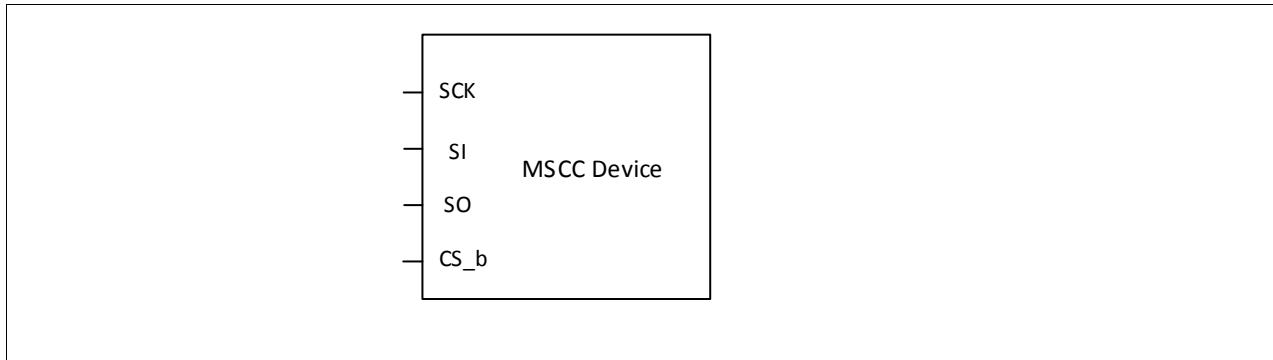
Outputs can be enabled by toggling one or both OUT\_TYPE\_SEL0/1 pins low depending on which type of interface needs to be enabled. As soon as one or both OUT\_TYPE\_SEL0/1 pins go low ( $t_1$ ) the outputs will go from high-Z to low ( $OUT_{X_p} = \text{low}$ ,  $OUT_{X_n} = \text{high}$ ) and will start to track the input after the first falling edge ( $t_2$ ) of the input signal as shown in Figure 17.



**Figure 17. Output Enable**

### SPI Control Mode

ZL40235 is controlled via four pin SPI slave interface as shown in the following figure.



**Figure 18. SPI slave interface**

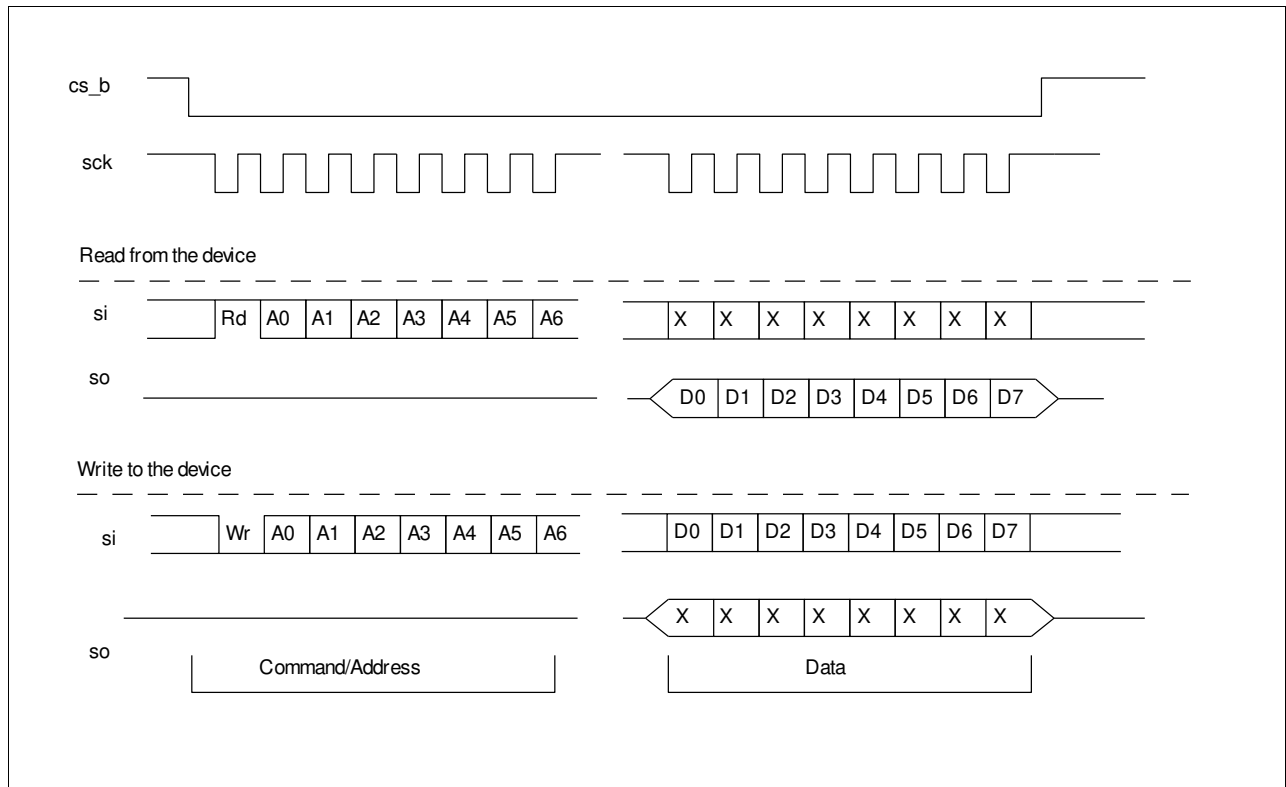
All SPI input pins have low threshold voltage so they can be driven from low output voltage SPI master device. Supported voltages are between 1.2V and VDD (2.5V or 3.3V). This allows device to be controlled from an FPGA with low voltage I/O supply.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **SO** pin must be ignored. Similarly, the input data on the **SI** pin is ignored by the device during a read cycle.

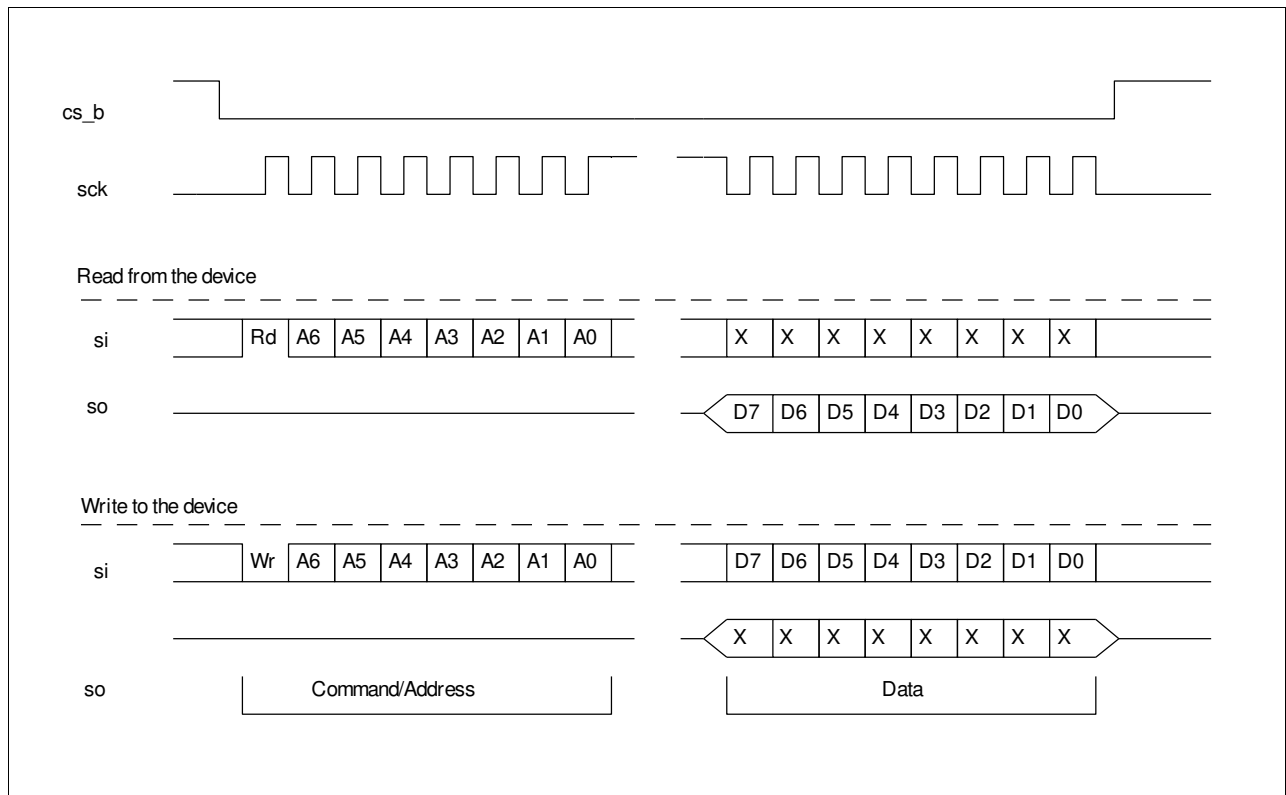
The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission or Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **SCK** pin when the **CS\_b** pin is active. If the **SCK** pin is low during **CS\_b** activation, then MSb first timing is selected. If the **SCK** pin is high during **CS\_b** activation, then LSb first timing is assumed.

The SPI port expects 1-bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **CS\_b** pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal **CS\_b** is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

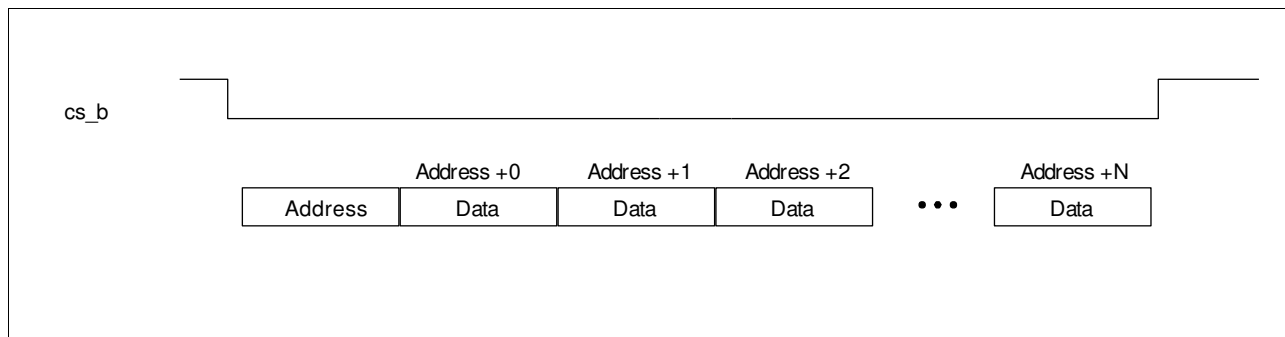
Functional waveforms for the LSb and MSb first mode, and burst mode are shown in Figure 19 and Figure 20 respectively. Figure 21 shows an example of burst mode operation which allows user to read or write consecutive location in the register map.



**Figure 19. Serial Peripheral Interface Functional Waveform – LSB First Mode**



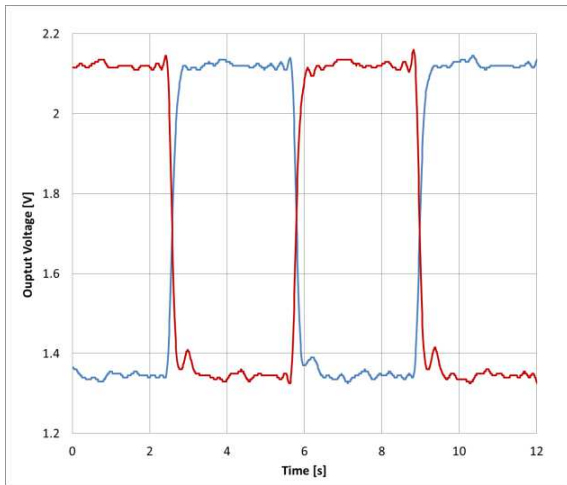
**Figure 20. Serial Peripheral Interface Functional Waveform – MSB First Mode**



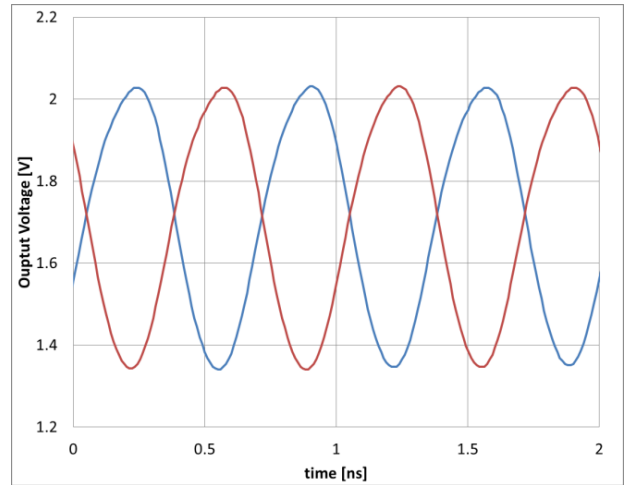
**Figure 21. Example of the Burst Mode Operation**

## Typical device performance

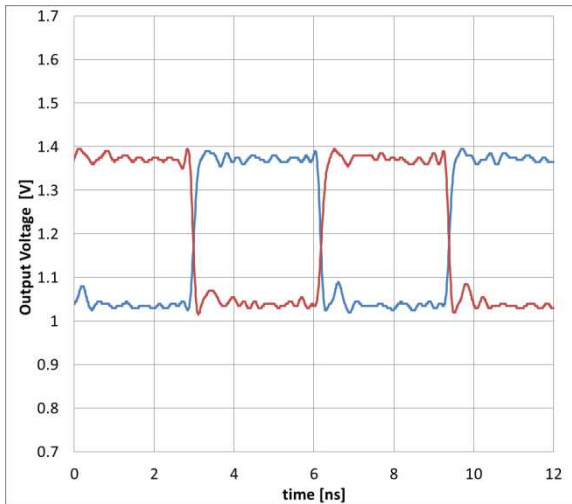
The following plots show typical device performances



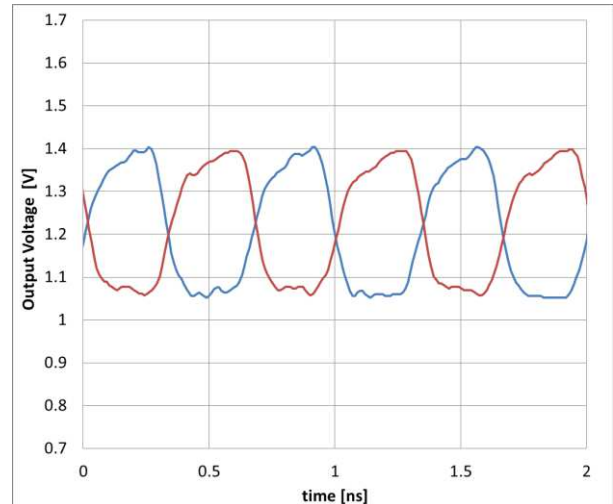
**Figure 22. 156.25MHz LVPECL**



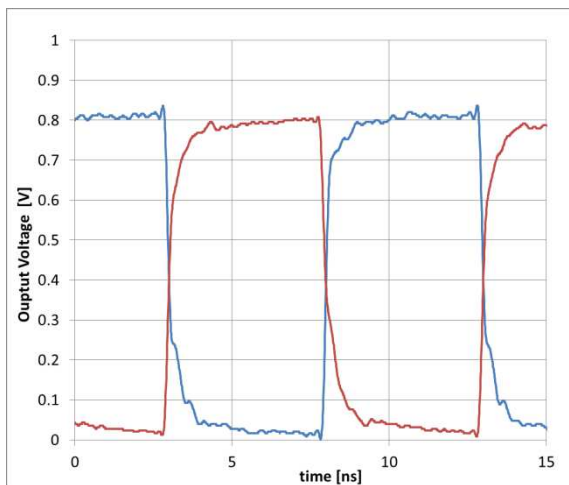
**Figure 23. 1.5GHz LVPECL**



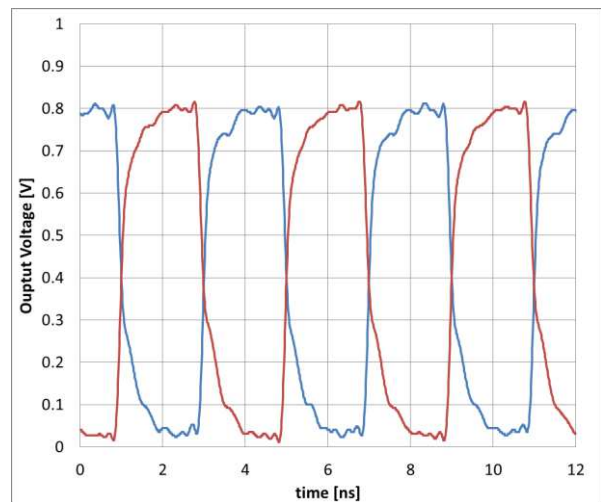
**Figure 24. 156.25MHz LVDS**



**Figure 25. 1.5GHz LVDS**



**Figure 26. 100MHz HCSSL**



**Figure 27. 250MHz HCSSL**

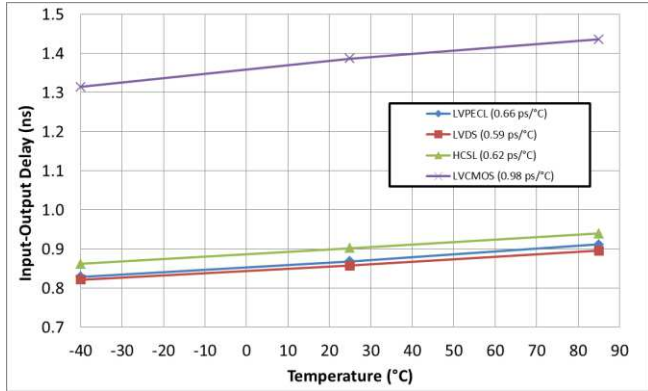


Figure 28. I/O delay vs temperature

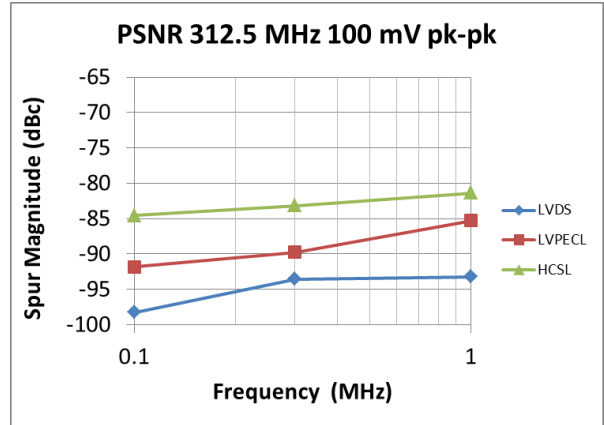


Figure 29. PSNR vs noise frequency

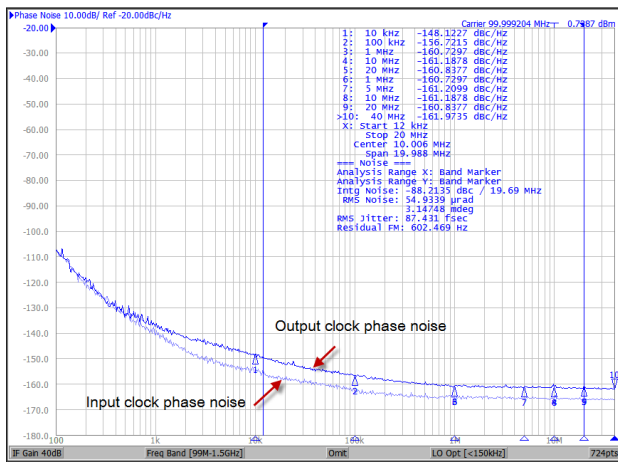


Figure 30. 100MHz LVPECL Phase Noise

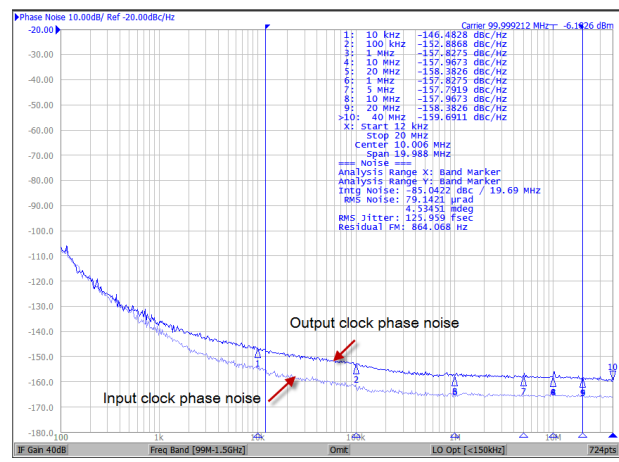


Figure 31. 100MHz LVDS Phase Noise

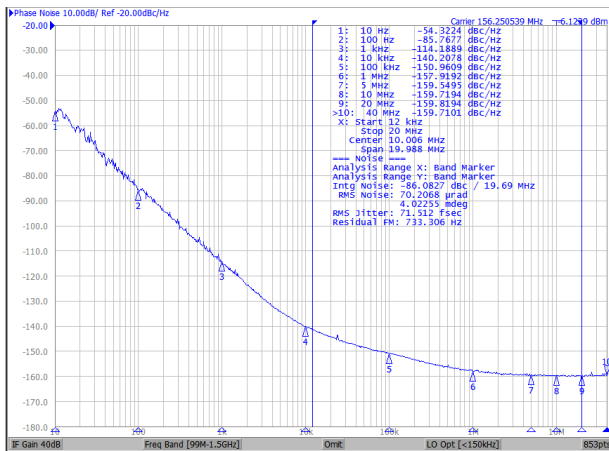


Figure 32. 156.25MHz LVDS Phase Noise in Xtal mode

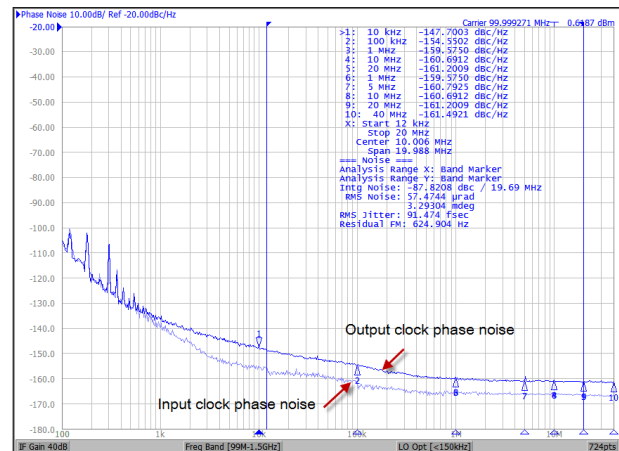


Figure 33. 100MHz HCSL Phase Noise

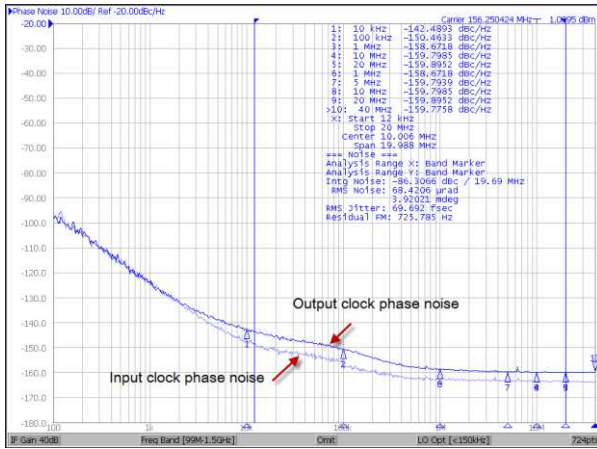


Figure 34. 156.25MHz LVPECL Phase Noise

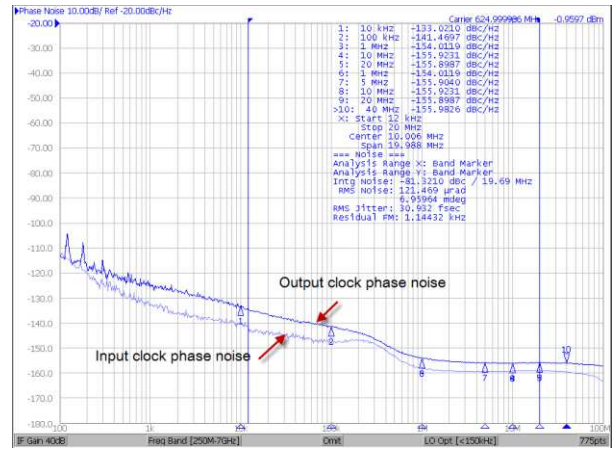


Figure 35. 625MHz LVPECL Phase Noise

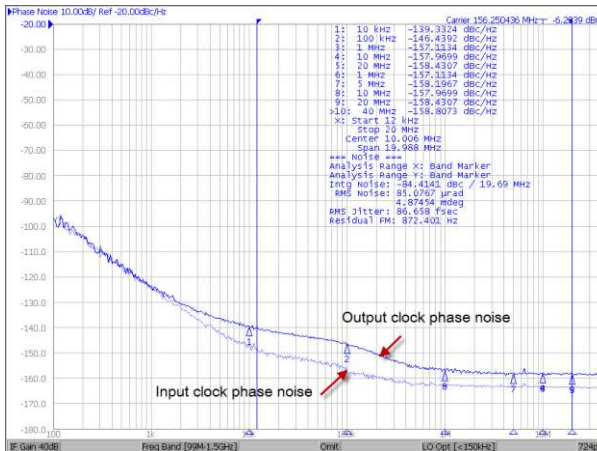


Figure 36. 156.25MHz LVDS Phase Noise

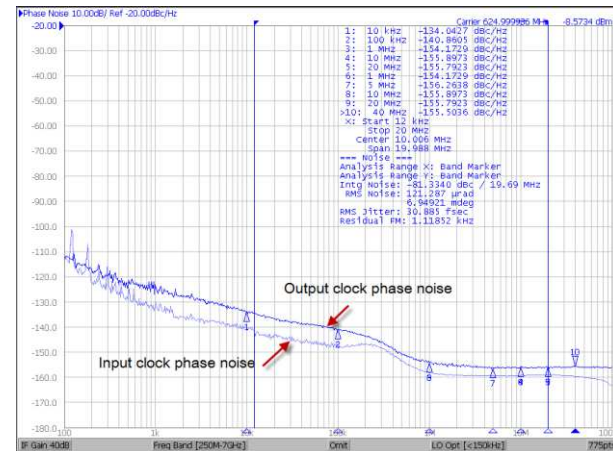


Figure 37. 625MHz LVDS Phase Noise

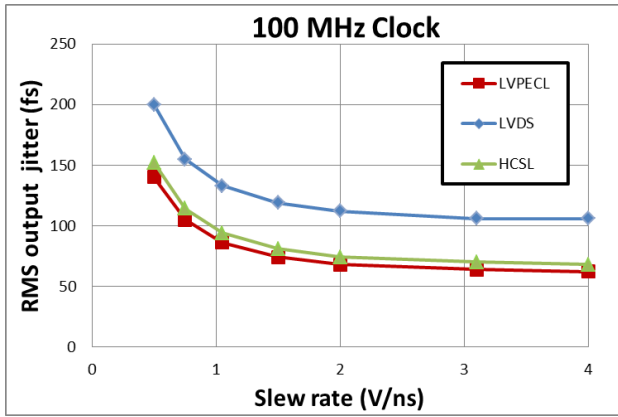


Figure 38. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

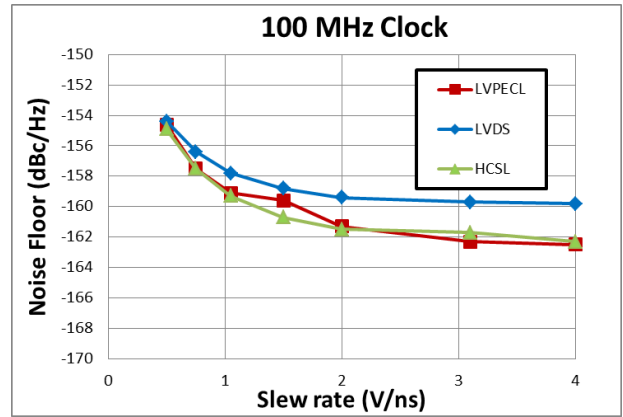


Figure 39. Output clock noise floor vs input clock slew-rate

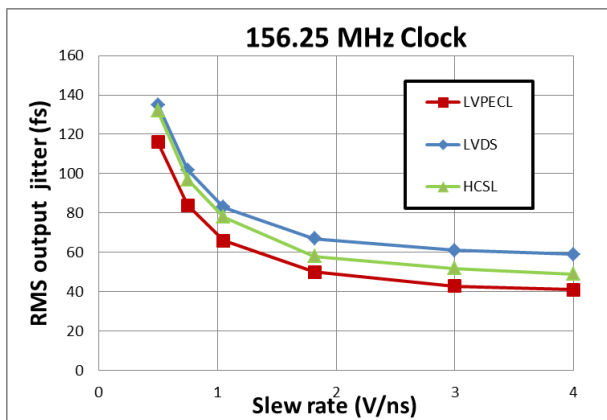


Figure 40. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

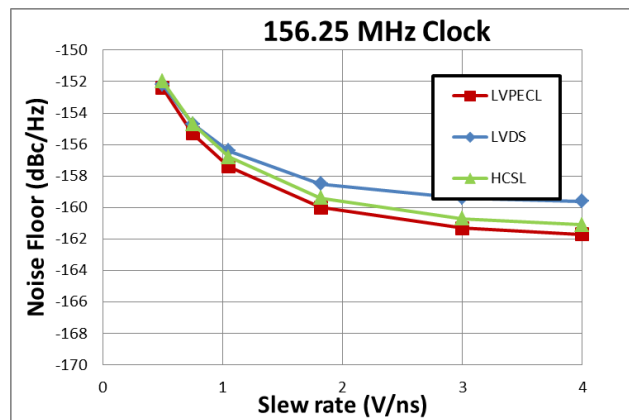


Figure 41. Output clock noise floor vs input clock slew-rate

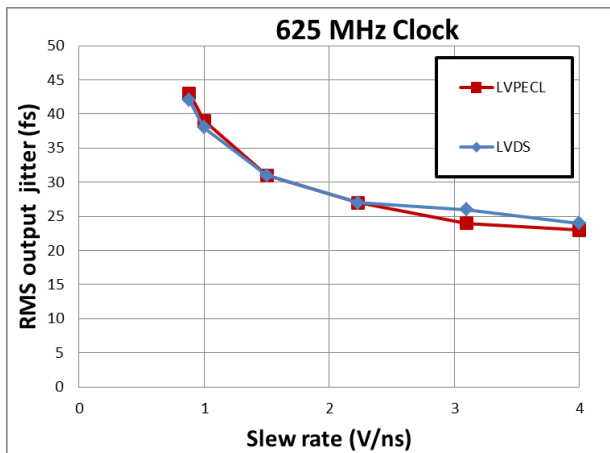


Figure 42. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

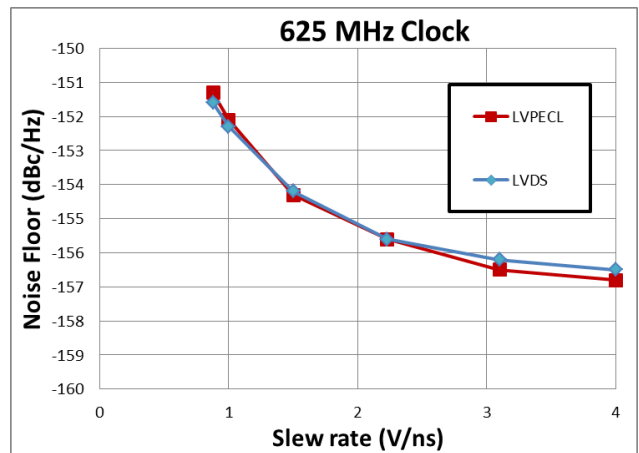


Figure 43. Output clock noise floor vs input clock slew-rate



## Register Map

The device is controlled by accessing registers through the serial interface. The following table provides a summary of the registers available for the configuration of the device.

**Table 4 Register Map**

Address SPI A[6:0] Hex (0x)	Name	Data D[7:0]
00	XTALBG	xtal_buf_gain[7:0]
01	XTALDL	xtal_drive_level[7:0]
02	XTALLC	xtal_load_cap[7:0]
03	XTALNR	xtal_normal_run
04	-	Not used
05	INSEL	input_select[1:0]
06	OUTLOW	output_drive_low
07	DRVTYPEA	{driver_type[5:4], 4'bxxxx} (differential output 1 and 0)
08	-	Not used
09	DRVTYPEB	{driver_type[17:12], 2'bxx} (differential output 4, 3, and 2)
0A	-	Not used
0B	CMOSDIV	cmos_div[2:0] (cmos)
0C	CMOSOUTEN	output_enable (cmos)
0D	CMOSDRVSTR	driver_strength (cmos)
0E	-	Not used
0F/11	Reserved	Leave as default
11	DEVID	Device ID
12 to 1F	Reserved	Leave as default

Address	0x00			Hex
XTALBG		XTAL Buffer Gain		
Bit	Name	Description	Type	Reset
7:0	xtal_buf_gain[7:0]	<p>Programs crystal buffer (inverting amplifier) gain. Every bit pair (bits: 01, 23, 45, 67) of this register correspond to additional equal gain block which can be added (bits set) or removed (bits cleared). Minimum gain is 0x00 (default) and 0xFF is maximum gain. When reference input mode is "bypass XTAL mode" or "differential input modes" with HIGH xtal_normal_run bit, the buffer is disabled and follows "Input Selection". When xtal_normal_run bit is LOW, XTAL buffer is in the "xtal forced run" mode and keep running.</p> <p><b>8'b0000_0000: default crystal buffer strength.</b>            8'b0000_0011: enable additional buffer strength            8'b0000_1100: enable additional buffer strength            8'b0011_0000: enable additional buffer strength            8'b1100_0000: enable additional buffer strength</p>	RW	FF

Address	0x01			Hex
XTALDL		XTAL Drive Level		
Bit	Name	Description	Type	Reset
7:0	xtal_drive_level[7:0]	<p>Internal damping resistance of crystal circuit to limit external crystal's drive level uW. The value of damping resistor is determined by crystal's motion resistance of crystal's equivalent circuit. Drive level should be lower than crystal manufacturer's specification. Crystal's equivalent values should be requested to the manufacturer, (motion resistance and shunt capacitance). The selected resistors are connected to XOUT. Multiple bit combinations available by 7-bit control. Because they use parallel connections, 0xFF is the smallest resistance and 0x01 is the highest resistance.</p> <p>8'b0000_0000: disable all resistors            8'b0000_0001: 312 Ohm resistor            8'b0000_0010: 161 Ohm resistor            8'b0000_0100: 84 Ohm resistor            8'b0000_1000: 42 Ohm resistor            8'b0001_0000: 21 Ohm resistor            8'b0010_0000: 10.5 Ohm resistor            8'b0100_0000: 0 Ohm connection            8'b1000_0000: not used</p>	RW	04