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ZL40250–ZL40253 SmartBuffer™

6- or 10-Output Programmable Fanout Buffers with Multi-Format I/O and Dividers

Data Sheet

December 2016

Features

- **Four Flexible Input Clocks**
  - One crystal/CMOS input
  - Two differential/CMOS inputs
  - One single-ended/CMOS input
  - Any input frequency up to 1GHz (300MHz for CMOS)
  - Manual clock switching by pin or register
- **6 or 10 Universal Output Clocks with Dividers**
  - Each output has independent divider
  - Low additive jitter <200fs RMS (12kHz-20MHz, for input frequencies ≥100MHz)
  - Each output configurable as LVDS, LVPECL, HCSL, 2xCMOS or HSTL
  - In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)*
  - Multiple output supply voltage banks with CMOS output voltages from 1.5V to 3.3V
  - Precise output alignment circuitry from GPIO pin or register bit*
  - Per-output skew adjustment*
  - Per-output enable/disable and glitchless start/stop (stop high or low)*

Ordering Information

ZL40250LDG1	ext. EEPROM	6 Outputs	Trays
ZL40250LDF1	ext. EEPROM	6 Outputs	Tape and Reel
ZL40251LDG1	int. EEPROM	6 Outputs	Trays
ZL40251LDF1	int. EEPROM	6 Outputs	Tape and Reel
ZL40252LDG1	ext. EEPROM	10 Outputs	Trays
ZL40252LDF1	ext. EEPROM	10 Outputs	Tape and Reel
ZL40253LDG1	int. EEPROM	10 Outputs	Trays
ZL40253LDF1	int. EEPROM	10 Outputs	Tape and Reel

Matte Tin
Package size: 8 x 8 mm, 56 Pin QFN
-40°C to +85°C

- **General Features**
  - Automatic self-configuration at power-up from external (ZL40250 or 2) or internal (ZL40251 or 3) EEPROM; up to 8 configurations pin-selectable
  - Four multi-purpose I/O pins
  - SPI or I^2C processor Interface
  - Core supply voltage options: 2.5V only, 3.3V only, 1.8V+2.5V or 1.8V+3.3V
  - Space-saving 8x8mm QFN56 (0.5mm pitch)
  - Easy-to-use evaluation/programming software

Applications

- Clock signal fanout, format conversion, frequency division and skew adjustment in a wide variety of equipment types

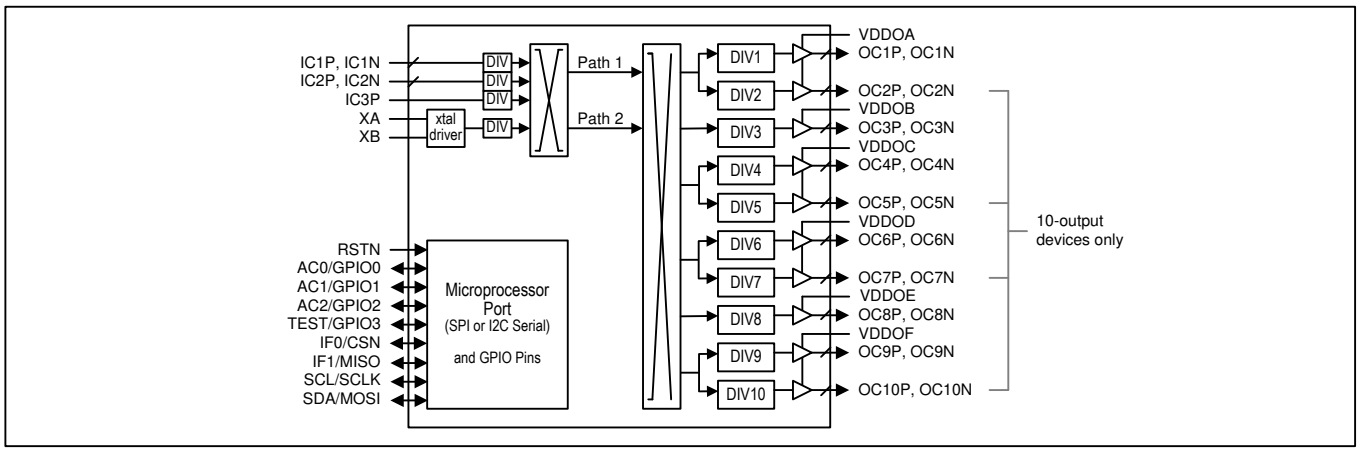

Figure 1 - Functional Block Diagram

* some features require a higher-frequency input clock and enabling the output dividers

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1. Application Examples

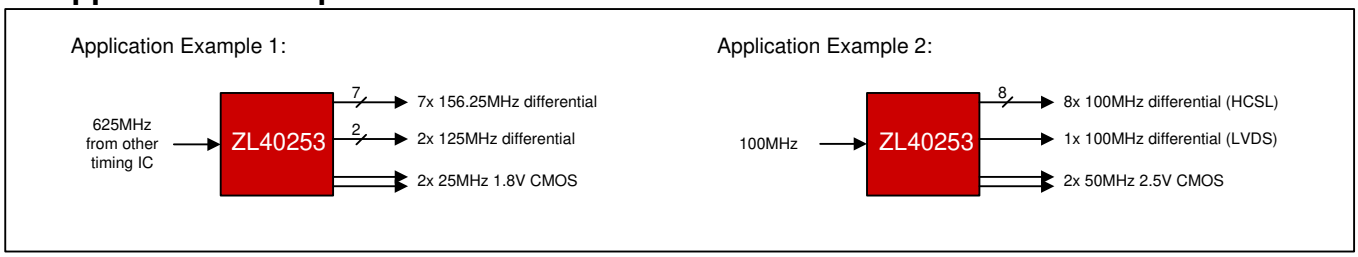

Figure 2 - Application Examples: Ethernet and PCIe Clocks

2. Pin Diagram

The device is packaged in a 8x8mm 56-pin QFN.

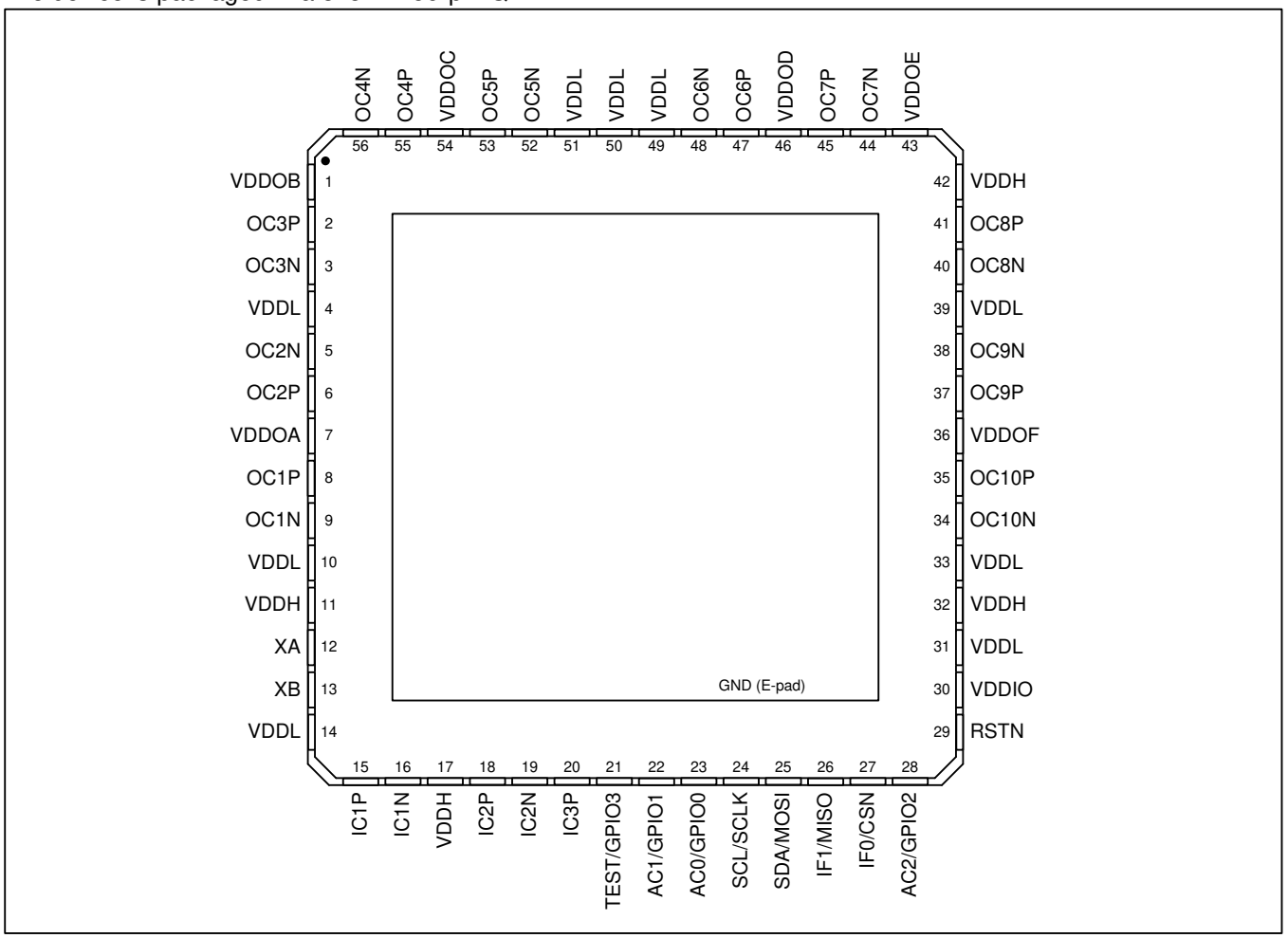

Figure 3 - Pin Diagram

3. Pin Descriptions

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – input, O – output, A – analog, P – power supply pin. All GPIO and SPI/I^2C interface pins have Schmitt-trigger inputs and have output drivers that can be disabled (high impedance).

Table 1 - Pin Descriptions

Pin #	Name	Type	Description
15, 16 18, 19 20	IC1P, IC1N IC2P, IC2N IC3P	I I I	**Input Clock Pins** Differential or Single-ended signal format. Programmable frequency. *Differential:* See Table 9 for electrical specifications, and see Figure 14 for recommended external circuitry for interfacing these differential inputs to LVDS, LVPECL, CML or HSCL output pins on neighboring devices. *Single-ended:* For input signal amplitude >2.5V, connect the signal directly to ICxP pin. For input signal amplitude ≤2.5V, AC-coupling the signal to ICxP is recommended. Connect the N pin to a capacitor (0.1µF or 0.01µF) to VSS. As shown in Figure 14, the ICxP and ICxN pins are internally biased to approximately 1.3V. Treat the ICxN pin as a sensitive node; minimize stubs; do not connect to anything else including other ICxN pins. *Unused:* Set ICEN.ICxEN=0. The ICxP and ICxN pins can be left floating. Note that the IC3N pin is not bonded out. A differential signal can be connected to IC3P by AC-coupling the POS trace to IC3P and terminating the signal on the driver side of the coupling cap.
12 13	XA XB	A / I	**Crystal or Input Clock Pins** *Crystal:* MCR1.XAB=01. An on-chip crystal driver circuit is designed to work with an external crystal connected to the XA and XB pins. See section 4.3.2 for crystal characteristics and recommended external components. *Input Clock:* MCR1.XAB=10. An external local oscillator or clock signal can be connected to the XA pin. The XB pin must be left unconnected. The signal on XA can be as large as 3.3V even when VDDH is only 2.5V.
8, 9 6, 5 2, 3 55, 56 53, 52 47, 48 45, 44 41, 40 37, 38 35, 34	OC1P, OC1N OC2P, OC2N OC3P, OC3N OC4P, OC4N OC5P, OC5N OC6P, OC6N OC7P, OC7N OC8P, OC8N OC9P, OC9N OC10P, OC10N	O	**Output Clock Pins** LVDS, programmable differential (which includes LVPECL), HCSL, HSTL or 1 or 2 CMOS. Programmable frequency. Programmable VCM and VOD in programmable differential mode. Programmable drive strength in CMOS and HSTL modes. See Figure 16 for example external interface circuitry. See Table 10, Table 11 and Table 12 for electrical specifications for LVDS, LVPECL and HCSL, respectively. See Table 13 for electrical specifications for interfacing to CMOS and HSTL inputs on neighboring devices. Outputs OC2, OC5, OC7 and OC10 are not present on 6-output products.
29	RSTN	I	**Reset (Active Low)** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as RSTN is low. Minimum low time is 1µs.
23 22 28	AC0/GPIO0 AC1/GPIO1 AC2/GPIO2	I/O	**Auto-Configure [2:0] / General Purpose I/O 0, 1 and 2** *Auto Configure:* On the rising edge of RSTN these pins behave as AC[2:0] and specify one of the configurations stored in ROM or EEPROM. See section 4.2.

Pin #	Name	Type	Description
			General-Purpose I/O: After reset these pins are GPIO0, GPIO1 and GPIO2. GPIOCR1 and GPIOCR2.GPIO2C configure these pins. Their states are indicated in GPIOSR which has both real-time and latched status bits.
21	TEST/GPIO3	I/O	**Factory Test / General Purpose I/O 3** *Factory Test:* On the rising edge of RSTN the pin behaves as TEST. Factory test mode is enabled when TEST is high. For normal operation TEST must be low on the rising edge of RSTN. *General-Purpose I/O:* After reset this pin is GPIO3. GPIOCR2.GPIO3C configures the pin. Its state is indicated in GPIOSR which has both real-time and latched status bits.
27	IF0/CSN	I/O	**Interface Mode 0 / SPI Chip Select (Active Low)** *Interface Mode:* On the rising edge of RSTN the pin behaves as IF0 and, together with IF1, specifies the interface mode for the device. See section 4.2. *SPI Chip Select:* After reset this pin is CSN. When the device is configured as a SPI slave, an external SPI master must assert (low) CSN to access device registers. When the device is configured as a SPI master (ZL40250, ZL40252 only), the device asserts CSN to access an external SPI EEPROM during auto-configuration and then changes CSN to an input during normal operation. CSN should not be allowed to float.
26	IF1/MISO	I/O	**Interface Mode 1 / SPI Master-In-Slave-Out** *Interface Mode:* On the rising edge of RSTN the pin behaves as IF1 and, together with IF0, specifies the interface mode for the device. See section 4.2. *SPI MISO:* After reset this pin is MISO. When the device is configured as a SPI slave, the device outputs data to an external SPI master on MISO during SPI read transactions. When the device is configured as a SPI master (ZL40250, ZL40252 only), the device receives data on MISO from an external SPI EEPROM during auto-configuration.
24	SCL/SCLK	I/O	**I^2C Clock / SPI Clock** *I^2C Clock:* When the device is configured as an I^2C slave, an external I^2C master must provide the I^2C clock signal on the SCL pin. *SPI Clock:* When the device is configured as a SPI slave, an external SPI master must provide the SPI clock signal on SCLK. When the device is configured as a SPI master (ZL40250, ZL40252 only), the device drives SCLK as an output to clock accesses to an external SPI EEPROM during auto-configuration.
25	SDA/MOSI	I/O	**I^2C Data / SPI Master-Out-Slave-In** *I^2C Data:* When the device is configured as an I^2C slave, SDA is the bidirectional data line between the device and an external I^2C master. *SPI MOSI:* When the device is configured as a SPI slave, an external SPI master sends commands, addresses and data to the device on MOSI. When the device is configured as a SPI master (ZL40250, ZL40252 only), the device sends commands, addresses and data on MOSI to an external SPI EEPROM during auto-configuration.
11,17, 32,42	VDDH	P	**Higher Core Power Supply.** 2.5V or 3.3V ±5%. When VDDH=3.3V the device has additional internal power supply regulators enabled.

Pin #	Name	Type	Description
4,10, 14,31, 33,39, 49,50, 51	VDDL	P	**Lower Core Power Supply.** 1.8V ±5% or same voltage as VDDH.
30	VDDIO	P	**Digital Power Supply for Non-Clock I/O Pins.** 1.8V to VDDH.
7	VDDOA	P	**Power Supply for OC1P/N and OC2P/N.** 1.5V to VDDH.
1	VDDOB	P	**Power Supply for OC3P/N.** 1.5V to VDDH.
54	VDDOC	P	**Power Supply for OC4P/N and OC5P/N.** 1.5V to VDDH.
46	VDDOD	P	**Power Supply for OC6P/N and OC7P/N.** 1.5V to VDDH.
43	VDDOE	P	**Power Supply for OC8P/N.** 1.5V to VDDH.
36	VDDOF	P	**Power Supply for OC9P/N and OC10P/N.** 1.5V to VDDH.
E-pad	VSS	P	**Ground.** 0 Volts.

Important Note: The voltages on VDDL, VDDIO, and all VDDOx pins must not exceed VDDH. Not complying with this requirement may damage the device.

4. Functional Description

4.1 Device Identification

The 12-bit read-only ID field and the 4-bit revision field are found in the ID1 and ID2 registers. Contact the factory to interpret the revision value and determine the latest revision.

4.2 Pin-Controlled Automatic Configuration at Reset

The device configuration is determined at reset (i.e. on the rising edge of RSTN) by the signal levels on these device pins: TEST/GPIO3, AC2/GPIO2, AC1/GPIO1, AC0/GPIO0, IF1/MISO and IF0/CSN. For these pins, the first name (TEST, AC2, AC1, AC0, IF1, IF0) indicates their function when they are sampled by the rising edge of the RSTN pin. The second name refers to their function after reset. The values of these pins are latched into the CFGSR register when RSTN goes high. To ensure the device properly samples the reset values of these pins, the following guidelines should be followed:

1. Any pullup or pulldown resistors used to set the value of these pins at reset should be 1kΩ.
2. RSTN must be asserted at least as long as specified in section 4.9.

The hardware configuration pins are grouped into three sets:

1. TEST - Manufacturing test mode
2. IF[1:0] – Microprocessor interface mode and I^2C address
3. AC[2:0] – Auto-config configuration number (0 to 7)

The TEST pin selects manufacturing test modes when TEST=1 (the AC[2:0] pins specify the test mode). For ZL40251 and ZL40253 (devices with internal EEPROM), TEST=1, AC[2:0]=000, IF[1:0]=11 configures the part so that production SPI EEPROM programmers can program the internal EEPROM (see section 4.11.2). TEST=1 and AC[2:0]=011 causes the part to start normally except it does not auto-configure from EEPROM or ROM. For more information about auto-configuration from EEPROM or ROM see section 4.11.

For all of these pins Microsemi recommends that board designs include component sites for both pullup and pulldown resistors (only one or the other populated per pin).

4.2.1 ZL40250 and ZL40252—Internal ROM, External or No EEPROM

For these part numbers the IF[1:0] pins specify the processor interface mode, the I^2C slave address and whether the device should auto-configure from internal ROM or external EEPROM. The AC[2:0] pins specify which device configuration in the ROM or EEPROM to execute after reset. Descriptions of the standard-product ROM configurations are available from Microsemi.

IF1	IF0	Processor Interface	Configuration Memory to Use
0	0	I^2C, slave address 11101 00	Internal ROM
0	1	I^2C, slave address 11101 01	Internal ROM
1	0	SPI Slave	Internal ROM
1	1	SPI Master during auto-configuration then SPI Slave	External SPI EEPROM

To configure the device as specified in the first three rows above but *without* auto-configuring from internal ROM, wire devices pins as follows: TEST=1 and AC[2:0]=011, as described in section 4.2.

AC2	AC1	AC0	Auto Configuration
0	0	0	Configuration 0
0	0	1	Configuration 1
0	1	0	Configuration 2
0	1	1	Configuration 3
1	0	0	Configuration 4
1	0	1	Configuration 5
1	1	0	Configuration 6
1	1	1	Configuration 7

Notes about the device auto-configuring from external EEPROM:

1. The device's CSN pin should have a pull-up resistor to VDD to ensure its processor interface is inactive after auto-configuration is complete. The SCLK, MISO and MOSI pins should also have pull-up resistors to VDD to keep them from floating.
2. If a processor or similar device will access device registers after the device has auto-configured from external EEPROM, the SPI SCLK, MOSI and MISO wires can be connected directly to the processor, the device and the external EEPROM. The processor and device CSN pins can be wired together also. The EEPROM CSN signal must be controlled by the device's CSN pin during device auto-configuration and then held inactive when the processor accesses device registers.
3. The bits of the I^2C address are as shown above by default but can be changed in the I2CA register.

4.2.2 ZL40251 and ZL40253—Internal EEPROM

For these part numbers the IF[1:0] pins specify the processor interface mode and the I^2C slave address. The AC[2:0] pins specify which device configuration in the EEPROM to execute after reset.

IF1	IF0	Processor Interface
0	0	I^2C, slave address 11101 00
0	1	I^2C, slave address 11101 01
1	0	I^2C, slave address 11101 10
1	1	SPI Slave

AC2	AC1	AC0	Auto Configuration
0	0	0	Configuration 0
0	0	1	Configuration 1
0	1	0	Configuration 2
0	1	1	Configuration 3
1	0	0	Configuration 4
1	0	1	Configuration 5
1	1	0	Configuration 6
1	1	1	Configuration 7

Note: the bits of the I^2C address are as shown above by default but can be changed in the I2CA register. A device's I^2C slave address can be set to any value during auto-configuration at power-up by writing the I2CA register as part of the configuration script.

4.3 Local Oscillator or Crystal

Section 4.3.1 describes how to connect an external oscillator and the required characteristics of the oscillator. Section 4.3.2 describes how to connect an external crystal to the on-chip crystal driver circuit and the required characteristics of the crystal. The device does not require an external oscillator or crystal for operation.

4.3.1 External Oscillator

A signal from an external oscillator can be connected to the XA pin (XB must be left unconnected).

Table 8 specifies the range of possible frequencies for the XA input. To minimize jitter, the signal must be properly terminated and must have very short trace length. A poorly terminated single-ended signal can greatly increase output jitter, and long single-ended trace lengths are more susceptible to noise. When MCR1.XAB=10, XA is enabled as a single-ended input.

4.3.2 External Crystal and On-Chip Driver Circuit

The on-chip crystal driver circuit is designed to work with a fundamental mode, AT-cut crystal resonator. See Table 2 for recommended crystal specifications. To enable the crystal driver, set MCR1.XAB=01.

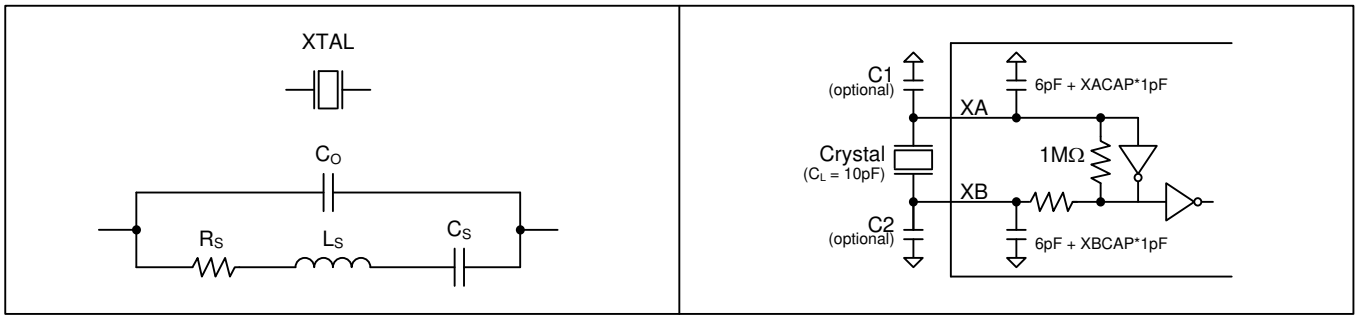

Figure 4 - Crystal Equivalent Circuit / Recommended Crystal Circuit

See Figure 4 for the crystal equivalent circuit and the recommended external component connections. The driver circuit design includes configurable internal load capacitors. For a 10pF crystal the total capacitance on each of XA and XB should be 2 x 10pF = 20pF. To achieve these loads without external capacitors, register field XACR3.XACAP should be set to 20pF minus actual XA external board trace capacitance minus XA's minimum internal capacitance of 6pF. For example, if external trace capacitance is 2pF then XACAP should be set to 20pF – 2pF – 6pF = 12pF. Register field XACR3.XBCAP should be set in a similar manner for XB load capacitance. Crystals with nominal load capacitance other than 10pF usually can be supported with only internal load capacitance. If the XACAP and XBCAP fields do not have sufficient range for the application, capacitance can be increased by using external caps C1 and C2.

Users should also note that on-chip capacitors are not nearly as accurate as discrete capacitors (which can have 1% accuracy). If tight frequency accuracy is required for the crystal driver circuit then set XACAP and XBCAP both to 0 and choose appropriate C1 and C2 capacitors with 1% tolerance.

The crystal, traces, and two external capacitors sites (if included) should be placed on the board as close as possible to the XA and XB pins to reduce crosstalk of active signals into the oscillator. Also no active signals should be routed under the crystal circuitry.

Note: Crystals have temperature sensitivies that can cause frequency changes in response to ambient temperature changes. In applications where significant temperature changes are expected near the crystal, it is recommended that the crystal be covered with a thermal cap, or an external XO or TCXO should be used instead.

Table 2 - Crystal Selection Parameters

Parameter	Symbol	Min.	Typ.	Max.	Units
Crystal Oscillation Frequency[1]	f_{OSC}	25		60	MHz
Shunt Capacitance	C_O		2	5	pF
Load Capacitance[3]	C_L	8	10	16	pF

Parameter		Symbol	Min.	Typ.	Max.	Units
Equivalent Series Resistance (ESR)[2]	f_{OSC} < 40MHz	R_S			60	Ω
	f_{OSC} > 40MHz	R_S			50	Ω
Maximum Crystal Drive Level			100	100, 200, 300		µW

Note 1: Higher frequencies give lower output jitter, all else being equal.
Note 2: These ESR limits are chosen to constrain crystal drive level to less than 100µW. If the crystal can tolerate a drive level greater than 100µW then proportionally higher ESR is acceptable.
Note 3: For crystals with 100µW max drive level: (a) f_{OSC}>55MHz and C_L≥12pF is not supported, and (b) f_{OSC}>45MHz and C_L≥16pF is not supported. Crystals with max drive level of 200µW or higher do not have these limitations.

Parameter	Symbol	Min.	Typ.	Max.	Units
Crystal Frequency Stability vs. Power Supply	f_{FVD}		0.2	0.5	ppm per 10% Δ in VDD

4.3.3 Ring Oscillator (for Auto-Configuration)

After reset the internal auto-configuration boot controller is clocked by an internal ring oscillator. After auto-configuration is complete (GLOBISR.BCDONE=1) the ring oscillator can be disabled by setting MCR1.ROSCD=1. The device's processor interface is asynchronous and does not require the ring oscillator.

4.4 Input Signal Format Configuration

Input clocks IC1, IC2 and IC3 are enabled by setting the enable bits in the ICEN register. The power consumed by a differential receiver is shown in Table 6. The electrical specifications for these inputs are listed in Table 9. Each input clock can be configured to accept nearly any differential signal format by using the proper set of external components (see Figure 14). To configure these differential inputs to accept single-ended CMOS signals, connect the single-ended signal to the ICxP pin, and connect the ICxN pin to a capacitor (0.1µF or 0.01µF) to VSS. Each ICxP and ICxN pin is internally biased to approximately 1.3V. If an input is not used, both ICxP and ICxN pins can be left floating. Note that the IC3N pin is not present. A differential signal can be connected to IC3P by AC-coupling the POS trace to IC3P and terminating the signal on the driver side of the coupling cap.

4.5 Path 1 and Path 2 Signal Selection

The device has two internal fanout paths, each with its own input mux. See the block diagram in Figure 1. Each bank of outputs can be connected to either path using the appropriate field in the OCMUX registers.

The Path 1 input mux can select any of inputs IC1 through IC3, a clock signal on XA, or the crystal driver circuit when a crystal is connected to XA and XB. The input to Path 1 can be controlled by a register field or a GPIO pin. When P1CR3.EXTSW=0, the P1CR3.MUX register field controls the Path 2 input mux.

When P1CR3.EXTSW=1, a GPIO pin controls the Path 1 input mux. When the GPIO pin is low, the mux selects the input specified by P1CR3.MUX. When the GPIO pin is high, the mux selects the input specified by P1CR3.ALTMUX. P1CR1.EXTSS specifies which GPIO pin controls this behavior.

The P1SR.SELREF real-time status field indicates Path 2's selected reference.

Path 2 has identical register fields to those of Path 1 in the P2CR1, P2CR3 and P2SR registers.

4.6 Output Clock Configuration

The ZL40250 and ZL40251 have six output clock signal pairs while the ZL40252 and ZL40253 have ten. Each output has individual divider, enable and signal format controls. In CMOS mode each signal pair can become two CMOS outputs, allowing the device to have up to 12 or 20 output clock signals. Also in CMOS mode, the OCxN pin can have an additional divider allowing the OCxN frequency to be an integer divisor of the OCxP frequency (example: OC3P 125MHz and OC3N 25MHz). The outputs can be aligned relative to each other, and the phases of output signals can be adjusted dynamically with high resolution.

4.6.1 Output Enable, Signal Format, Voltage and Interfacing

To use an output, the output driver must be enabled by setting OCxCR2.OCSF≠0, and the per-output dividers must be enabled by setting the appropriate bit in the OCEN register. The per-output dividers include the medium-speed divider, the low-speed divider and the associated phase adjustment/alignment circuitry and start/stop logic.

Using the OCxCR2.OCSF register field, each output pair can be disabled or configured as LVDS, LVPECL, HCSL, HSTL, or one or two CMOS outputs. When an output is disabled it is high impedance, and the output driver is in a low-power state. In CMOS mode, the OCxN pin can be disabled, in-phase or inverted vs. the OCxP pin. All of these options are specified by OCxCR2.OCSF. The clock to the output driver can inverted by setting OCxCR2.POL=1. The CMOS/HSTL output driver can be set to any of four drive strengths using OCxCR2.DRIVE.

When OCxCR2.OCSF=0001 the output driver is in LVDS mode. V_{OD} is forced to 400mV and OCxDIFF.VOD is ignored. V_{CM} can be configured in OCxDIFF.VCM, but the default value of 0000 is typically used to get V_{CM}=1.23V for LVDS.

When OCxCR2.OCSF=0010 the output driver is in programmable differential mode. In this mode the output swing (V_{OD}) can be set in OCxDIFF.VOD and the common-mode voltage can be set in OCxDIFF.VCM. Together these fields allow the output signal to be customized to meet the requirements of the clock receiver and minimize the need for external components. By default, when OCSF=0010 the output is configured for LVPECL signal swing with a 1.23V common mode voltage. This gives a signal that can be AC-coupled (after a 100Ω termination resistor) to receivers that are LVPECL or that require a larger signal swing than LVDS. The output driver can also be configured for LVPECL output with standard 2.0V common-mode voltage by seting OCxDIFF.VCM for 2.0V and setting OCxREG.VREG appropriately.

In both LVDS mode and programmable differential mode the output driver requires a DC path through a 100Ω resistor between OCxP and OCxN for proper operation. This resistor is usually placed as close as possible to the receiver inputs to terminate the differential signal. If the receiver requires a common-mode voltage that cannot be matched by the output driver then the POS and NEG signals can be AC-coupled to the receiver after the 100Ω resistor.

HCSL mode requires a DC path through a 50Ω resistor to ground on each of OCxP and OCxN. Note that each of the OCxDIFF.VCM, OCxDIFF.VOD and OCxREG.VREG register fields has a particular setting required for HCSL signal format. See the descriptions of these fields for details.

Outputs are grouped into six power supply banks, VDDOA through VDDOF to allow CMOS or HSTL signal swing from 1.5V to 3.3V for glueless interfacing to neighboring components. 10-output products have outputs grouped into banks in a 2-1-2-2-1-2 arrangement, as shown in Figure 1. 6-output products have one output per bank. If OCSF is set to HSTL mode then a 1.5V power supply voltage should be used to get a standards-compliant HSTL output. Note that LVDS, LVPECL and HCSL signal formats must have a power supply of 2.5V or 3.3V. Also note that VDDO voltage must not exceed VDDH voltage.

4.6.2 Output Frequency Configuration

The frequency of each output is determined by the output bank source signal and the per-output dividers. Each bank of outputs can be connected to Path 1 or Path 2 using the appropriate field in the OCMUX registers.

Each output has two output dividers, a 7-bit medium-speed divider (OCxCR1.MSDIV) and a 24-bit low-speed output divider (LSDIV field in the OCxDIV registers). These dividers are in series, medium-speed divider first then output divider. These dividers produce signals with 50% duty cycle for all divider values including odd numbers. The low-speed divider can only be used if the medium-speed divider is used (i.e. OCxCR1.MSDIV>0).

Since each output has its own independent dividers, the device can output families of related frequencies that have a path frequency as a common multiple. For example, for Ethernet clocks, a 625MHz Path 1 clock can be divided by four for one output to get 156.25MHz, divided by five for another output to get 125MHz, and divided by 25 for another output to get 25MHz. Similarly, for SDH/SONET clocks, a 622.08MHz Path 1 clock can be divided by 4 to get 155.52MHz, by 8 to get 77.76MHz, by 16 to get 38.88MHz or by 32 to get 19.44MHz.

Two Different Frequencies in 2xCMOS Mode

When an output is in 2xCMOS mode it can be configured to have the frequency of the OCxN clock be an integer divisor of the frequency of the OCxP clock. Examples of where this can be useful:

- 125MHz on OCxP and 25MHz on OCxN for Ethernet applications
- 77.76MHz on OCxP and 19.44MHz on OCxN for SONET/SDH applications
- 25MHz on OCxP and 1Hz (i.e. 1PPS) on OCxN for telecom applications with Synchronous Ethernet and IEEE1588 timing

An output can be configured to operate like this by setting the LSDIV value in the OCxDIV registers to OCxP_freq / OCxN_freq - 1 and setting OCxCR3.LSSEL=0 and OCxCR3.NEGLSD=1. Here are some notes about this dual-frequency configuration option:

- In this mode only the medium speed divider is used to create the OCxP frequency. The low-speed divider is then used to divide the OCxP frequency down to the OCxN frequency. This means that the lowest OCxP frequency is the bank source frequency divided by 128.
- An additional constraint is that the medium-speed divider must be configured to divide by 2 or more (i.e. must have OCxCR1.MSDIV≥1).

4.6.3 Output Duty Cycle Adjustment

The duty cycle of the output clock can be modified using the OCxDC.OCDC register field. This behavior is only available when MSDIV>0 and LSDIV > 1. When OCDC = 0 the output clock is 50%. Otherwise the clock signal is a pulse with a width of OCDC number of MSDIV output clock periods. The range of OCDC can create pulse widths of 1 to 255 MSDIV output clock periods. When OCxCR2.POL=0, the pulse is high and the signal is low the remainder of the cycle. When POL=1, the pulse is low and the signal is high the remainder of the cycle.

Note that duty cycle adjustment is done in the low-speed divider. Therefore when OCxCR3.LSSEL=0 the duty cycle of the output is not affected. Also, when a CMOS output is configured with OCxCR3.LSSEL=0 and OCxCR3.NEGLSD=1, the OCxN pin has duty cycle adjustment but the OCxP pin does not. This allows a higher-speed 50% duty cycle clock signal to be output on the OCxP pin and a lower-speed frame/phase/time pulse (e.g. 2kHz, 8kHz or 1PPS) to be output on the OCxN pin at the same time.

An output configured for CMOS or HSTL signal format should not be configured to have a duty cycle with high time shorter than 2ns or low time shorter than 2ns.

4.6.4 Output Phase Adjustment

The phase of an output signal can be shifted by 180° by setting OCxCR2.POL=1. In addition, the phase can be adjusted using the OCxPH.PHADJ register field. The adjustment is in units of bank source clock cycles. For example, if the bank source clock is 625MHz then one bank source clock cycle is 1.6ns, the smallest phase adjustment is 0.8ns, and the adjustment range is ±5.6ns.

4.6.5 Output-to-Output Phase Alignment

A 0-to-1 transition of the P1CR1.DALIGN bit causes a simultaneous reset of the medium-speed dividers and low-speed dividers for all output clocks following Path 1 where OCxCR1.PHEN=1. After this reset, all PHEN=1 output clocks with frequencies that are exactly integer multiples of one another are rising-edge aligned, with the phase of each output clock signal adjusted as specified by its OCxPH.PHADJ register field. Similarly a 0-to-1 transition of the P2CR1.DALIGN bit aligns all output clocks following Path 2 where OCxCR1.PHEN=1. Alignment is not glitchess; i.e. it may cause a short high time or low time on participating output clock signals. A glitchless alignment can be accomplished by first stopping the clocks, then aligning them, then starting them. Output clock start and stop is described in section 4.6.6.

4.6.6 Output Clock Start and Stop

Output clocks can be stopped high or low or high-impedance. One use for this behavior is to ensure “glitchless” output clock operation while the output is reconfigured or phase aligned with some other signal.

Each output has an OCxSTOP register with fields to control this behavior. The OCxSTOP.MODE field specifies whether the output clock signal stops high, low, or high-impedance. The OCxSTOP.SRC field specifies the source of the stop signal. Options include control bits or one of the GPIO pins. When OCxSTOP.SRC=0001 the output clock is stopped when the corresponding bit is set in the STOPCR registers OR the MCR1.STOP bit is set.

When the stop mode is Stop High (OCxSTOP.MODE=x1) and the stop signal is asserted, the output clock is stopped after the next rising edge of the output clock. When the stop mode is Stop Low (OCxSTOP.MODE=x0) and the stop signal is asserted, the output clock is stopped after the next falling edge of the output clock. When the output is stopped, the output driver can optionally go high-impedance (OCxSTOP.MODE=1x). Internally the clock signal continues to toggle while the output is stopped. When the stop signal is deasserted, the output clock resumes on the opposite edge that it stopped on. Low-speed output clocks can take long intervals before being stopped after the stop signal goes active. For example, a 1 Hz output could take up to 1 second to stop.

When OCxCR2.POL=1 the output stops on the opposite polarity that is specified by the OCxSTOP.MODE field.

Generally OCxCR1.MSDIV must be > 0 for this function to operate correctly since MSDIV=0 bypasses the start-stop circuits.

When MSDIV=0, OCxSTOP.MODE=11 (stop high then go high-impedance) can be used to make outputs high-impedance, but the action won't necessarily be glitchless. To use this behavior to get "stop *low* then go-impedance" behavior, OCxCR2.POL can be set to 1.

Note that when OCxCR3.NEGLSD=1 the start-stop logic is bypassed for the OCxN pin, and OCxN may not start/stop without glitches.

Each output has a status register (OCxSR) with several stop/start status bits. The STOPD bit is a real-time status bit indicating stopped or not stopped. The STOPL bit is a latched status bit that is set when the output clock has stopped. The STARTL bit is a latched status bit that is set when the output clock has started.

4.7 Microprocessor Interface

The device can communicate over a SPI interface or an I^2C interface.

In SPI mode ZL4025x devices without internal EEPROM can be configured at reset to be a SPI slave to a processor master or a SPI master to an external EEPROM slave. (SPI master operation changes to SPI slave operation after auto-configuration from the external EEPROM is complete.) The ZL4025x devices with internal EEPROM can only be configured as a SPI slave to a processor master. All devices are always slaves on the I^2C bus.

Section 4.2 describes reset pin settings required to configure the device for these interfaces.

4.7.1 SPI Slave

The device can present a SPI slave port on the CSN, SCLK, MOSI, and MISO pins. SPI is a widely used master/slave bus protocol that allows a master and one or more slaves to communicate over a serial bus. SPI masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master, which also generates the SCLK signal. The device receives serial data on the MOSI (Master Out Slave In) pin and transmits serial data on the MISO (Master In Slave Out) pin. MISO is high impedance except when the device is transmitting data to the bus master.

Bit Order. The register address and all data bytes are transmitted most significant bit first on both MOSI and MISO.

Clock Polarity and Phase. The device latches data on MOSI on the rising edge of SCLK and updates data on MISO on the falling edge of SCLK. SCLK does not have to toggle between accesses, i.e., when CSN is high.

Device Selection. Each SPI device has its own chip-select line. To select the device, the bus master drives its CSN pin low.

Command and Address. After driving CSN low, the bus master transmits an 8-bit command followed by a 16-bit register address. The available commands are shown below.

Table 3 - SPI Commands

Command	Hex	Bit Order, Left to Right
Write Enable	0x06	0000 0110
Write	0x02	0000 0010
Read	0x03	0000 0011
Read Status	0x05	0000 0101

Read Transactions. The device registers are accessible when EESEL=0. On ZL4025x devices with internal EEPROM, the EEPROM memory is accessible when the EESEL bit is 1. On ZL4025x devices without internal EEROM, the EESEL bit must be set to 0. After driving CSN low, the bus master transmits the read command followed by the 16-bit address. The device then responds with the requested data byte on MISO, increments its address counter, and prefetches the next data byte. If the bus master continues to demand data, the device continues to provide the data on MISO, increment its address counter, and prefetch the following byte. The read transaction is completed when the bus master drives CSN high. See Figure 5.

Register Write Transactions. The device registers are accessible when EESEL=0. After driving CSN low, the bus master transmits the write command followed by the 16-bit register address followed by the first data byte to be written. The device receives the first data byte on MOSI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the device continues to write the data received and increment its address counter. The write transaction is completed when the bus master drives CSN high. See Figure 7.

EEPROM Writes (ZL40251, ZL40253 Only). The internal EEPROM memory is accessible when the EESEL bit is 1. After driving CSN low, the bus master transmits the write enable command and then drives CSN high to set the internal write enable latch. The bus master then drives CSN low again and transmits the write command followed by the 16-bit address followed by the first data byte to be written. The device first copies the page to be written from EEPROM to its page buffer. The device then receives the first data byte on MOSI, writes it to its page buffer,

increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the device continues to write the data received to its page buffer and continues to increment its address counter. The address counter rolls over at the 32-byte page boundary (i.e. when the five least-significant address bits are 11111). When the bus master drives CSN high, the device transfers the data in the page buffer to the appropriate page in the EEPROM memory. See Figure 6 and Figure 7.

EEPROM Read Status (ZL40251, ZL40253 Only). After the bus master drives CSN high to end an EEPROM write command, the EEPROM memory is not accessible for up to 5ms while the data is transferred from the page buffer. To determine when this transfer is complete, the bus master can use the Read Status command. After driving CSN low, the bus master transmits the Read Status command. The device then responds with the status byte on MISO. In this byte, the least significant bit is set to 1 if the transfer is still in progress and 0 if the transfer has completed.

Early Termination of Bus Transactions. The bus master can terminate SPI bus transactions at any time by pulling CSN high. In response to early terminations, the device resets its SPI interface logic and waits for the start of the next transaction. If a register write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, the data byte is not written. On devices with internal EEPROM, if an EEPROM write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, none of the bytes in that write transaction are written.

Design Option: Wiring MOSI and MISO Together. Because communication between the bus master and the device is half-duplex, the MOSI and MISO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the MOSI/MISO line when the device is transmitting.

AC Timing. See Table 15 and Figure 17 for AC timing specifications for the SPI interface.

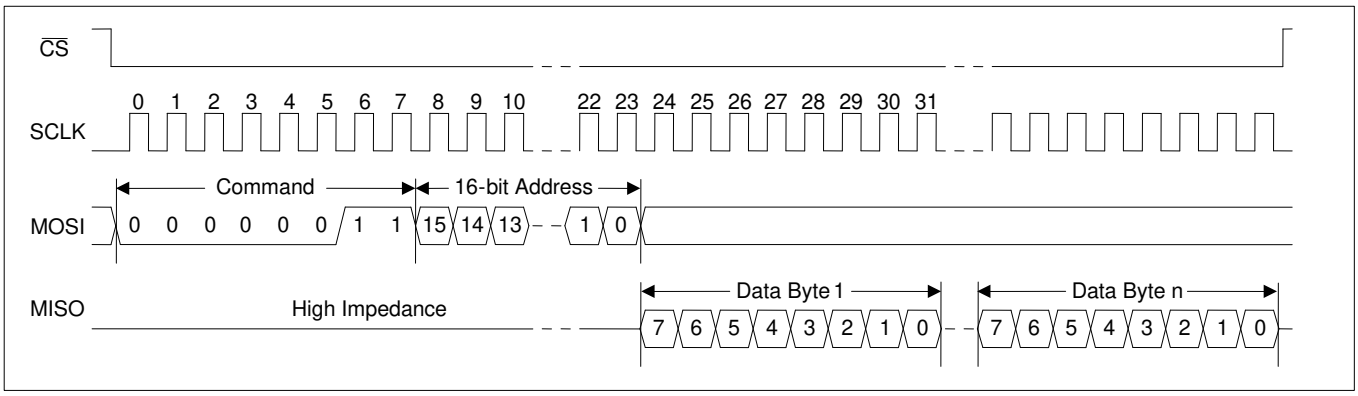

Figure 5 - SPI Read Transaction Functional Timing

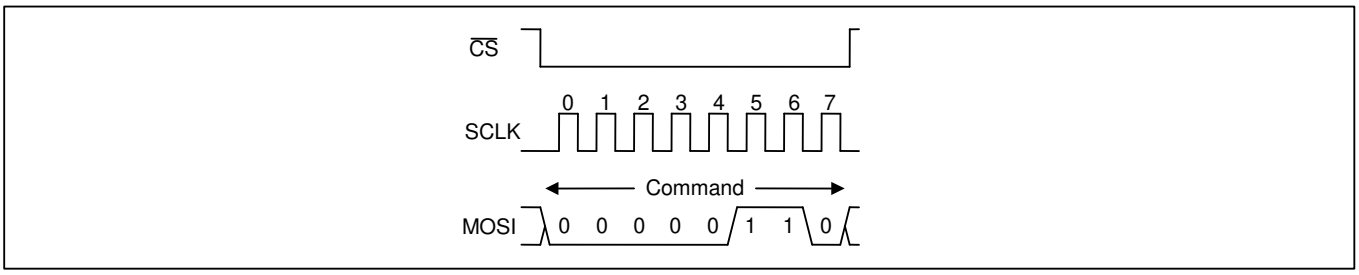

Figure 6 - SPI Write Enable Transaction Functional Timing (ZL40251 and ZL40253 Only)

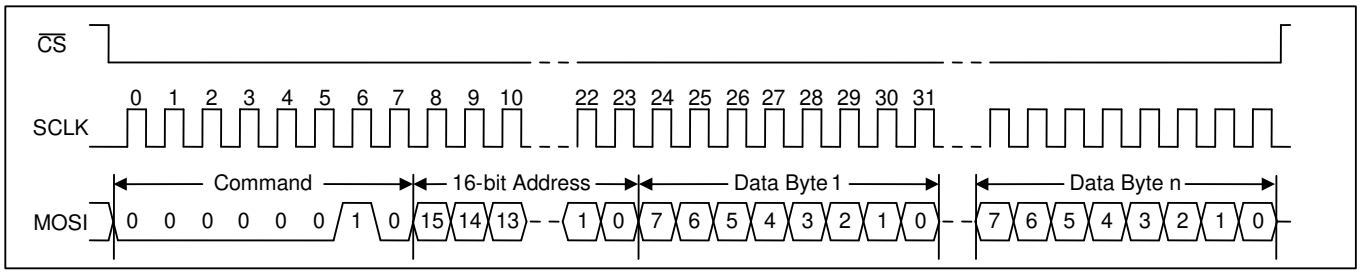

Figure 7 - SPI Write Transaction Functional Timing

4.7.2 SPI Master (ZL40250 and ZL40252 Only)

After reset these devices can present a SPI master port on the CSN, SCLK, MOSI, and MISO pins for auto-configuration using data read from an external SPI EEPROM. During auto-configuration the device is always the SPI master and generates the CSN and SCLK signals. The device transmits serial data on the the MOSI (Master Out Slave In) pin and receives serial data on the MISO (Master In Slave Out) pin.

Bit Order. The register address and all data bytes are transmitted most significant bit first on both MOSI and MISO.

Clock Polarity and Phase. The device latches data on MISO on the rising edge of SCLK and updates data on MOSI on the falling edge of SCLK.

Device Selection. Each SPI device has its own chip-select line. To select the external EEPROM, the device drives the CSN signal low.

Command and Address. After driving CSN low, the device transmits an 8-bit read command followed by a 16-bit register address. The read command is shown below.

Command	Hex	Bit Order, Left to Right
Read	0x03	0000 0011

Read Transactions. After driving CSN low, the device transmits the read command followed by the 16-bit register address. The external EEPROM then responds with the requested data byte on MISO, increments its address counter, and prefetches the next data byte. If the device continues to demand data, the EEPROM continues to provide the data on MISO, increment its address counter, and prefetch the following byte. The read transaction is completed when the device drives CSN high. See Figure 5.

Writing the External EEPROM. Due to the small package size and low pin count of the device, there is no way to use the ZL40250 or ZL40252 to write the external EEPROM. The auto-configuration data used by the ZL40250 or ZL40252 must be pre-programmed into the EEPROM by some other method, such as:

1. The EEPROM manufacturer can write the data to the EEPROM during production testing. This is a service they routinely provide.
2. A contract manufacturer or distributor can write the data to the EEPROM using a production EEPROM programmer before the EEPROM is mounted to the board.

4.7.3 I²C Slave

The device can present a fast-mode (400kbit/s) I²C slave port on the SCL and SDA pins. I²C is a widely used master/slave bus protocol that allows one or more masters and one or more slaves to communicate over a two-wire serial bus. I²C masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master, which also generates the SCL signal. The device is compliant with version 2.1 of the I²C specification.

The I²C interface on the device is a protocol translator from external I²C transactions to internal SPI transactions. This explains the slightly increased protocol complexity described in the paragraphs that follow.

Read Transactions. The device registers are accessible when the EESEL bit is 0. On ZL40251 and ZL40253 the internal EEPROM memory is accessible when the EESEL bit is 1. On ZL40250 and ZL40252 the EESEL bit must be set to 0. The bus master first does an I²C write to the device. In this transaction three bytes are written: the SPI Read command (see Table 3), the upper byte of the register address, and the lower byte of the register address. The bus master then does an I²C read. During each acknowledge (A) bit the device fetches data from the read address and then increments the read address. The device then transmits the data to the bus master during the next 8 SCL cycles. The bus master terminates the read with a not-acknowledge (NA) followed by a STOP condition (P). See Figure 8. After the I²C write there can be unlimited idle time on the bus before the I²C read, but the device cannot tolerate other I²C bus traffic between the I²C write and the I²C read. Care must be taken to ensure that the I²C read is the first command on the bus after the I²C write to ensure the two-part read transaction happens correctly.

Register Write Transactions. The device registers are accessible when the EESEL bit is 0. The bus master does an I²C write to the device. The first three bytes of this transaction are the SPI Write command (see Table 3), the upper byte of the register address, and the lower byte of the register address. Subsequent bytes are data bytes to be written. After each data byte is received, the device writes the byte to the write address and then increments the write address. The bus master terminates the write with a STOP condition (P). See Figure 9.

EEPROM Writes (ZL40251 and ZL40253 Only). The EEPROM memory is accessible when the EESEL bit is 1. The bus master first does an I²C write to transmit the SPI Write Enable command (see Table 3) to the device. The bus master then does an I²C write to transmit data to the device as described in the Register Write Transactions paragraph above. See Figure 10.

EEPROM Read Status (ZL40251 and ZL40253 Only). The bus master first does an I²C write to transmit the SPI Read Status command (see Table 3) to the device. The bus master then does an I²C read to get the status byte. In this byte, the least significant bit is set to 1 if the transfer is still in progress and 0 if the transfer has completed. See Figure 11. Similar to read transactions described above, the I²C write and the I²C read cannot be separated by other I²C bus traffic.

I²C Features Not Supported by the Device. The I²C specification has several optional features that are not supported by the device. These are: 3.4Mbit/s high-speed mode (Hs-mode), 10-bit device addressing, general call address, software reset, and device ID. The device does not hold SCL low to force the master to wait.

I²C Slave Address. By default the upper 5 bits of the device's 7-bit slave address are fixed at 11101 and the lower 2 bits can be pin-configured for any of three values as shown in the table in section 4.2. For a device that can auto-configure from EEPROM at power-up, its I²C slave address can be set to any value during auto-configuration at power-up by writing the the I2CA register as part of the configuration script.

Bit Order. The I²C specification requires device address, register address and all data bytes to be transmitted most significant bit first on the SDA signal.

Note: as required by the I²C specification, when power is removed from the device, the SDA and SCL pins are left floating so they don't obstruct the bus lines.

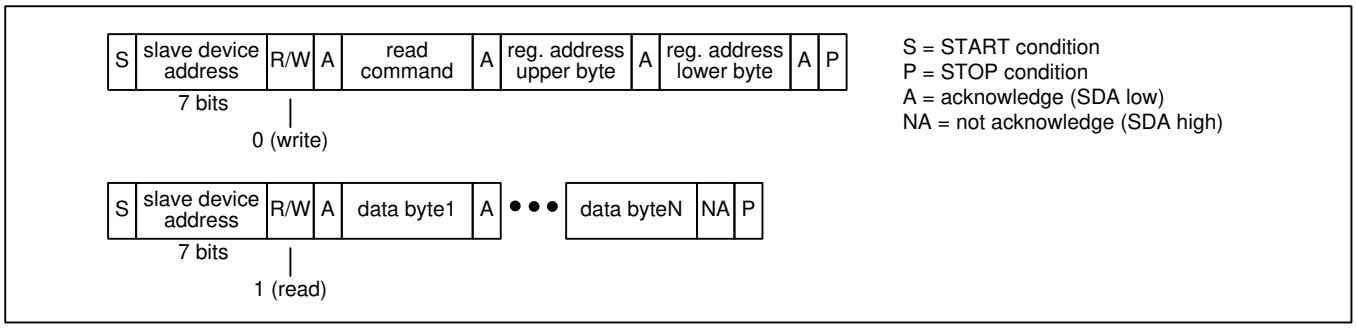

Figure 8 - I²C Read Transaction Functional Timing

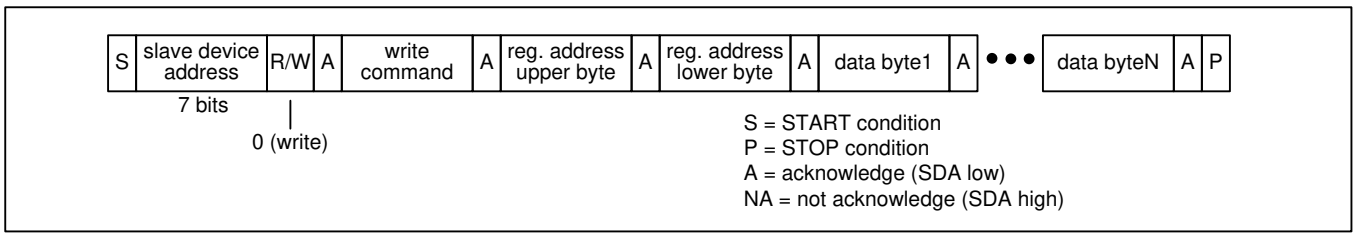

Figure 9 - I²C Register Write Transaction Functional Timing

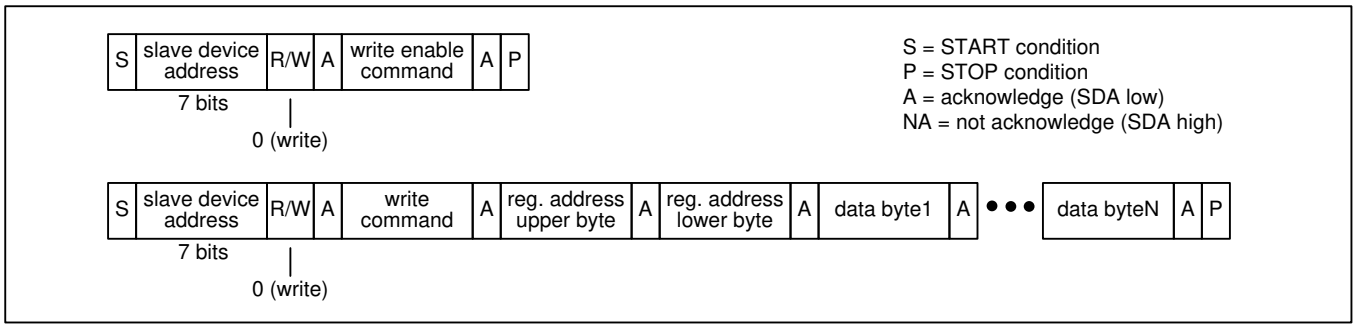

Figure 10 - I²C EEPROM Write Transaction Functional Timing (ZL40251 and ZL40253 Only)

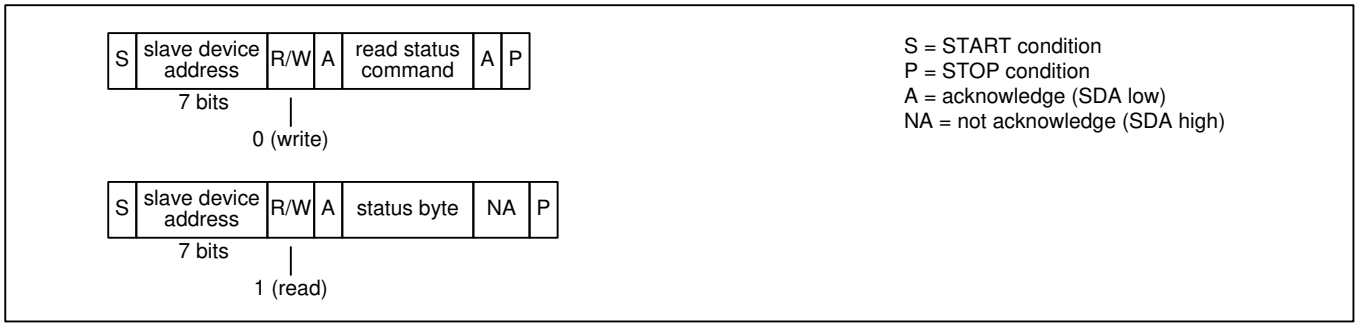

Figure 11 - I²C EEPROM Read Status Transaction Functional Timing (ZL40251 and ZL40253 Only)

Note: In Figure 8 through Figure 11, a STOP condition (P) immediately followed by a START condition (S) can be replaced by a repeated START condition (Sr) as described in the I²C specification.

4.8 Interrupt Logic

Any of the GPIO pins can be configured as an interrupt-request output by setting the appropriate GPIOxC field in the GPIOCR registers to one of the status output options (01xx) and configuring the appropriate GPIOxSS register to follow the INTSR.INT bit. If system software is written to poll rather than receive interrupt requests, then software can read the INTSR.INT bit first to determine if any interrupt requests are active in the device.

Many of the latched status bits in the device can be the source of an interrupt request if their corresponding interrupt enable bits are set. The device's interrupt logic is shown in Figure 12. See the register map (Table 4) and the status register descriptions in section 5.3.2 for descriptions of the register bits shown in the figure.

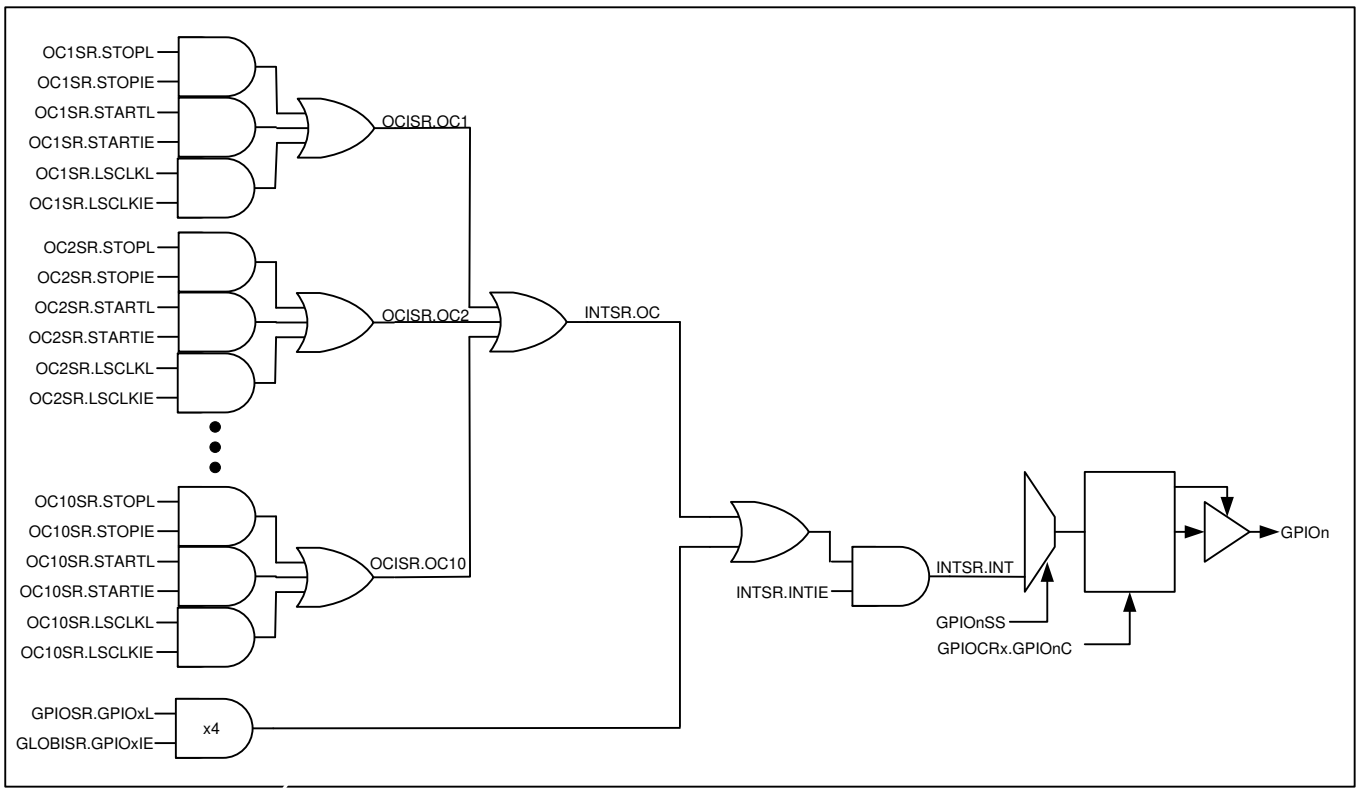

Figure 12 - Interrupt Structure

4.9 Reset Logic

The device has three reset controls: the RSTN pin, and the hard reset (HRST) and soft reset (SRST) bits in MCR1. The RSTN pin asynchronously resets the entire device. When the RSTN pin is low all internal registers are reset to their default values. When RSTN returns high the device's auto-configuration boot controller is started. **The RSTN pin must be asserted once after power-up.** Reset should be asserted for at least 1µs.

Asserting the MCR1.HRST (hard reset) bit is functionally similar to asserting the RSTN pin. The HRST bit resets the entire device except for the microprocessor interface, the HRST bit itself, the I2CA register, and CFGSR.IF[1:0]. While HRST=1 the device accepts register writes so that HRST can be set back to 0, but register reads are not allowed. When HRST is set back to 0, the TEST and AC[2:0] pins are sampled as described in section 4.2, but, unlike when RSTN is deasserted, the IF[1:0] pins are not sampled so that the device remains in the same interface mode (SPI or I^2C) and maintains the same slave address when in I^2C mode. When HRST is set back to 0, the device's auto-configuration boot controller is started after a 1 to 3µs delay.

The MCR1.SRST (soft reset) bit resets the entire device except for the microprocessor interface, the SRST bit itself, the MCR1.HRST bit, the I2CA register, and the CFGSR register. When the SRST bit is asserted the device's auto-configuration boot controller is **not** started.

Microsemi recommends holding RSTN low while the internal ring oscillator starts up and stabilizes. An incorrect reset condition could result if RSTN is released before the oscillator has started up completely.

Important: System software must wait at least 100µs after RSTN is deasserted and wait for GLOBISR.BCDONE=1 before configuring the device.

4.10 Power-Supply Considerations

Due to the multi-power-supply nature of the device, some I/Os have parasitic diodes between a lower-voltage supply and a higher-voltage supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the lower-voltage supply and the higher-voltage supply to force the higher-voltage supply to be within one parasitic diode drop of the lower-voltage supply. The second method is to ramp up the higher-voltage supply first and then ramp up the lower-voltge supply.

Important Note: The voltages on VDDL, VDDIO, and all VDDOx pins must not exceed VDDH. Not complying with this requirement may damage the device.

4.11 Auto-Configuration from EEPROM or ROM

For ZL40250 and ZL40252, the device optionally can configure itself at reset from an internal ROM. The ROM stores eight configurations, known as configurations 0 through 7. As described in section 4.2.1, IF[1:0] must be 00, 01 or 10 at reset, and the device configuration to be used is specified by the values of the AC[2:0] pins at reset (0 through 7). Descriptions of the standard-product ROM configurations are available from Microsemi.

For ZL40250 and ZL40252, the device optionally can configure itself at reset from an external EEPROM connected to its SPI interface. The EEPROM can store up to eight configurations, known as configurations 0 through 7. As described in section 4.2.1, IF[1:0] must be 11 at reset, and the device configuration to be used is specified by the values of the AC[2:0] pins at reset (0 through 7).

For ZL40251 and ZL40253, the internal EEPROM memory can store up to eight device configurations, known as configurations 0 through 7. As described in section 4.2.2, the device configuration to be used is specified by the values of the AC[2:0] pins at reset.

4.11.1 Generating Device Configurations

Device configurations are most easily generated using the evaluation software. This is true for auto-configurations stored in internal or external EEPROM and for configurations that are written to the device by a system processor. See section 4.12 for guidance if device configurations must be developed without using the evaluation software.

4.11.2 Direct EEPROM Write Mode (ZL40251 and ZL40253 Only)

To simplify writing the device's internal EEPROM during manufacturing, the device has a test mode known as direct EEPROM write mode. The device enters this mode when TEST=1, AC[2:0]=000 and IF[1:0]=11 on the rising edge of RSTN. In this mode the EEPROM memory is mapped into the address map and can be written as needed to store configuration scripts in the device. Device registers are not accessible in this mode. The device exits this mode on the rising edge of RSTN. Note: the device drives the MISO pin continually during this mode. Therefore this mode cannot be used when MOSI and MISO are tied together as described in the **Design Option: Wiring MOSI and MISO Together** paragraph in section 4.7.1.

4.11.3 Holding Other Devices in Reset During Auto-Configuration

Using the appropriate GPIOCR and GPIO0SS registers, a GPIO pin can be configured to follow the GLOBISR.BCDONE status bit. This GPIO can then be used as a reset signal to hold other devices (device that use clocks from this device) in reset while the device configures itself. As an example, to configure GPIO0 to follow BCDONE with 0=reset add the following writes at the beginning of the configuration file: write 0x1F to GPIO0SS and write 0x04 to GPIOCR1.

4.12 Configuration Sequence

Device configurations are most easily generated using the evaluation software, which automatically generates configurations that follow Microsemi's suggested sequence. To develop device configurations manually (i.e. from device documentation rather than the evaluation software) see Application Note ZLAN-591 for Microsemi's suggested device configuration sequence.

4.13 Power Supply Decoupling and Layout Recommendations

Application Note ZLAN-592 describes recommended power supply decoupling and layout practices.

5. Register Descriptions

Table 4 shows the register map. In each register, bit 7 is the MSb and bit 0 is the LSb. Register addresses not listed are reserved. Bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 4.

5.1 Register Types

5.1.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status bits can cause an interrupt request if enabled to do so by corresponding interrupt enable bits. Status bits marked "—" are reserved and must be ignored.

5.1.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

5.1.3 Bank-Switched Registers (ZL40251 and ZL40253 Only)

The EESEL register is a bank-select control field that maps the device registers into the memory map at address 0x1 and above when the EESEL bit is 0 and maps the EEPROM memory into the memory map at address 0x1 and above when the EESEL bit is 1. The EESEL register itself is always in the memory map at address 0x0.

5.2 Register Map

Table 4 - Register Map

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Global Configuration Registers									
00h	EESEL	EESEL	—	—	—	—	—	—	—
01	MCR1	SRST	HRST	STOP	—	ROSCD	AINCDIS	ODMISO	—
02	MCR2	—	—	—	—	—	—	XAB[1:0]	
04	ICEN	—	—	—	—	—	IC3EN	IC2EN	IC1EN
05	OCEN1	OC8EN	OC7EN	OC6EN	OC5EN	OC4EN	OC3EN	OC2EN	OC1EN
06	OCEN2	—	—	—	—	—	—	OC10EN	OC9EN
07	OCMUX1	—	—	OCMUXC[1:0]		OCMUXB[1:0]		OCMUXA[1:0]	
08	OCMUX2	—	—	OCMUXF[1:0]		OCMUXE[1:0]		OCMUXD[1:0]	
09	STOPCR1	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1
0A	STOPCR2	—	—	—	—	—	—	OC10	OC9
0B	GPIOCR1	GPIO1C[3:0]				GPIO0C[3:0]			
0C	GPIOCR2	GPIO3C[3:0]				GPIO2C[3:0]			
0D	GPIO0SS	REG[4:0]					BIT[2:0]		
0E	GPIO1SS	REG[4:0]					BIT[2:0]		
0F	GPIO2SS	REG[4:0]					BIT[2:0]		
10	GPIO3SS	REG[4:0]					BIT[2:0]		
11	I2CA	—	I2CA[6:0]						
Status Registers									
30	ID1	IDU[7:0]							
31	ID2	IDL[3:0]				REV[3:0]			
40	CFGSR	CFGD	—	IF[1:0]		TEST	AC[2:0]		
41	GPIOSR	GPIO3L	GPIO2L	GPIO1L	GPIO0L	GPIO3	GPIO2	GPIO1	GPIO0
42	INTSR	—	—	OC	—	—	—	INTIE	INT
43	GLOBISR	BCDONE	—	—	—	GPIO3IE	GPIO2IE	GPIO1IE	GPIO0IE
45	OCISR1	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1
46	OCISR2	—	—	—	—	—	—	OC10	OC9
48	P1SR	—	—	—	—	—	—	—	SELREF
49	P2SR	—	—	—	—	—	—	—	SELREF
50	OC1SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
51	OC2SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
52	OC3SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
53	OC4SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
54	OC5SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
55	OC6SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
56	OC7SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
57	OC8SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
58	OC9SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
59	OC10SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
Path 1 Configuration Registers									
100	P1CR1	—	DALIGN	EXTSS[1:0]		—	—	1	—
102	P1CR3	—	EXTSW	ALTMUX[2:0]			MUX[2:0]		
Path 2 Configuration Registers									
180	P2CR1	—	DALIGN	EXTSS[1:0]		—	—	1	—
182	P2CR3	—	EXTSW	ALTMUX[2:0]			MUX[2:0]		

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Output Clock Configuration Registers									
	OC1 Registers								
200	OC1CR1	PHEN	MSDIV[6:0]						
201	OC1CR2	—	POL	DRIVE[1:0]		OCSF[3:0]			
202	OC1DIFF	VCM[3:0]				VOD[3:0]			
203	OC1REG	—	—	—	—	VREG[3:0]			
204	OC1CR3	SRLSEN	—	NEGLSD	LSSEL	—	—	—	LSDIV[24]
205	OC1DIV1	LSDIV[7:0]							
206	OC1DIV2	LSDIV[15:8]							
207	OC1DIV3	LSDIV[23:16]							
208	OC1DC	OCDC[7:0]							
209	OC1PH	—	—	—	—	PHADJ[3:0]			
20A	OC1STOP	—	SRC[3:0]				NEGLSD	MODE[1:0]	
	OC2 Registers								
210	OC2CR1	same as OC1 registers							
…	…								
21A	OC2STOP								
	OC3 Registers								
220	OC3CR1	same as OC1 registers							
…	…								
22A	OC3STOP								
	OC4 Registers								
230	OC4CR1	same as OC1 registers							
…	…								
23A	OC4STOP								
	OC5 Registers								
240	OC5CR1	same as OC1 registers							
…	…								
24A	OC5STOP								
	OC6 Registers								
250	OC6CR1	same as OC1 registers							
…	…								
25A	OC6STOP								
	OC7 Registers								
260	OC7CR1	same as OC1 registers							
…	…								
26A	OC7STOP								
	OC8 Registers								
270	OC8CR1	same as OC1 registers							
…	…								
27A	OC8STOP								
	OC9 Registers								
280	OC9CR1	same as OC1 registers							
…	…								
28A	OC9STOP								

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OC10 Registers								
290	OC10CR1	same as OC1 registers							
…	…								
29A	OC10STOP								
Input Clock Configuration									
300	XACR1	—	POL	—	—	—	—	HSDIV[1:0]	
301	XACR2	XOAMP[7:0]							
302	XACR3	XBCAP[3:0]				XACAP[3:0]			
303	IC1CR1	—	POL	—	—	—	—	HSDIV[1:0]	
304	IC2CR1	—	POL	—	—	—	—	HSDIV[1:0]	
305	IC3CR1	—	POL	—	—	—	—	HSDIV[1:0]	

5.3 Register Definitions

5.3.1 Global Configuration Registers

Register Name: EESEL
Register Description: EEPROM Memory Selection Register
Register Address: 00h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EESEL	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 7: EEPROM Memory Select (EESEL). This bit is a bank-select that specfies whether device register space or EEPROM memory is mapped into addresses 0x1 and above. This applies only to the ZL40251 and ZL40253. The ZL40250 and ZL40252 do not have internal EEPROM memory. Note that ROMSEL has priority over EESEL. See sections 4.7 and 5.1.3.

0 = Device registers
1= EEPROM memory

Register Name: MCR1
Register Description: Master Configuration Register 1
Register Address: 01h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SRST	HRST	STOP	—	ROSCD	AINCDIS	ODMISO	—
Default	0	0	0	0	0	0	0	0

Bit 7: Soft Reset (SRST). This bit resets the entire device except for the microprocessor interface, the SRST bit itself, the MCR1.HRST bit, the I2CA register, and CFGSR bits 5:0. When SRST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. When the SRST bit is asserted the device's auto-configuration boot controller is **not** started. See section 4.9.

0 = Normal operation
1 = Reset

Bit 6: Hard Reset (HRST). Asserting this bit is functionally equivalent to asserting the RSTN pin. The HRST bit resets the entire device except for the microprocessor interface and the HRST bit itself. Register fields with pin-programmed defaults latch their values from the corresponding input pins, and the device's auto-configuration boot controller is started. See section 4.9.

0 = Normal operation
1 = Reset

Bit 5: Output Clock Stop (STOP). Asserting this bit stops all output clocks that are configured with OCxSTOP.SRC=0001. Note that this signal is ORed with the per-output stop control bit in the STOPCR registers to make each output's internal stop control signal. See section 4.6.6.

Bit 3: Ring Oscillator Disable (ROSCD). This bit disables the ring oscillator. It can be set to 1 when auto-configuration is complete. See section 4.3.3.

0 = Enable
1 = Disable (power-down)

Bit 1: Open Drain MISO Enable (ODMISO). This bit configures the MISO pin to be open-drain. When this bit is set, the MISO pin only drives low and must have an external pullup resistor.

0 = Disable (MISO drives 0 and 1, high-impedance when not driven)
1 = Enable (MISO drives 0 only, high-impedance all other times)

Register Name: MCR2
Register Description: Master Configuration Register 2
Register Address: 02h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	XAB[1:0]	
Default	0	0	0	0	0	0	0	0

Bits 1 to 0: XA/XB Pin Mode (XAB[1:0]). This field specifies the behavior of the XA and XB pins. See section 4.3.

00 = Crystal driver and input disabled / powered down
01 = Crystal driver and input enabled on XA/XB
10 = XA enabled as single-ended input for external oscillator signal; XB must be left floating
11 = {unused value}